MOTOROLA FAST AND LS TTL DATA

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REV 4

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REV 4

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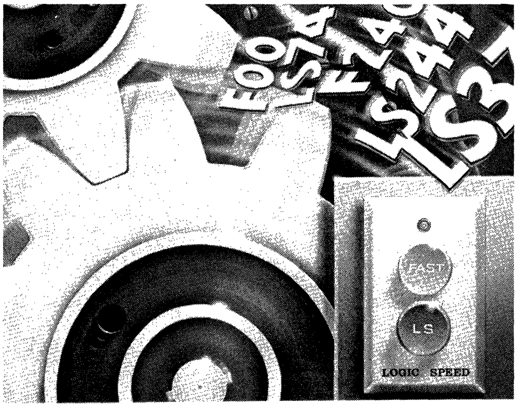
LS
LOGIC SPEED

FAST AND LS TTL DATA

FAST AND LS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FAST AND LS

Prepared by
Technical Information Center

Low Power Schottky (LSTTL) has become the industry standard logic in recent years, replacing the original 7400 TTL with lower power and higher speeds. In addition to offering the standard LS TTL circuits, Motorola offers the FAST Schottky and TTL family. Complete specifications for each of these families are provided in data sheet form. Functional selector guides not only provide an overview of already introduced devices but planned introduction dates of new products.

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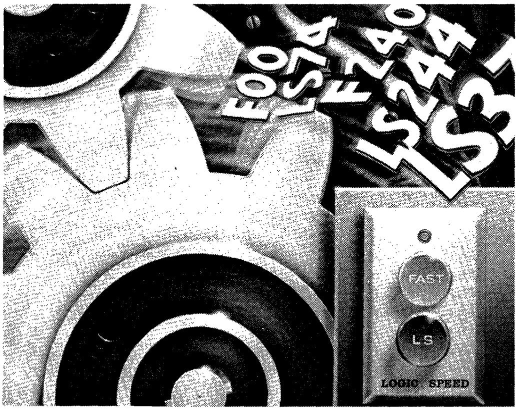
Selection Information
FAST/LS

FAST AND LS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LOGIC SPEED

GENERAL INFORMATION

TTL in Perspective

Since its introduction, TTL has become the most popular form of digital logic. It has evolved from the original gold-doped saturated 7400 logic, to Schottky-Clamped logic, and finally to the modern advanced families of TTL logic. The popularity of these TTL families stem from their ease of use, low cost, medium-to-high speed operation, and good output drive capability.

Motorola offers two modern TTL logic families — LS and FAST™. They are pin and functionally compatible and can easily be combined in a system to achieve maximum performance at minimum cost.

LS (Low Power Schottky) is currently the more popular and commands by far the largest share of the total TTL logic market. It is low-cost and provides moderate performance at low power.

FAST, the state-of-the-art, high-performance TTL family, is growing rapidly and gaining a significant share of the total TTL logic market. FAST offers a 20–30 percent improvement in performance over the older Standard Schottky family (74S) with a 75–80 percent reduction in power. When compared with the Advanced Schottky family (74AS), FAST offers nearly equal performance at a 25–50 percent savings in power.

FAST is manufactured on Motorola's MOSAIC (oxide-isolated) process. This process provides FAST with inherent speed/power advantages over the older junction-isolated 74S and 74LS families, allowing the FAST family to be designed and specified with improved noise margins, reduced input currents, and superior line driving capabilities in comparison to these earlier families. Additionally, FAST designs incorporate power-down circuitry on all three-state outputs, and buffered outputs on all storage devices.

Two further advantages of FAST are the load specifications and power supply specifications. FAST ac characteristics are specified at a heavier capacitive load than the earlier families (50 pF versus 15 pF) to more accurately reflect actual in-circuit performance. Motorola's dc and ac characteristics for FAST are specified over a full 10% supply voltage range — a significant improvement over the industry standard specifications for the earlier families (5% for dc, 0% for ac).

These design and specification improvements offered by the Motorola FAST family provide the user with better system performance, enhanced design flexibility, and more reliable system operation.

TTL Family Comparisons

General Characteristics for Schottky TTL Logic

(ALL MAXIMUM RATINGS)

		LS		FAST		
Characteristic	**Symbol**	**54LSxxx**	**74LSxxx**	**54Fxxx**	**74Fxxx**	**Units**
Operating Voltage Range	V_{CC}	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	Vdc
Operating Temperature Range	T_A	−55 to 125	0 to 70	−55 to 125	0 to 70	°C
Input Current	I_{IN} I_{IH}	20	20	20	20	µA
	I_{IL}	−400	−400	−600	−600	
Output Drive	I_{OH}	−0.4	−0.4	−1.0	−1.0	mA
Standard Output	I_{OL}	4.0	8.0	20	20	mA
	I_{SC}	−20 to −100	−20 to −100	−60 to −150	−60 to −150	mA
	I_{OH}	−12	−15	−12	−15	mA
Buffer Output	I_{OL}	12	24	48	64	mA
	I_{SC}	−40 to −225	−40 to −225	−100 to −225	−100 to −225	mA

Speed/Power Characteristics for Schottky TTL Logic(1)

(ALL TYPICAL RATINGS)

Characteristic	Symbol	LS	FAST	Units
Quiescent Supply Current/Gate	I_G	0.4	1.1	mA
Power/Gate (Quiescent)	P_G	2.0	5.5	mW
Propagation Delay	t_p	9.0	3.7	ns
Speed Power Product	—	18	19.2	pJ
Clock Frequency (D-F/F)	f_{max}	33	125	MHz
Clock Frequency (Counter)	f_{max}	40	125	MHz

NOTES: 1. Specifications are shown for the following conditions:
a) V_{CC} = 5.0 Vdc (AC);
b) T_A = 25°C
c) C_L = 50 pF for FAST; 15 pF for LS

Functional Selection

Abbreviations

S = Synchronous
A = Asynchronous
B = Both Synchronous and Asynchronous

2S = 2-State Output
3S = 3-State Output
OC = Open-Collector Output

P = Planned (See FAST/LS Selector Guide, SG-60 for latest availability status)
X = Available

Inverters

Description	Type of Output	No.	LS	FAST
Hex	2S	04	X	X
	OC	05	X	

AND Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	08	X	X
	OC	09	X	
Triple 3-Input	2S	11	X	X
	OC	15	X	
Dual 4-Input	2S	21	X	X

NAND Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	00	X	X
	OC	01	X	
	OC	03	X	
Quad 2-Input, High Voltage	OC	26	X	
Triple 3-Input	2S	10	X	X
	OC	12	X	
Dual 4-Input	2S	20	X	X
	OC	22	X	
8-Input	2S	30	X	
13-Input	2S	133	X	

OR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	32	X	X

NOR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	2	X	X
Triple 3-Input	2S	27	X	
Dual 5-Input	2S	260	X	

Exclusive OR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	86	X	X
	OC	136	X	
	2S	386	X	

Exclusive NOR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	OC	266	X	

AND-OR-INVERT Gates

Description	Type of Output	No.	LS	FAST
Dual 2-Wide, 2-Input 3-Input	2S	51	X	X
4-Wide, 2-3-2-3-Input	2S	54	X	
2-Wide, 4-Input	2S	55	X	
4-Wide, 4-2-2-3-Input	2S	64		X

Schmitt Triggers

Description	Type of Output	No.	LS	FAST
Dual 4-Input NAND Gate	2S	13	X	X
Hex, Inverting	2S	14	X	X
Quad 2-Input NAND Gate	2S	132	X	X

SSI Flip-Flops

Description	Clock Edge	No.	LS	FAST
Dual D w/Set & Clear	Pos	74	X	X
Dual JK w/Set	Neg	113	X	P
Dual JK w/Clear	Neg	73	X	
	Neg	107	X	
Dual JK w/Set & Clear Individual J, K, C_P, S_D, C_D Inputs	Neg	76	X	
Dual JK w/Set & Clear Common C_O, C_P	Neg	78	X	
Same as 76 with Different Pinout	Neg	112	X	P
Same as 112 with Different Pinout	Neg	114	X	P
Dual $J\overline{K}$ w/Set & Clear	Pos	109	X	X

Multiplexers

Description	Type of Output	No.	LS	FAST
Quad 2-to-1, Non-Inverting	2S	157	X	X
	2S	157A		X
	3S	257	X	X
	2S	257A		X
Quad 2-to-1, Inverting	2S	158	X	X
	2S	158A		X
	3S	258	X	X
	2S	258A		X
Dual 4-to-1, Non-Inverting	2S	153	X	X
	3S	253	X	X
Dual 4-to-1, Inverting	2S	352	X	X
	3S	353	X	X
8-to-1	2S	151	X	X
	3S	251	X	X
Quad 2-to-1 with Output Register				
398 — Positive edge triggered, $Q/\overline{Q}$ Outputs	2S	398	X	X
399 — Positive edge triggered, Q Output Only	2S	399	X	X

Decoders/Demultiplexers

Description	Type of Output	No.	LS	FAST
Dual 1-of-4	2S	139	X	X
	2S	155	X	
	OC	156	X	
	3S	539		X
1-of-8	2S	138	X	X
	3S	538		X
1-of-8 with Latch	2S	137	X	
1-of-10	2S	42	X	
	3S	537		X

Latches

Description	No. of Bits	Type of Output	No.	LS	FAST
Transparent, Non-Inverting	4	2S	77	X	
	8	3S	373	X	X
Octal, Non-Inverting	8	3S	573		
Transparent, Inverting	8	3S	533		X
Transparent, Q and $\overline{Q}$ Outputs	4	2S	75	X	
	4	2S	375	X	
Quad Set-Reset Latch	4	2S	279	X	
Addressable	8	2S	259	X	X
Dual 4-Bit Addressable	4	2S	256	X	X

Encoders

Description	Type of Output	No.	LS	FAST
10-to-4-Line BCD	2S	147	X	
8-to-3-Line Priority Encoder	2S	148	X	X
	3S	348	X	
	2S	748	X	
	3S	848	X	

Register Files

Description	Type of Output	No.	LS	FAST
4 x 4	OC	170	X	
	3S	670	X	

Shift Registers

Description	No. of Bits	Type of Output	Mode*				No.	LS	FAST
			SR	SL	Hold	Reset			
Serial In-Serial Out	8	2S	X				91	X	
Serial In-Parallel Out	8	2S	X			A	164	X	P
Parallel In-Serial Out	8	2S	X		X		165	X	
	8	2S	X		X	A	166	X	
	16	3S	X		X		674	X	
Parallel In-Parallel Out	4	2S	X				95	X	
	4	2S	X	X	X	A	194	X	X
	4	2S	X			A	195	X	P
	4	3S	X				295	X	
	4	3S	X			A	395	X	
Parallel In-Parallel Out, Bidirectional	8	3S	X	X	X	A	299	X	P
	8	3S	X	X	X	S	323	X	P
Sign Extended Bidirectional	8	3S	X		X	A	322	X	
Serial In-Parallel Out with Storage Register	16	2S/3S	X	X	X	S	673	X	

* SR = Shift Right
SL = Shift Left

Asynchronous Counters — Negative Edge-Triggered

Description	Load	Set	Reset	No.	LS	FAST
Decade (2/5)		X	X	90	X	
	X		X	196	X	
		X	X	290	X	
Dual Decade (2/5)			X	390	X	
Dual Decade		X	X	490	X	
Modulo 12 (2/6)			X	92	X	
4-Bit Binary (2/8)			X	93	X	
	X		X	197	X	
			X	293	X	
Dual 4-Bit Binary			X	393	X	
Divide-By-N (0–9)	X		X	716*	X	
Divide-By-N (0–15)	X		X	718*	X	

*The 716 and 718 are positive edge-triggered.

Display Decoders/Drivers with Open-Collector Outputs

Description	No.	LS	FAST
1-of-10	145	X	
BCD-to-7 Segment	47	X	
	48*	X	
	49	X	
	247	X	
	248*	X	
	249	X	

*The 48 and 248 have internal pullup resistors to V_{CC} on their outputs.

Cascadable Synchronous Counters — Positive Edge-Triggered

Description	Type of Output	Load	Reset	No.	LS	FAST
Decade	2S	S	A	160	X	
	2S	S	A	160A		X
	2S	S	S	162	X	X
Decade, Up/Down	2S	S		168	X	X
	2S	A		190	X	P
	2S	A	A	192*	X	P
	3S	S	B	568	X	X
	2S	S		668	X	
4-Bit Binary	2S	S	A	161	X	
	2S	S	A	161A		X
	2S	S	S	163	X	
	2S	S	S	163A		X
4-Bit Binary, Up/Down	2S	S		169	X	X
	2S	A		191	X	P
	2S	A	A	193*	X	P
	3S	S	B	569	X	X
	2S	S		669	X	

*The 192 and 193 do not provide a clock enable for synchronous cascading.

MSI Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	Clock Enable	No.	LS	FAST
D-Type, Non-Inverting	4	3S	A	X	173	X	
	4	2S		X	377	X	P
	6	2S	A		174	X	X
	6	2S		X	378	X	X
	8	2S	A		273	X	P
	8	3S			374	X	X
	8	3S			574		
Quad 2-Port	4	2S	A	X	398		X
	4	2S	A	X	399		X
D-Type, Inverting	8	3S			534		X
	8	3S			564		
D-Type, Q and $\overline{Q}$ Outputs	4	2S	A		175	X	X
	4	2S		X	379	X	X
Dual 8-Bit with Multiplexers	16	3S			604	X	
	16	OC			605	X	
	16	3S			606	X	
	16	OC			607	X	

Arithmetic Operators

Description	No.	LS	FAST
4-Bit Adder	83	X	
	283	X	X
4-Bit ALU	181	X	X
	381		X
	382		X
Look Ahead Carry Generator	182	X	X
Quad 4-Bit Adder/Subtractor	385	X	
Dual Carry/Save Full Adder	183	X	
4-Bit Barrel Shifter	350		X

Magnitude Comparators

Description	Type of Output	P=Q	P>Q	P<Q	No.	LS	FAST
4-Bit	2S	X	X	X	85	X	
8-Bit	2S	X	X		682	X	
	OC	X	X		683	X	
	2S	X	X		684	X	
	OC	X	X		685	X	
	2S	X			521		X
8-Bit with	2S	X	X		686	X	
Output	OC	X	X		687	X	
Enable	2S	X			688	X	
	OC	X			689	X	

Parity Generators/Checkers

Description	No.	LS	FAST
9-Bit Odd Even Parity Generator Checker	280	X	X

Dynamic Memory Support

Description	No.	LS	FAST
Synchronous Address Multiplexer (MC6883)	783	X	
Synchronous Address Multiplexer	785	X	
Error Detection and Correction Circuit	2960		X
(EDAC)	2960A		X
EDAC Bus Buffer (Inverting)	2961A		X
EDAC Bus Buffer (Non-Inverting)	2962A		X
Dynamic Memory Controller	2968A		X
Dynamic Memory Timing Controller with EDAC	2969		X
Dynamic Memory Timing Controller without EDAC	2970		P
1 MB DMC	29368		P

VCOs and Multivibrators

Description	No.	LS	FAST
Retriggerable Monostable Multivibrator	122	X	
Dual 122	123	X	
Precision Non-Retriggerable Monostable Multivibrator	221	X	
Voltage Crystal Controlled Oscillator	724	X	

Buffers/Line Drivers

Description	Type of Output	No.	LS	FAST
Quad 2-Input NOR	2S	28	X	
	OC	33	X	
Quad 2-Input NAND	2S	37	X	X
	OC	38	X	X
Dual 4-Input NAND	2S	40	X	X
Quad, Non-Inverting	3S	125	X	X
	3S	126	X	X
Hex, Non-Inverting	3S	365	X	X
	3S	367	X	X
Hex, Inverting	3S	366	X	X
	3S	368	X	X
Octal, Non-Inverting	3S	241	X	X
	3S	244	X	X
Bus Pinout	3S	541	X	
	3S	795	X	
	3S	797	X	
Octal, Inverting	3S	240	X	X
Bus Pinout	3S	540	X	
	3S	796	X	
	3S	798	X	

Transceivers

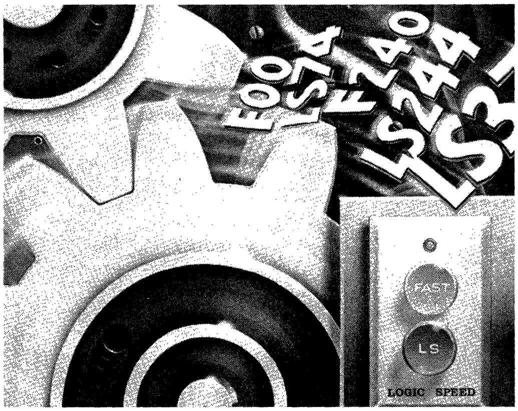
Description	Type of Output	No.	LS	FAST
Quad, Non-Inverting	3S	243	X	X
Quad, Inverting	3S	242	X	X
Octal, Non-Inverting	3S	245	X	X
	3S	645	X	
	OC	621	X	
	3S	623	X	P
	OC	641	X	
Bus Pinout	OC	543		P
Octal, Inverting	3S	620	X	P
	OC	622	X	
	3S	640	X	P
	OC	642	X	
	3S	643	x	P
	OC	644	X	
Octal, Non-Inverting with Register Mux	3S	646		P
	OC	647		P
Latch	3S	543		P
Octal, Inverting with Register Mux	3S	544		P
Latch				

Clock Drivers

Description	Type of Output	No.	LS	FAST
Quad Matched Propagation Delays		803		X

Circuit Characteristics

FAST AND LS


F00
LS74
F240
LS244
LS3
FAST
LS
LOGIC SPEED

CIRCUIT CHARACTERISTICS

FAMILY CHARACTERISTICS

LS TTL

The Low Power Schottky (LSTTL) family combines a current and power reduction improvement over standard 7400 TTL by a factor of 5. This is accomplished by using Schottky diode clamping to prevent saturation and advanced processing.

FAST TTL

The FAST Schottky TTL family provides a 75–80% power reduction compared to standard Schottky (54/74S) TTL and yet offers a 20–40% improvement in circuit performance over the standard Schottky due to the MOSAIC process. Also, FAST circuits contain additional circuitry to provide a flatter power/frequency curve. The input configuration of FAST uses a lower input current which translates into higher fanout.

CIRCUIT FEATURES

Circuit features of LS and FAST are best understood by examining the TTL 2-input NAND gate of each family (Figures 2-1a, b). The input/output circuits of other functions are almost identical.

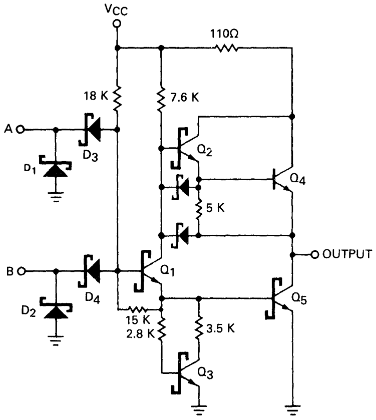

V_{CC}
110Ω
18 K
7.6 K
A
D_3
D_1
Q_2
Q_4
5 K
OUTPUT
B
Q_1
D_4
D_2
Q_5
15 K
2.8 K
3.5 K
Q_3

FIGURE 2-1a
LS00 — 2-INPUT NAND GATE

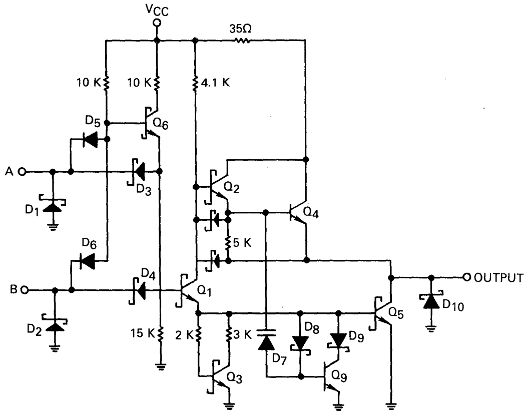

V_{CC}
35Ω
10 K
10 K
4.1 K
D_5
Q_6
A
D_3
D_1
Q_2
Q_4
5 K
D_6
D_4
OUTPUT
B
Q_1
D_{10}
Q_5
D_2
15 K
2 K
3 K
D_8
D_9
D_7
Q_3
Q_9

FIGURE 2-1b
F00 — 2-INPUT NAND GATE

INPUT CONFIGURATION. Motorola LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in Figure 2-1a. Compared to the classical multi-emitter structure, this circuit is faster and increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 7.0 V and the input breakdown voltage is typically 15 V or more.

The F00 input configuration utilizes a PN diode (D5 and D6) rather than the PNP transistor. This is required due to the high speed response of FAST™ logic. The PNP transistor, a relatively large device in current bipolar logic technology, has an associated capacitance large enough to make the gate input susceptible to ac noise. The PN diode results in much better ac noise immunity at the expense of increased input current.

Another input arrangement often used in LS MSI has three diodes connected as shown in Figure 2-2. This configuration gives a slightly higher input threshold than that of Figure 2-1a. A third input configuration that is sometimes used in LS TTL employs a vertical PNP transistor as shown in Figure 2-3. This arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the PNP input configuration have breakdown voltage ratings greater than 7.0 V.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in Figure 2-1a, b. These diodes conduct when an input signal goes negative, which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2 mA and with a duration greater than 500 ns can activate a parasitic lateral NPN transistor, which in turn can steal current from internal nodes of an LS circuit and thus cause logic errors.

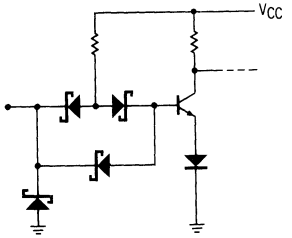


FIGURE 2-2
DIODE CLUSTER INPUT

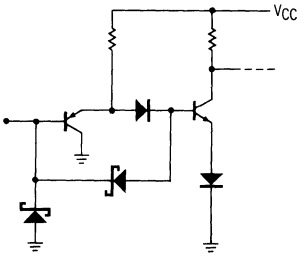


FIGURE 2-3
PNP INPUT

INPUT CHARACTERISTICS — Figure 2-4 shows the typical input characteristics of LS and FAST™. Typical transfer characteristics can be found in Figure 2-5 and input threshold variation with temperature information is provided in Table 2-1.

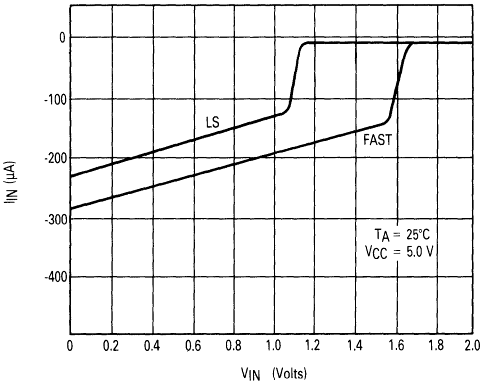


FIGURE 2-4
TYPICAL INPUT CURRENT vs INPUT VOLTAGE

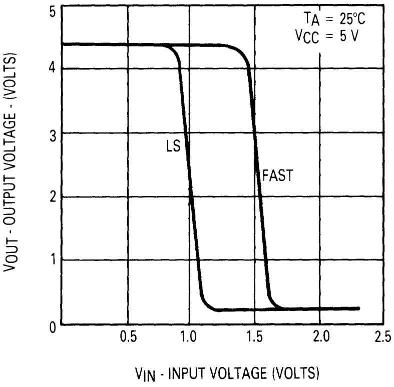


FIGURE 2-5
TYPICAL OUTPUT vs
INPUT VOLTAGE CHARACTERISTIC

TABLE 2.1
TYPICAL INPUT THRESHOLD VARIATION WITH TEMPERATURE

	-55°C	+25°C	+125°C
FAST	1.8	1.5	1.3
ALS	1.8	1.5	1.3
S	1.5	1.3	1.1
LS	1.2	1.0	0.8

OUTPUT CONFIGURATION. The output circuitry of LSTTL has several features not found in conventional TTL. A few of these features are discussed below.

Referring to Figures 2-1a, b, the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics (Figure 2-5) by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5k resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one V_{BE} below V_{CC} for low values of output current.

The F00 output includes clamping diodes to limit undershoot and control ringing on long signal lines. As with the input diode clamps, these diodes are intended for transient suppression only and should not be used as steady-state clamps.

The F00 output configuration also includes additional circuitry to improve the rise time and decrease the power consumption at high operating frequencies. This circuit, which consists of Q9, D7, D8, and D9 causes Q5 to off more quickly on LOW to HIGH output transitions.

Figure 2-6 shows the extra circuitry used to obtain the "high Z" condition in 3-state outputs. When the Output Enable signal is HIGH, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of two or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time.

FAST™ 3-state outputs have some additional circuitry due to the nature of the environment in which they are used. The effective capacitive load of a 3-state output tends to increase at high bus rates. The addition of Q10 reduces this effect by clamping the base of Q5 low when the device is in the high impedance state. In the high Z state, the output capacitance is about 5 pF for 24 mA outputs and about 12 pF for 64 mA outputs.

An additional feature of many FAST™ 3-state devices is the incorporation of power-up circuitry to guarantee that the output will not sink current if the device is disabled during the application or removal of power.

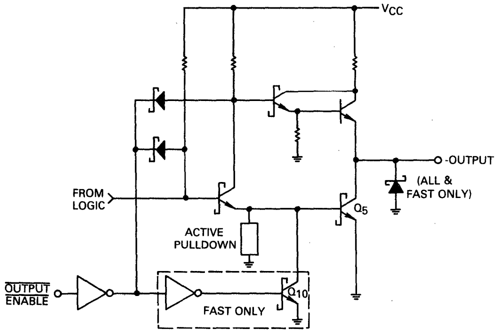


FIGURE 2-6
TYPICAL 3-STATE OUTPUT CONTROL

OUTPUT CHARACTERISTICS. Figure 2-7 shows the LOW-state output characteristics for LS and FAST™. For LOW I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. Figure 2-8 shows the HIGH-state output characteristics.

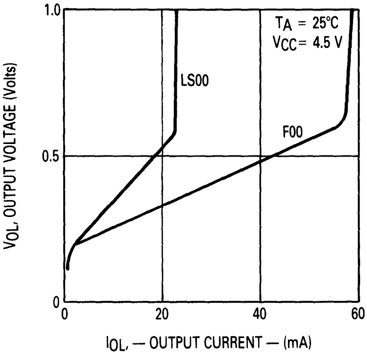


FIGURE 2-7a — OUTPUT LOW CHARACTERISTIC

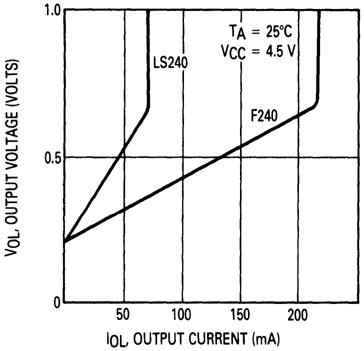


FIGURE 2-7b — OUTPUT LOW CHARACTERISTIC

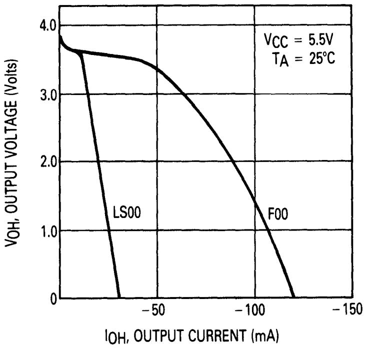


FIGURE 2-8a — OUTPUT HIGH CHARACTERISTIC

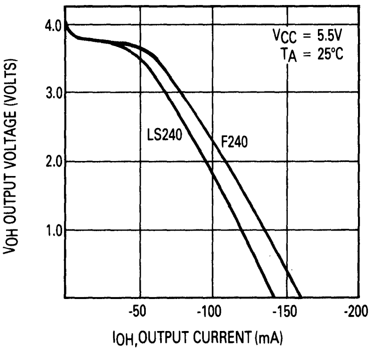


FIGURE 2-8b — OUTPUT HIGH CHARACTERISTIC

AC SWITCHING CHARACTERISTICS. The propagation through a logic element depends on power supply voltage, ambient temperature, and output load. The effect of each of these parameters on ac propagation is shown in Figures 2-9 through 2-11.

Propagation delays are specified with only one output switching, the delay through a logic-element will increase to some extent when multiple outputs switch simultaneously due to inductance internal to the IC package. This effect can be seen by comparing Figures 2-11e and 2-11f.

For LS TTL, limits are guaranteed at 25°C, V_{CC} = 5.0 V, and Cl = 15 pF (normally, resistive load has minimal effect on propagation delay) FAST™ and TTL limits are guaranteed over the commercial or military temperature and supply voltage ranges and with Cl = 50 pF.

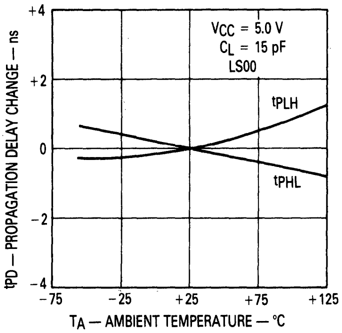


FIGURE 2-9

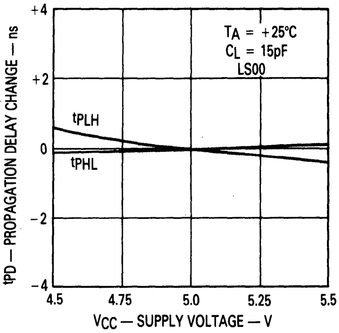


FIGURE 2-10

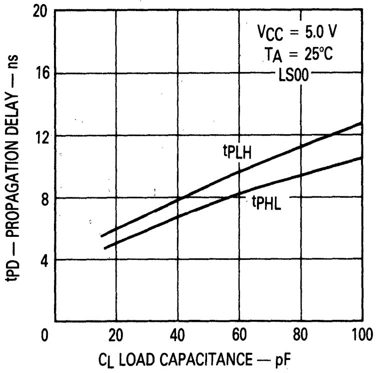


FIGURE 2-11a*

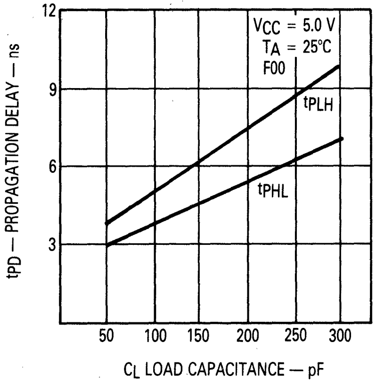


FIGURE 2-11b*

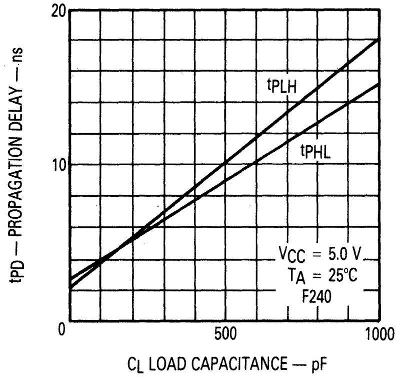


FIGURE 2-11c*

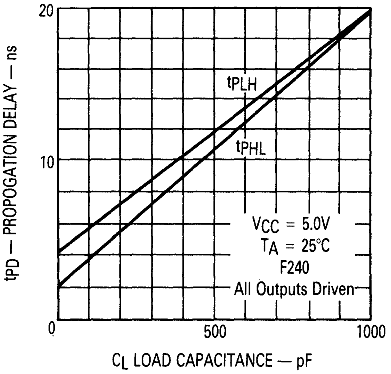


FIGURE 2-11d*

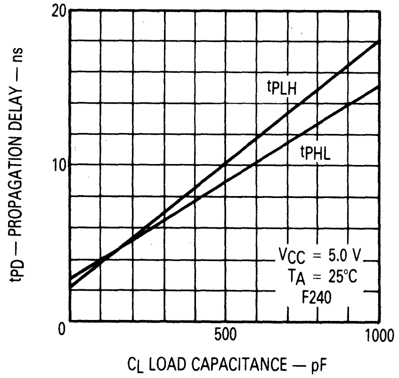


FIGURE 2-11e*

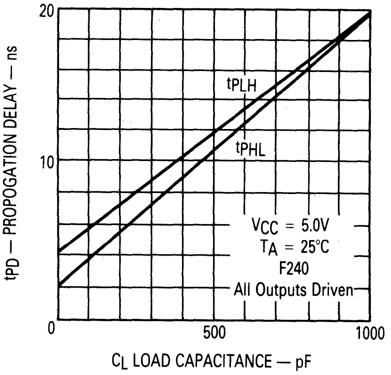
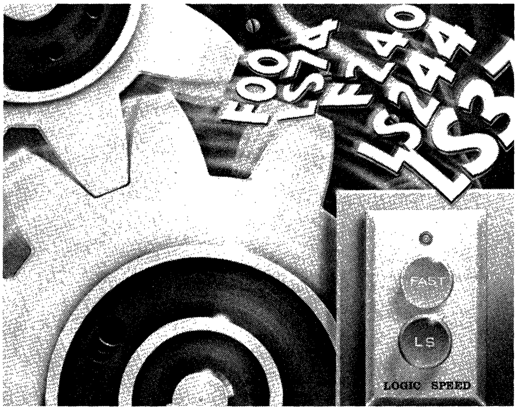


FIGURE 2-11f

*Data for Figures 2-11a through 2-11e was taken with only one output switching at a time. Figure 2-11f data was taken with all 8 inputs of the F240 tied together.

Design Considerations and Testing

FAST AND LS


F00
74
LS
F240
LS244
LS3
FAST
LS
LOGIC SPEED

DESIGN CONSIDERATIONS

SELECTING TTL LOGIC. TTL Families may be mixed in a system for optimum performance. For instance, in new designs, ALS would commonly be used in non-critical speed paths to minimize power consumption while FAST™ TTL would be used in high speed paths. The ratio of ALS to FAST™ will depend on overall system design goals.

NOISE IMMUNITY. When mixing TTL families it is often desirable to know the guaranteed noise immunity for both LOW and HIGH logic levels. Table 3.1 lists the guaranteed logic levels for various TTL families and can be used to calculate noise margin. Table 3.2 specifies these noise margins for systems containing LS, S, ALS and/or FAST™ TTL. Note that Table 3.2 represents "worst case" limits and assumes a maximum power supply and temperature variation across the IC's which are interconnected, as well as maximum rated load. Increased noise immunity can be achieved by designing with decreased maximum allowable operating ranges.

TABLE 3.1
Worst Case TTL Logic Levels

Electrical Characteristics

		Military (—55 to ±125°C)				Commercial (0 to 70°C)				
	TTL Families	V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	UNITS
TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
HTTL	High Speed TTL 54H/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LPTTL	Low Power TTL 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
STTL	Schottky TTL 54S/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LSTTL	Low Power Schottky TTL 54LS/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V
ALS TTL (5% V_{CC})	Advanced LS TTL, 54ALS/74ALS					0.8	2.0	0.5	2.75	V
(10% V_{CC})		0.8	2.0	0.4	2.5	0.8	2.0	0.5	2.5	V
FAST TTL(5% V_{CC})	Advanced S TTL, 54F/74F					0.8	2.0	0.5	2.7	V
(10% V_{CC})		0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.5	V

V_{OL} and V_{OH} are the voltages generated at the output V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

TABLE 3.2a
LOW Level Noise Margins (Military)

To					
From	LS	S	ALS	FAST	Units
LS	300	400	400	400	mV
S	200	300	300	300	mV
ALS	300	400	400	400	mV
FAST™	200	300	300	300	mV

From "V_{OL}" to "V_{IL}"

TABLE 3.2b
HIGH Level Noise Margins (Military)

To					
From	LS	S	ALS	FAST	Units
LS	500	500	500	500	mV
S	500	500	500	500	mV
ALS	500	500	500	500	mV
FAST™	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

TABLE 3.2c
LOW Level Noise Margins (Commercial)

To					
From	LS	S	ALS	FAST	Units
LS	300	300	300	300	mV
S	300	300	300	300	mV
ALS	300	300	300	300	mV
FAST™	300	300	300	300	mV

From "V_{OL}" to "V_{IL}"

TABLE 3.2d
HIGH Level Noise Margins (Commercial)

To					
From	LS	S	ALS	FAST	Units
LS	700	700	700	700	mV
S	700	700	700	700	mV
ALS (5% V_{CC})	750	750	750	750	mV
FAST (5% V_{CC})	700	700	700	700	mV
ALS (10% V_{CC})	500	500	500	500	mV
FAST (10% V_{CC})	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

POWER CONSUMPTION. With the exception of ECL, all logic families exhibit increased power consumption at high frequencies. Figure 3.1 shows this characteristic for common logic families. This figure refers to an average single gate dissipation, care must be taken when switching multiple gates at high frequencies to assure that their combined dissipation does not exceed package and/or device capabilities. As indicated, TTL devices are more efficient at high frequencies than CMOS.

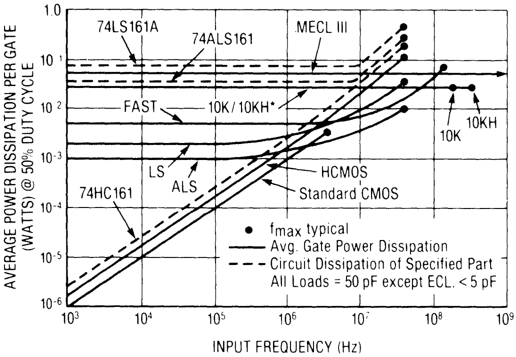


FIGURE 3-1
AVERAGE GATE POWER DISSIPATION
versus FREQUENCY

FAN-IN AND FAN-OUT. In order to simplify designing with Motorola TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA in the HIGH state (Logic "1")
1 TTL Unit Load (U.L.) = 1.6 mA in the LOW state (Logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES — INPUT LOAD

1. A 7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 74LS95B which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8\text{ mA}}{1.6\text{ mA}} \text{ or } 0.5\text{ U.L.} \quad \text{and an input HIGH load factor of} \quad \frac{40\,\mu\text{A}}{40\,\mu\text{A}} \text{ or } 1\text{ U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.4 mA and an I_{IH} of 20 μA, has an input LOW load factor of

$$\frac{0.4\text{ mA}}{1.6\text{ mA}} \text{ or } 0.25\text{ U.L.} \quad \text{an input HIGH load factor of} \quad \frac{20\,\mu\text{A}}{40\,\mu\text{A}} \text{ or } 0.5\text{ U.L.}$$

EXAMPLES — OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16\text{ mA}}{1.6\text{ mA}} = 10\text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800\,\mu\text{A}}{40\,\mu\text{A}} \text{ or } 20\text{ U.L.}$$

2. The output of the 74LS00 will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{8.0\text{ mA}}{1.6\text{ mA}}\text{ or 5 U.L.}$$

and the output HIGH drive factor is

$$\frac{400\ \mu\text{A}}{40\ \mu\text{A}}\text{ or 10 U.L.}$$

Relative load and drive factors for the basic TTL families are given in Table 3.3.

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74 ALS	0.5 U.L.	0.0625 U.L.	10 U.L.	5 U.L.
74 FAST	0.5 U.L.	0.375 U.L.	25 U.L.	12.5 U.L.

TABLE 3.3

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS. Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP
RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(\text{LOW}) \bullet 1.6\text{ mA}} \qquad R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(\text{HIGH}) \bullet 40\ \mu\text{A}}$$

where:

R_x = External Pull-up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads (U.L.) being Driven
$I_{OH} = I_{CEX}$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan-out Current of Driving Element
V_{OL} = Output LOW Voltage Level (0.5 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ \text{V} - 0.5\ \text{V}}{8\ \text{mA} - 1.6\ \text{mA}} = \frac{4.75\ \text{V}}{6.4\ \text{mA}} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ \text{V} - 2.4\ \text{V}}{4 \bullet 100\,\mu\text{A} + 2 \bullet 40\,\mu\text{A}} = \frac{2.35\ \text{V}}{0.48\ \text{mA}} = 4.9\ \text{k}\Omega$$

where:

N_1 = 4
N_2 (HIGH) = 4 • 0.5 U.L. = 2 U.L.
N_2 (LOW) = 4 • 0.25 U.L. = 1 U.L.
I_{OH} = 100 μA
I_{OL} = 8 mA
V_{OL} = 0.5 V
V_{OH} = 2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS. For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

3

1. Connect unused input to V_{CC}, LS and FAST™ TTL inputs have a breakdown voltage >7.0 V and require, therefore no series resistor.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: *Do not connect an unused LS or FAST™ input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.*

INPUT CAPACITANCE. As a rule of thumb, LS and FAST™ TTL inputs have an average capacitance of 5 pF for DIP packages. For an input that serves more than one internal function, each additional function adds approximately 1.5 pF.

LINE DRIVING — Because of its superior capacitive drive characteristics, TTL logic is often used in line driving applications which require various termination techniques to maintain signal integrity. Parameters associated with this application are listed in Table 3.4.

It is also often necessary to construct load lines to determine reflection waveforms in line driving applications. The input and output characteristics graphs of section 3 (Figs. 2-4, 2-7 and 2-8) can be very useful for this purpose.

OUTPUT RISE AND FALL TIMES provide important information in determining reflection waveforms and crosstalk coefficients. Typical rise and fall times are approximately 6.0 ns for LS and about 2.0 ns for FAST™ with a 50-pF load (measured 10–90%). Output rise and fall times become longer as capacitive load is increased.

INTERCONNECTION DELAYS. For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 100 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

(ALL MAXIMUM RATINGS)		LS		FAST		
Characteristic	Symbol	54LSxxx	74LSxxx	54Fxxx	74Fxxx	Units
Operating Voltage Range	V_{CC}	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	Vdc
Output Drive:	I_{OH}	−0.4	−0.4	−1.0	−1.0	mA
Standard Output	I_{OL}	4.0	8.0	20	20	mA
	I_{SC}	−20 to −100	−20 to −100	−60 to −150	−60 to −150	mA
Buffer Output	I_{OH}	−12	−15	−12	−15	mA
	I_{OL}	12	24	48	64	mA
	I_{SC}	−40 to −225	−40 to −225	−100 to −225	−100 to −225	mA

TABLE 3.4
OUTPUT CHARACTERISTICS FOR SCHOTTKY TTL LOGIC

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

	LS	FAST
Storage Temperature	−65°C to +150°C	−65°C to + 150°C
Temperature (Ambient) Under Bias	−55°C to +125°C	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V	−0.5 V to +7.0 V
*Input Voltage (dc) Diode Inputs	−0.5 V to 15 V	−0.5 V to 7.0 V
*Input Current (dc)	−30 mA to +5.0 mA	−30 mA to +5.0 mA
Voltage Applied to Open Collector Outputs (Output HIGH)	−0.5 V to +10 V	−0.5 V to +5.5 V
High Level Voltage Applied to Disabled 3-State Output	5.5 V	5.5 V

*Either input voltage limit or input current limit is sufficient to protect the inputs — Circuits with 5.5 V maximum limits are listed below.

Device types having inputs limited to 5.5 V are as follows:

SN74LS242/243, SN74LS245 — Inputs connected to outputs.
SN74LS640/641/642/645 — Inputs connected to outputs.
SN74LS299/322A/323 — Certain Inputs.
SN74LS673/674 — Certain Inputs.
SN74LS151/251 — Multiplexer Inputs.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATABOOK

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC}	**Supply Current** — The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.
I_{IH}	**Input HIGH current** — The current flowing into an input when a specified HIGH voltage is applied.
I_{IL}	**Input LOW current** — The current flowing out of an input when a specified LOW voltage is applied.
I_{OH}	**Output HIGH current.** The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.
I_{OL}	**Output LOW current** — The current flowing into an output which is in the LOW state.
I_{OS}	**Output short-circuit current** — The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).
I_{OZH}	**Output off current HIGH** — The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	**Output off current LOW** — The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES — All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.,* −10 V is greater than −1.0 V).

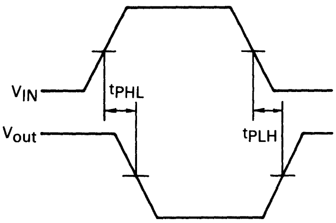
V_{CC}	**Supply voltage** — The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
$V_{IK(MAX)}$	**Input clamp diode voltage** — The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.
V_{IH}	**Input HIGH voltage** — The range of input voltages that represents a logic HIGH in the system.
$V_{IH(MIN)}$	**Minimum input HIGH voltage** — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.
V_{IL}	**Input LOW voltage** — The range of input voltages that represents a logic LOW in the system.
$V_{IL(MAX)}$	**Maximum input LOW voltage** — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.
$V_{OH(MIN)}$	**Output HIGH voltage** — The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.
$V_{OL(MAX)}$	**Output LOW voltage** — The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.
V_{T+}	**Positive-going threshold voltage** — The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.
V_{T-}	**Negative-going threshold voltage** — The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS AND WAVEFORMS

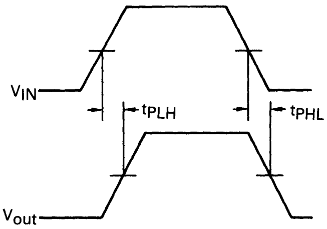
t_{PLH} **Propagation delay LOW-TO-HIGH:**
The time delay from when the input is 1.3 V (1.5 for FAST) to when the output reaches 1.3 V (1.5 for FAST), while the output changes to a logic HIGH.

t_{PHL} **Propagation delay HIGH-TO-LOW:**
The time delay from when the input is 1.3 V (1.5 for FAST) to when the output reaches 1.3 V (1.5 for FAST), while the output changes to a logic LOW.

For Inverting Function

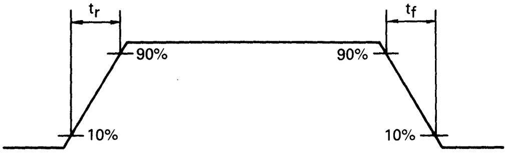

V_{IN}
t_{PHL}
V_{out}
t_{PLH}

For Non Inverting


V_{IN}
t_{PLH}
t_{PHL}
V_{out}

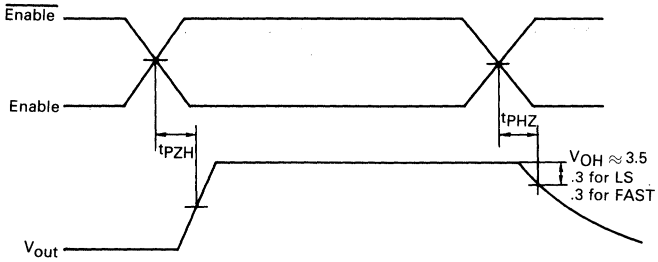
t_r **Waveform Rise Time:**
LOW to HIGH logic transition time, measured from the 10% to 90% points of the waveform.

t_f **Waveform Fall Time:**
HIGH to LOW logic transition time, measured the 90% to the 10% points of the waveform.


t_r
t_f
90%
90%
10%
10%

t_{PHZ} **Output disable time: HIGH to Z**
The time delay between the specified amplitude point on the enable input and when the output falls 0.3 V (0.3 V for FAST) from the steady-state HIGH level.

t_{PZH} **Output enable time: Z to HIGH**
The time delay between the specified amplitude points on the enable input and the output, when the output is going from a disabled state to a logic HIGH state.

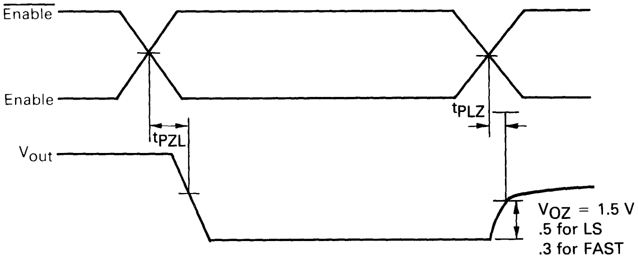

$\overline{\text{Enable}}$
Enable
t_{PZH}
t_{PHZ}
$V_{OH} \approx 3.5$
.3 for LS
.3 for FAST
V_{out}

t_{PLZ} **Output disable time: LOW to Z**

The time delay between the specified amplitude point on the enable input and when the output falls 0.3 V (0.3 V for FAST) from the steady-state LOW level.

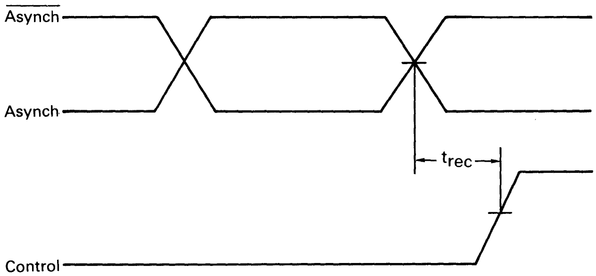
t_{PZL} **Output enable time: Z to LOW**

The time delay between the specified amplitude points on the enable input and the output when the output is going from a disabled state to a logic LOW state.


$\overline{\text{Enable}}$
Enable
V_{out}
t_{PZL}
t_{PLZ}
V_{OZ} = 1.5 V
.5 for LS
.3 for FAST

t_{rec} **Recovery time**

Time required between an asynchronous signal (SET, RESET, CLEAR or PARALLEL load) and the active edge of a synchronous control signal, to insure that the device will properly respond to the synchronous signal.

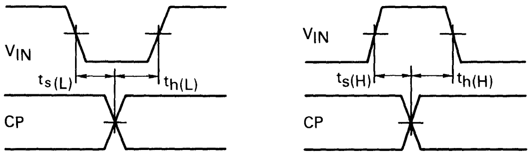

$\overline{\text{Asynch}}$
Asynch
t_{rec}
Control

t_h **Hold Time**

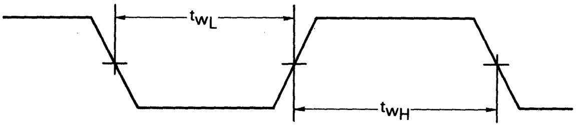
The interval of time from the active edge of the control signal (usually the clock) to when the data to be recognized is no longer required to ensure proper interpretation of the data. A negative hold time indicates that the data may be removed at some time prior to the active edge of the control signal.

t_s **Setup time**

The interval of time during which the data to be recognized is required to remain constant prior to the active edge of the control signal to ensure proper data recognition.


V_{IN}
$t_{s(L)}$
$t_{h(L)}$
CP
V_{IN}
$t_{s(H)}$
$t_{h(H)}$
CP

t_W or t_{PW}	**Pulse width** The time between the specified amplitude points (1.3 V for LS and 1.5 V for FAST™) on the leading and trailing edges of a pulse.



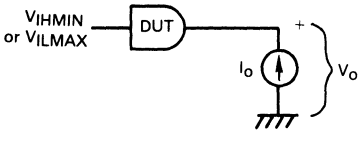
f_{MAX}	**Toggle frequency/operating frequency** The maximum rate at which clock pulses meeting the clock requirements *(i.e.,* t_{WH}, t_{WL}, and t_r, t_f) may be applied to a sequential circuit. Above this frequency the device may cease to function.
f_{MAX}min	**Guaranteed maximum clock frequency** The lowest possible value for f_{MAX}.

TESTING

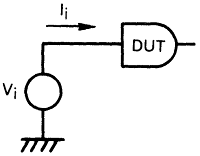
DC TEST CIRCUITS

The following test circuits and forcing functions represent Motorola's typical DC test procedures

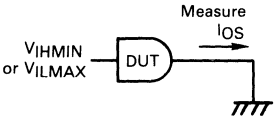
V_{OH} AND V_{OL} TESTS
Force I_{OHMAX} or I_{OLMAX}
Measure V_{OH} or V_{OL}


V_{IHMIN} or V_{ILMAX}
DUT
+
I_o
V_o

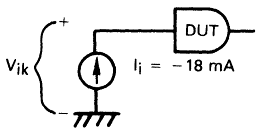
I_{IHH}, I_{IH} AND I_{IL} TESTS
Force 7.0, 5.5, 2.7, or 0.4 V
Measure I_{IHH}, I_{IH}, or I_{IL}



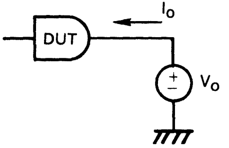
I_{OS} TEST


Measure I_{OS}
V_{IHMIN} or V_{ILMAX}
DUT

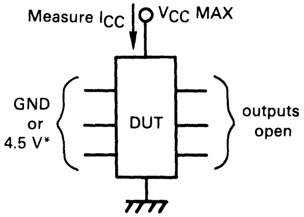
V_{IK} TEST
Force I_i
Measure V_{IK}


+
V_{ik}
−
DUT
I_i = −18 mA

I_{OH}, I_{OZH}, and I_{OZL} TESTS
Force 5.5, 2.4, or 0.4 V
Measure I_O



I_{CC} TEST


Measure I_{CC}
V_{CC} MAX
GND or 4.5 V*
DUT
outputs open

*Unless otherwise indicated, input conditions are selected to produce a worst case condition.

AC TEST CIRCUITS The following test circuits and conditions represent Motorola's typical test procedures. AC waveforms and terminology can be found on pages 3-8 to 3-10.

Proper testing requires that care be taken in the construction of AC test fixtures. This is especially true of FAST™ TTL.

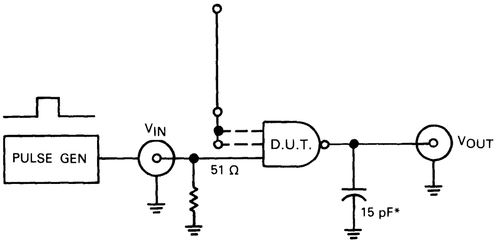
Maintaining a 50 Ω environment on the ac test fixture, as well as the use of multilayer boards with internal V_{CC} and ground planes is highly recommended for FAST™ TTL. Bypassing with both electrolytic and high quality RF type capacitors should be provided on the board. Lead lengths for all components should be kept as short as possible (Motorola uses and recommends chip capacitors and resistors for ac test fixtures). Following these rules will result in cleaner waveforms as well as better correlation between Motorola and the FAST™ TTL consumer.

FUNCTIONAL TESTING OF TTL IN A NOISY ENVIRONMENT

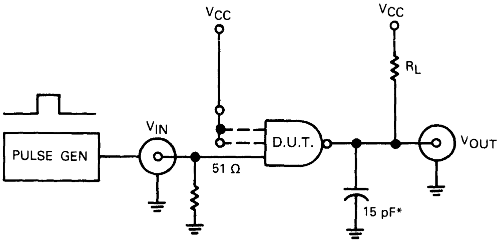
Testing noise (noise generated by the test system itself and noise generated by TTL devices under test interacting with the test system) adds to, or subtracts from the threshold voltage applied to the TTL device under test. For this reason Motorola does not recommend functional testing of TTL devices using threshold levels of 0.8 V and 2.0 V. Instead, good TTL testing techniques call for hard levels of less than 0.5 V VIL and greater than 2.4 V VIH to be applied for functional testing. Input threshold voltages should be tested separately, and only (for noise reasons above) after setting the device state with a hard level.

LS TEST CIRCUITS

Test Circuit for Standard Output Devices

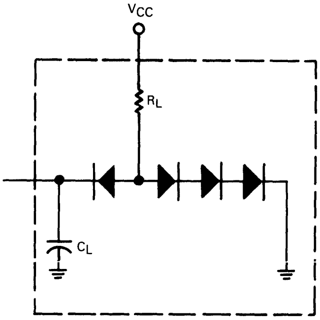


Test Circuit for Open Collector Output Devices



*includes all probe and jig capacitance

Optional LS Load (Guaranteed—Not Tested)

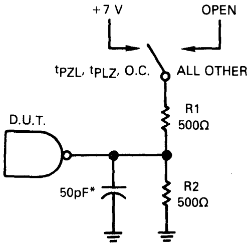


PULSE GENERATOR SETTINGS (UNLESS OTHERWISE SPECIFIED)

	LS	FAST
Frequency =	1MHz	1MHz
Duty Cycle =	50%	50%
1 TLH (t_r) =	6 ns (15)*	2.5 ns
1 THL (t_f) =	6 ns (15)*	2.5 ns
Amplitude =	0 to 3 V	0 to 3 V

*The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

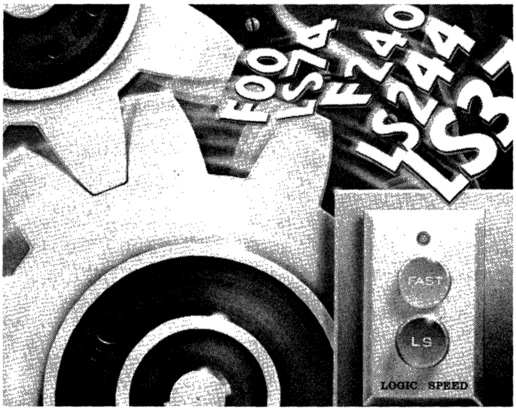
FAST TEST CIRCUITS



*includes all probe and jig capacitance

FAST Data Sheets

FAST AND LS


F00
LS74
F240
LS244
LS3
FAST
LS
LOGIC SPEED

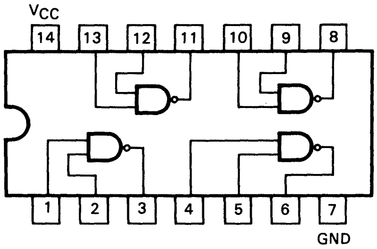
MOTOROLA

MC54F/74F00

QUAD 2-INPUT NAND GATE

FAST™ SCHOTTKY TTL

QUAD 2-INPUT NAND GATE



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.8	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				10.2	mA	V_{CC} = MAX, V_{IN} = Open	

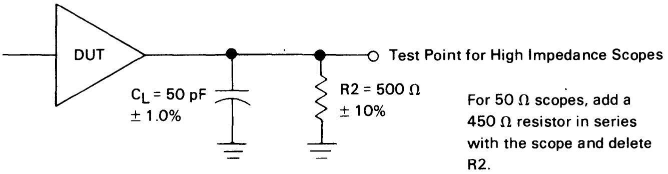
NOTES:

1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50\ pF$		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50\ pF$		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

AC TEST CIRCUIT


DUT
Test Point for High Impedance Scopes
$C_L = 50$ pF
± 1.0%
R2 = 500 Ω
± 10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

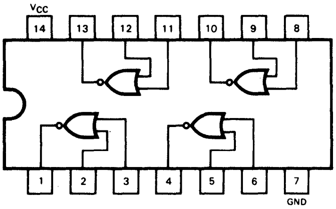
MOTOROLA

MC54F/74F02

QUAD 2-INPUT NOR GATE

QUAD 2-INPUT NOR GATE

FAST™ SCHOTTKY TTL



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

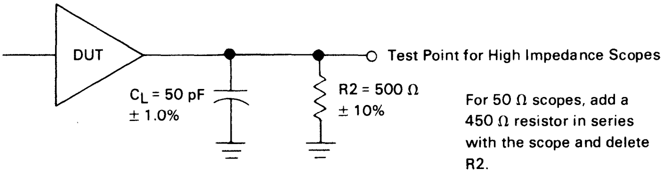
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				5.6	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				13	mA	V_{CC} = MAX, V_{IN} = Note 3	

NOTES:
1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.
3. Measured with one input high, one input low for each gate.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.5	5.5	2.5	7.5	2.5	6.5	ns
t_{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

AC TEST CIRCUIT


DUT
Test Point for High Impedance Scopes
C_L = 50 pF
± 1.0%
R2 = 500 Ω
± 10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

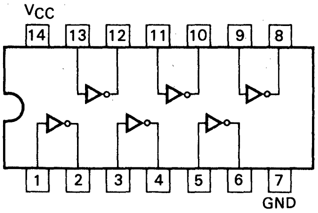
MOTOROLA

MC54F/74F04

HEX INVERTER

FAST™ SCHOTTKY TTL

HEX INVERTER



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

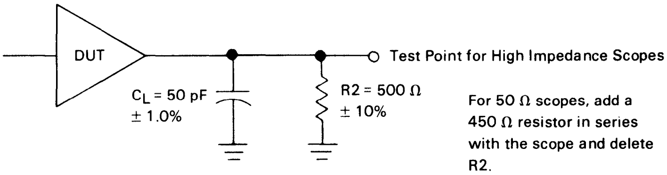
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				4.2	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				15.3	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

AC TEST CIRCUIT


DUT
Test Point for High Impedance Scopes
C_L = 50 pF
± 1.0%
R2 = 500 Ω
± 10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

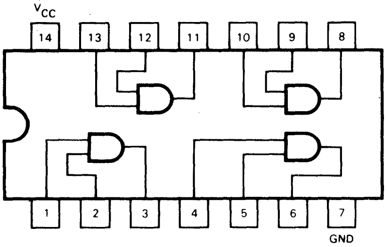
Fig. 1

MC54F/74F08

QUAD 2-INPUT AND GATE

FAST™ SCHOTTKY TTL

QUAD 2-INPUT AND GATE



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				8.3	mA	V_{CC} = MAX, V_{IN} = Open	
	Total, Output LOW				12.9	mA	V_{CC} = MAX, V_{IN} = GND	

NOTES:
1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	3.0	5.6	2.5	7.5	3.0	6.6	ns
t_{PHL}	Propagation Delay	2.5	5.3	2.0	7.5	2.5	6.3	ns

AC TEST CIRCUIT

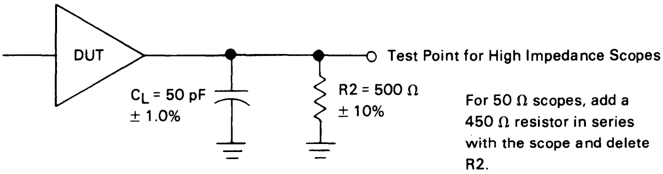

DUT
Test Point for High Impedance Scopes
$C_L = 50$ pF
± 1.0%
R2 = 500 Ω
± 10%
For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete
R2.

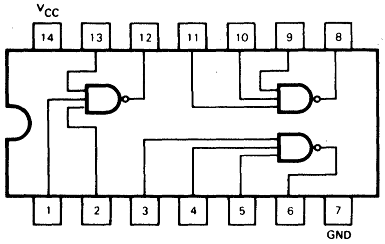
Fig. 1

MOTOROLA

MC54F/74F10

TRIPLE 3-INPUT NAND GATE

FAST™ SCHOTTKY TTL



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

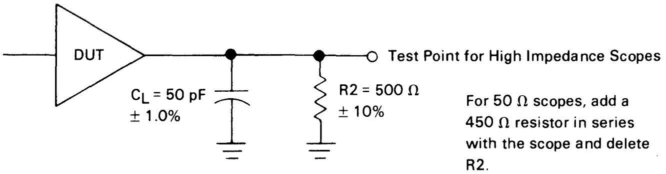
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.1	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				7.7	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

AC TEST CIRCUIT


DUT
Test Point for High Impedance Scopes
$C_L = 50$ pF ± 1.0%
R2 = 500 Ω ± 10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

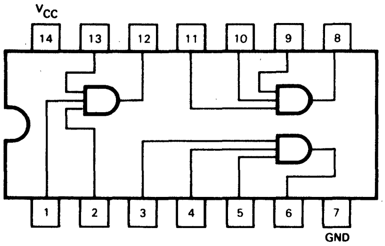
Fig. 1

MOTOROLA

MC54F/74F11

TRIPLE 3-INPUT AND GATE

FAST™ SCHOTTKY TTL



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				6.2	mA	V_{CC} = MAX, V_{IN} = Open	
	Total, Output LOW				9.7	mA	V_{CC} = MAX, V_{IN} = GND	

NOTES:

1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	3.0	5.6	2.5	7.5	3.0	6.6	ns
t_{PHL}	Propagation Delay	2.5	5.5	2.0	7.5	2.5	6.5	ns

AC TEST CIRCUIT

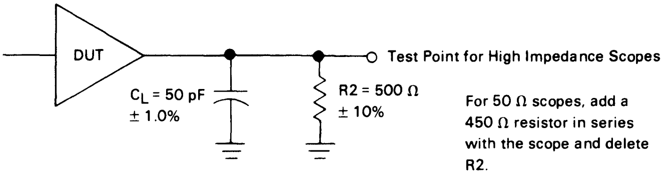

DUT
Test Point for High Impedance Scopes
C_L = 50 pF
± 1.0%
R2 = 500 Ω
± 10%
For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete
R2.

Fig. 1

MOTOROLA

MC54F/74F13
MC54F/74F14

SCHMITT TRIGGERS DUAL 4-INPUT NAND/HEX INVERTER

FAST™ SCHOTTKY TTL

Advance Information

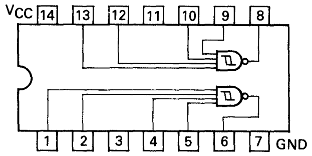
SCHMITT TRIGGERS/HEX INVERTERS

DESCRIPTION — The MC54F/74F13 and MC54F/74F14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

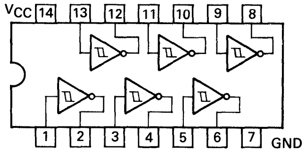
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAMS

MC54F/74F13



MC54F/74F14



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{T+}	Positive-Going Threshold Voltage		1.5		2.0	V	$V_{CC} = 5.0$ V	
V_{T-}	Negative-Going Threshold Voltage		0.7		1.1	V	$V_{CC} = 5.0$ V	
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	$V_{CC} = 5.0$ V	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$
		74	2.7			V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$
V_{OL}	Output LOW Voltage				0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T+}$	
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T-}$	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, $V_{IN} = 0.5$ V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, $V_{OUT} = 0$ V	
I_{CCH}	Power Supply Current Total, Output HIGH	F13		4.5	8.5	mA	V_{CC} = MAX	
		F14		13	22			
I_{CCL}	Power Supply Current Total, Output LOW	F13		7.0	10			
		F14		23	32			

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC CHARACTERISTICS (C_L = 50 pF)

SYMBOL	PARAMETER		54/74F T_A = +25°C V_{CC} = +5.0 V		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10%		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10%		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	F13	3.5	7.0	3.5	9.0	3.5	8.0	ns
t_{PHL}	Propagation Delay	F13	3.0	8.0	3.0	9.5	3.0	8.5	ns
t_{PLH}	Propagation Delay	F14	3.5	7.0	3.5	9.0	3.5	8.0	ns
t_{PHL}	Propagation Delay	F14	3.0	6.5	3.0	8.0	3.0	7.0	ns

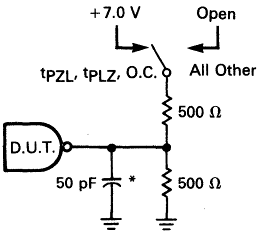
FUNCTION TABLE F13

Inputs				Outputs
A	B	C	D	O
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

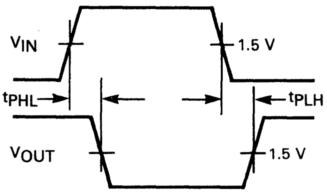
FUNCTION TABLE F14

Input	Output
A	O
L	H
H	L


+7.0 V
Open
t_{PZL}, t_{PLZ}, O.C.
All Other
500 Ω
D.U.T.
50 pF
*
500 Ω

*Includes Jig and Probe Capacitance

WAVEFORM FOR INVERTING FUNCTIONS


V_{IN}
1.5 V
t_{PHL}
t_{PLH}
V_{OUT}
1.5 V

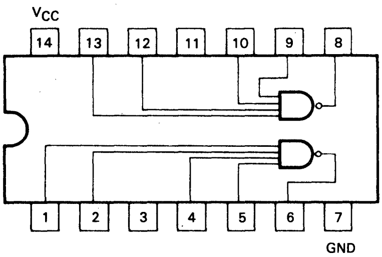
MOTOROLA

MC54F/74F20

DUAL 4-INPUT NAND GATE

DUAL 4-INPUT NAND GATE

FAST™ SCHOTTKY TTL



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				1.4	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				5.1	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t_{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

AC TEST CIRCUIT

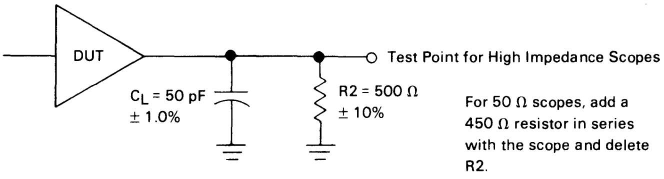

DUT
Test Point for High Impedance Scopes
$C_L = 50$ pF
± 1.0%
R2 = 500 Ω
± 10%
For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

MC54F/74F21

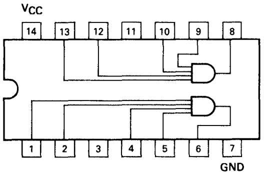
DUAL 4-INPUT AND GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

CONNECTION DIAGRAM



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

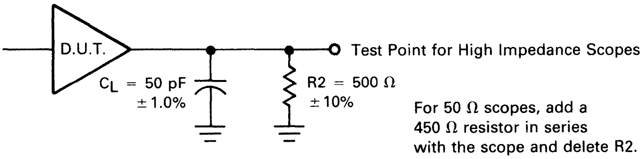
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −1.0 mA	V_{CC} = 4.5 V
		74	2.7			V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				4.1	mA	V_{CC} = MAX, V_{IN} = Open	
	Total, Output LOW				6.4	mA	V_{CC} = MAX, V_{IN} = GND	

AC CHARACTERISTICS

SYMBOL	PARAMETER	54F/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		$T_A = 0°C$ to $70°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.0	5.6	2.0	7.5	2.0	6.6	ns
t_{PHL}	Propagation Delay	2.5	5.3	2.0	7.5	2.5	6.3	ns

AC TEST CIRCUIT


D.U.T.
Test Point for High Impedance Scopes
C_L = 50 pF
±1.0%
R2 = 500 Ω
±10%

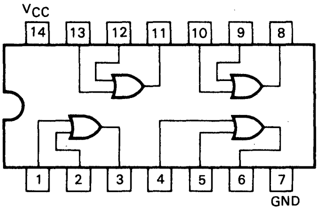
For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete R2.

FIGURE 1

MOTOROLA

MC54F/74F32

QUAD 2-INPUT OR GATE



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

QUAD 2-INPUT OR GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH CUrrent				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				9.2	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				15.5	mA	V_{CC} = MAX, V_{IN} = 4.5 V	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	3.0	5.6	3.0	7.5	3.0	6.6	ns
t_{PHL}	Propagation Delay	3.0	5.3	2.5	7.5	3.0	6.3	ns

AC TEST CIRCUIT

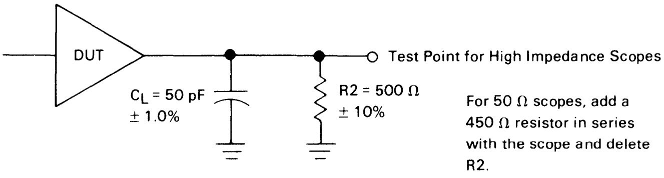

DUT
C_L = 50 pF
± 1.0%
R2 = 500 Ω
± 10%
Test Point for High Impedance Scopes
For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete
R2.

Fig. 1

MOTOROLA

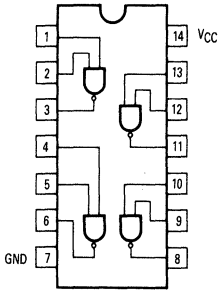
Advance Information

Quad 2-Input NAND Buffer

MC74F37

QUAD 2-INPUT
NAND BUFFER
FAST™ SCHOTTKY TTL

CONNECTION DIAGRAM



J SUFFIX — CASE 632-08 (CERAMIC)
N SUFFIX — CASE 646-06 (PLASTIC)
D SUFFIX — CASE 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−15	mA
I_{OL}	Output Current — Low	74			64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

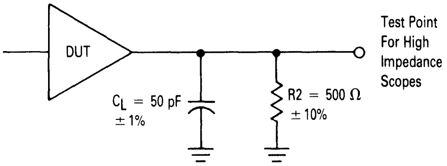
			Limits					
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Units**	**Test Conditions**	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	74	2			V	I_{OH} = −15 mA	V_{CC} = 4.5
		74	2.4			V	I_{OH} = −1 mA	
		74	2.7			V	I_{OH} = −1 mA	V_{CC} = 4.75
V_{OL}	Output LOW Voltage				0.55	V	I_{OL} = 64 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	Input LOW Current				−1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−100		−225	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				6	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				33	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC CHARACTERISTICS

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5 V C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5 V ±10% C_L = 50 pF		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	5.5	1.5	6.5	ns
t_{PHL}	Propagation Delay	1	4.5	1	5	ns


DUT
C_L = 50 pF ± 1%
R2 = 500 Ω ± 10%
Test Point For High Impedance Scopes

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Figure 1. AC Test Circuit

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

MOTOROLA

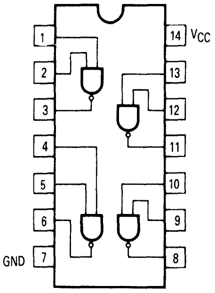
Advance Information

Quad 2-Input NAND Buffer, Open Collector

MC74F38

**QUAD 2-INPUT
NAND BUFFER,
OPEN COLLECTOR
FAST™ SCHOTTKY TTL**

CONNECTION DIAGRAM



J SUFFIX — CASE 632-08 (CERAMIC)
N SUFFIX — CASE 646-06 (PLASTIC)
D SUFFIX — CASE 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OL}	Output Current — Low	74			64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

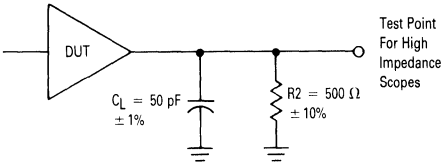
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
V_{IH}	Input HIGH Voltage	2			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OL}	Output LOW Voltage			0.55	V	I_{OL} = 64 mA V_{CC} = MIN
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
				0.1	mA	V_{CC} = MAX, V_{IN} = 7 V
I_{IL}	Input LOW Current			−1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V
I_{OH}	Output HIGH Current			250	µA	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX
I_{CC}	Power Supply Current Total, Output HIGH			7	mA	V_{CC} = MAX, V_{IN} = GND
	Total, Output LOW			30	mA	V_{CC} = MAX, V_{IN} = Open

NOTES: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC CHARACTERISTICS

		74F $T_A = +25°C$ $V_{CC} = +5\ V$ $C_L = 50\ pF$		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PLH}	Propagation Delay	7.5	12.5	7.5	13	ns
t_{PHL}	Propagation Delay	1	5	1	5.5	ns


DUT
$C_L = 50\ pF \pm 1\%$
$R2 = 500\ \Omega \pm 10\%$
Test Point For High Impedance Scopes

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Figure 1. AC Test Circuit

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

MOTOROLA

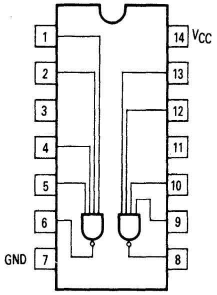
MC74F40

Advance Information

Dual 4-Input NAND Buffer

DUAL 4-INPUT
NAND BUFFER
FAST™ SCHOTTKY TTL

CONNECTION DIAGRAM



J SUFFIX — CASE 632-08 (CERAMIC)
N SUFFIX — CASE 646-06 (PLASTIC)
D SUFFIX — CASE 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−15	mA
I_{OL}	Output Current — Low	74			64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

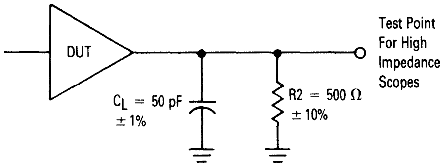
			Limits					
Symbol	Parameter		Min	Typ	Max	Units	Test Conditions	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	74	2			V	$I_{OH} = -15$ mA	$V_{CC} = 4.5$
		74	2.4			V	$I_{OH} = -1$ mA	
		74	2.7			V	$I_{OH} = -1$ mA	$V_{CC} = 4.75$
V_{OL}	Output LOW Voltage				0.55	V	$I_{OL} = 64$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7$ V	
I_{IL}	Input LOW Current				−1.2	mA	V_{CC} = MAX, $V_{IN} = 0.5$ V	
I_{OS}	Output Short Circuit Current (Note 2)		−100		−225	mA	V_{CC} = MAX, $V_{OUT} = 0$ V	
I_{CC}	Power Supply Current Total, Output HIGH				4	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				17	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC CHARACTERISTICS

		74F T_A = +25°C V_{CC} = +5 V C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5 V ±10% C_L = 50 pF		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PLH}	Propagation Delay	1.5	6	1.5	7	ns
t_{PHL}	Propagation Delay	1	5	1	5.5	ns


DUT
Test Point For High Impedance Scopes
C_L = 50 pF ±1%
R2 = 500 Ω ±10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Figure 1. AC Test Circuit

FUNCTION TABLE

INPUTS				OUTPUT
A	**B**	**C**	**D**	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	X	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

MOTOROLA

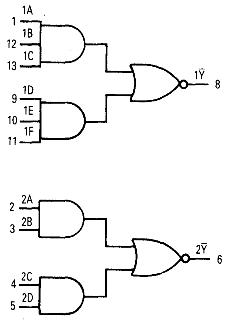
MC54F/74F51

Advance Information

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate

FAST™ Schottky TTL

LOGIC SYMBOL

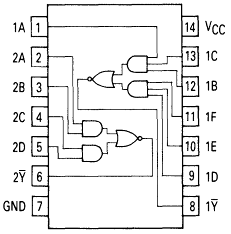

1A
1
1B
12
1C
13
1D
9
1E
10
1F
11
$1\overline{Y}$
8
2A
2
2B
3
2C
4
2D
5
$2\overline{Y}$
6

FUNCTIONAL TABLES

For 3-Input Gates							For 2-Input Gates				
Inputs						Output	Inputs				Output
A	B	C	D	E	F	$1\overline{Y}$	A	B	C	D	$2\overline{Y}$
H	H	H	X	X	X	L	H	H	X	X	L
X	X	X	H	H	H	L	X	X	H	H	L
All other combinations						H	All other combinations				H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

CONNECTION DIAGRAM


1A 1
2A 2
2B 3
2C 4
2D 5
$2\overline{Y}$ 6
GND 7
14 V_{CC}
13 1C
12 1B
11 1F
10 1E
9 1D
8 $1\overline{Y}$

J SUFFIX — CASE 632-08 (CERAMIC)
N SUFFIX — CASE 646-06 (PLASTIC)
D SUFFIX — CASE 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

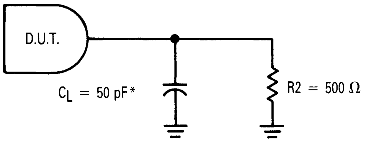
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −1 mA	V_{CC} = 4.5 V
		74	2.7			V	I_{OH} = −1 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Total Supply Current	I_{CCH}		1.8	3	mA	V_{IN} = GND	V_{CC} = MAX
		I_{CCL}		5.5	7.5		V_{IN} = 4.5 V	

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

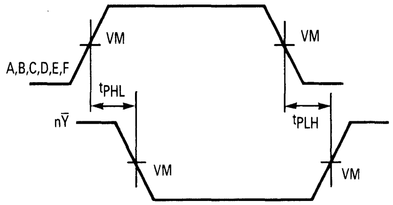
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Units
		T_A = 25°C V_{CC} = +5 V C_L = 50 pF			T_A = −55°C to +125°C V_{CC} = 5 V ±10% C_L = 50 pF		T_A = 0°C to +70°C V_{CC} = 5 V ±10% C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2		5.5	1.5	7.5	1.5	6.5	ns
t_{PHL}	A, B, C, D, E, F, to n$\overline{Y}$	1		4	1	5.5	1	4.5	


D.U.T.
C_L = 50 pF*
R2 = 500 Ω

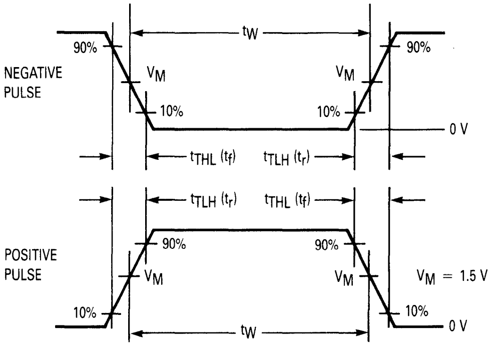
AC Test Circuit

* = INCLUDES ALL PROBE AND JIG CAPACITANCE.


A,B,C,D,E,F
VM
VM
t_{PHL}
t_{PLH}
n$\overline{Y}$
VM
VM

AC Waveform

NOTE: FOR ALL WAVEFORMS, VM = 1.5 V.
PROPAGATION DELAY INPUT TO OUTPUT


NEGATIVE PULSE
t_W
90%
90%
V_M
V_M
10%
10%
0 V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
POSITIVE PULSE
90%
90%
V_M
V_M
V_M = 1.5 V
10%
10%
0 V
t_W

Input Pulse Definition

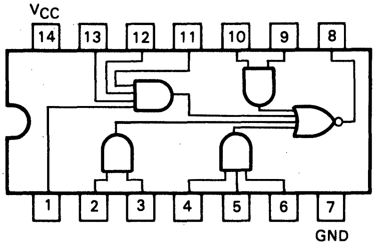
MOTOROLA

MC54F/74F64

4-2-3-2-INPUT AND-OR-INVERT GATE

FAST™ SCHOTTKY TTL

4-2-3-2-INPUT AND-OR-INVERT GATE



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					0.1	mA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				2.8	mA	V_{IN} = GND	V_{CC} = MAX
	Total, Output LOW				4.7	mA	V_{IN} = *	

NOTES:
1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

* I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.5	6.5	2.5	8.5	2.5	7.5	ns
t_{PHL}	Propagation Delay	1.5	4.5	1.5	6.5	1.5	5.5	ns

AC TEST CIRCUIT

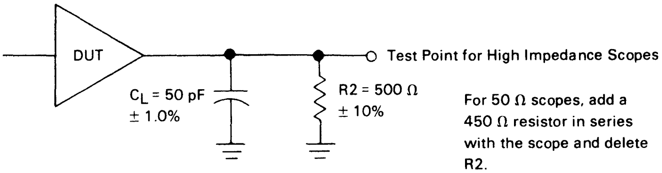

DUT
C_L = 50 pF
± 1.0%
R2 = 500 Ω
± 10%
Test Point for High Impedance Scopes
For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

MC54F/74F74

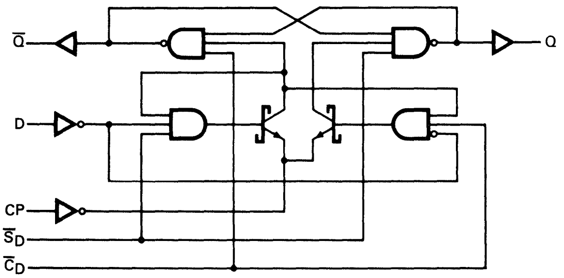
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The MC54F/74F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

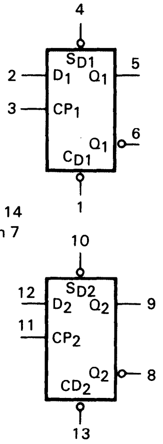
LOGIC DIAGRAM



$\overline{Q}$
Q
D
CP
$\overline{S}_D$
$\overline{C}_D$

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

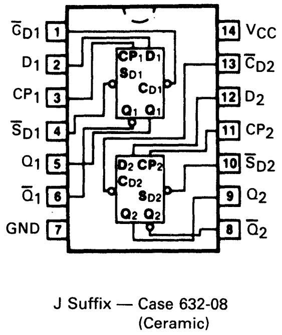
LOGIC SYMBOL



4
S_{D1}
2
D_1
Q_1
5
3
CP_1
$\overline{Q}_1$
6
C_{D1}
1
10
S_{D2}
12
D_2
Q_2
9
11
CP_2
$\overline{Q}_2$
8
C_{D2}
13

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM



$\overline{C}_{D1}$ 1
D_1 2
CP_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
GND 7
14 V_{CC}
13 $\overline{C}_{D2}$
12 D_2
11 CP_2
10 $\overline{S}_{D2}$
9 Q_2
8 $\overline{Q}_2$
CP_1 D_1
S_{D1}
C_{D1}
Q_1 $\overline{Q}_1$
D_2 CP_2
C_{D2}
S_{D2}
Q_2 $\overline{Q}_2$

J Suffix — Case 632-08
(Ceramic)
N Suffix — Case 646-06
(Plastic)
D Suffix — Case 751A-02
(SOIC)

TRUTH TABLE
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Asynchronous Inputs:
LOW Input to $\overline{S}_D$ sets Q to HIGH level
LOW Input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are indepedent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
$t_n + 1$ = Bit time after clock pulse

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current (CP and D Inputs)				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				-1.8	mA		
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			10.5	16	mA	V_{CP} = 0 V	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100		100		100		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.8 4.4	6.8 8.0	3.8 4.4	8.5 10.5	3.8 4.4	7.8 9.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.5 3.5	6.1 9.0	3.2 3.5	8.0 11.5	2.5 3.5	7.1 10.5	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Set up Time, HIGH or LOW	2.0			3.0		2.0		ns
t_s (L)	D_n to CP_n	3.0			4.0		3.0		
t_h (H)	Hold Time, HIGH or LOW	1.0			2.0		1.0		
t_h (L)	D_n to CP_n	1.0			2.0		1.0		
t_w (H)	CP_n Pulse Width, HIGH	4.0			4.0		4.0		ns
t_w (L)	or LOW	5.0			6.0		5.0		
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0			4.0		4.0		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			3.0		2.0		ns

MOTOROLA

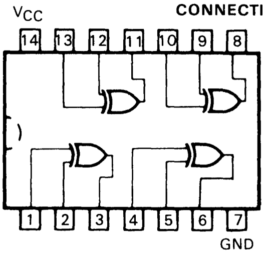
MC54F/74F86

QUAD 2-INPUT EXCLUSIVE-OR GATE

QUAD 2-INPUT EXCLUSIVE-OR GATE

FAST™ SCHOTTKY TTL

CONNECTION DIAGRAM



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			15	23	mA	1-Input HIGH 1-Input LOW	V_{CC} = MAX
				18	28		Inputs LOW	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V $\pm10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V $\pm10\%$ $C_L = 50$ pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	3.0	4.0	5.5	2.5	7.0	3.0	6.5	ns
t_{PHL}	(Other Input LOW)	3.0	4.2	5.5	3.0	7.0	3.0	6.5	
t_{PLH}	Propagation Delay	3.5	5.3	7.0	3.5	8.5	3.5	8.0	ns
t_{PHL}	(Other Input HIGH)	3.0	4.7	6.5	3.0	8.0	3.0	7.5	

MOTOROLA

MC54F/74F109

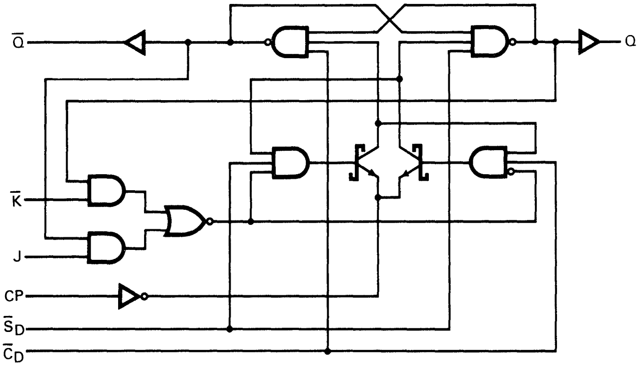
DUAL J$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL

DUAL J$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The MC54F/74F109 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{K}$ inputs together.

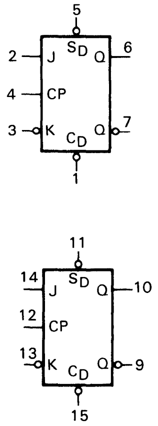
LOGIC DIAGRAM (one half shown)



$\overline{Q}$
Q
$\overline{K}$
J
CP
$\overline{S}_D$
$\overline{C}_D$

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

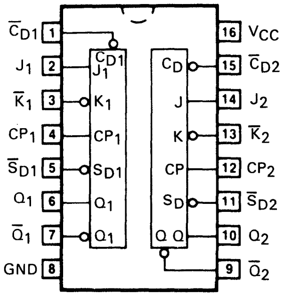
LOGIC SYMBOL



5
2
J
S_D
Q
6
4
CP
3
K
C_D
Q
7
1
11
14
J
S_D
Q
10
12
CP
13
K
C_D
Q
9
15

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



$\overline{C}_{D1}$ 1
J_1 2
$\overline{K}_1$ 3
CP_1 4
$\overline{S}_{D1}$ 5
Q_1 6
$\overline{Q}_1$ 7
GND 8
16 V_{CC}
15 $\overline{C}_{D2}$
14 J_2
13 $\overline{K}_2$
12 CP_2
11 $\overline{S}_{D2}$
10 Q_2
9 $\overline{Q}_2$
C_{D1}
J_1
K_1
CP_1
S_{D1}
Q_1
Q_1
C_D
J
K
CP
S_D
Q Q

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

TRUTH TABLE

INPUTS		OUTPUTS	
@ t_n		@ t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

Asynchronous Inputs:
LOW Input to $\overline{S}_D$ sets Q to HIGH level
LOW Input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are indepedent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse
$t_n + 1$ = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.50$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	µA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current (J, $\overline{K}$ and CP Inputs)				-0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				-1.8	mA		
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			11.7	17	mA	$V_{CP} = 0$ V	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			54F $T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		74F $T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100	125		70		90		MHz
t_{PLH}	Propagation Delay	3.8	5.3	7.0	3.8	9.0	3.8	8.0	ns
t_{PHL}	CP_n to Q_n or $\overline{Q}_n$	4.4	6.2	8.0	4.4	10.5	4.4	9.2	
t_{PLH}	Propagation Delay	2.5	5.2	7.0	2.5	9.0	2.5	8.0	ns
t_{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.5	7.0	9.0	3.5	11.5	3.5	10.5	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$			54F $T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$		74F $T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	1.0 1.0			1.0 1.0		1.0 1.0		
t_w (H) t_w (L)	CP_n Pulse Width, HIGH or LOW	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0			4.0		4.0		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			2.0		2.0		ns

MC54F/74F112

Product Preview

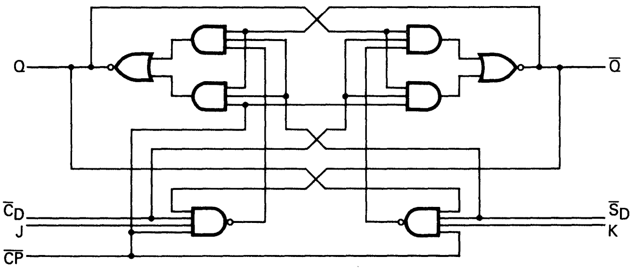
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — MC54F/74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

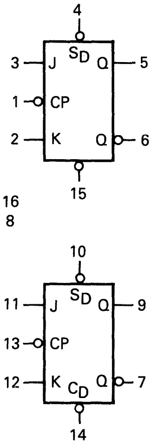
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL

LOGIC DIAGRAM (one half shown)


Q
$\overline{Q}$
$\overline{C}_D$
J
$\overline{CP}$
$\overline{S}_D$
K

LOGIC SYMBOL


4
3
J
S_D
Q
5
1
CP
2
K
Q
6
15
10
11
J
S_D
Q
9
13
CP
12
K
C_D
Q
7
14

V_{CC} = Pin 16
GND = Pin 8

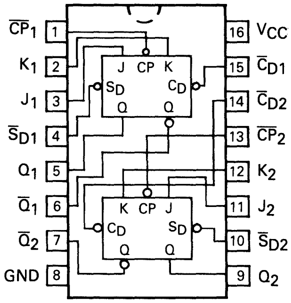
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM


$\overline{CP}_1$ 1
K_1 2
J_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
$\overline{Q}_2$ 7
GND 8
16 VCC
15 $\overline{C}_{D1}$
14 $\overline{C}_{D2}$
13 $\overline{CP}_2$
12 K_2
11 J_2
10 $\overline{S}_{D2}$
9 Q_2
J CP K
S_D
C_D
Q
Q
K CP J
C_D
S_D
Q
Q

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

*74F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					100	µA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current (J and K Inputs)				−0.6	mA	V_{CC} = MAX, $V_{IN} = 0.5$ V	
	($\overline{CP}$ Inputs)				−2.4	mA		
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				−3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, $V_{OUT} = 0$ V	
I_{CC}	Power Supply Current			12	19	mA	V_{CC} = MAX, $V_{CP} = 0$ V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

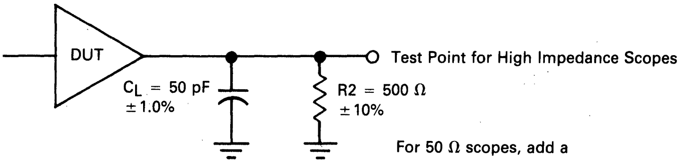
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	110						MHz
t_{PLH}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0	6.5			2.0	7.5	ns
t_{PHL}		2.0	6.5			2.0	7.5	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0	6.5			2.0	7.5	ns
t_{PHL}		2.0	6.5			2.0	7.5	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0					4.0 3.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0					0 0		
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width, HIGH or LOW	4.5 4.5					4.5 4.5		ns
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.5					4.5		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{CP}$	4.0					5.0		ns

AC TEST CIRCUIT



For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

Product Preview

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

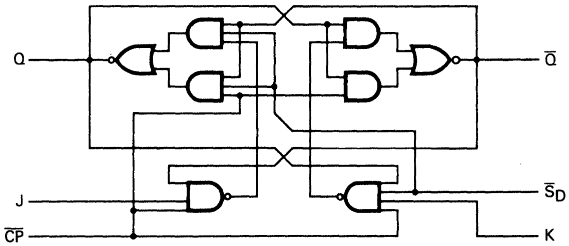
MC54F/74F113

DUAL JK EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL

DESCRIPTION — MC54F/74F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is in either state and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

LOGIC DIAGRAM (one half shown)



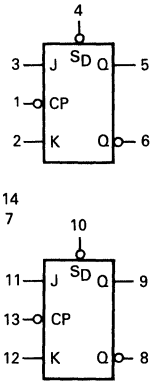
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

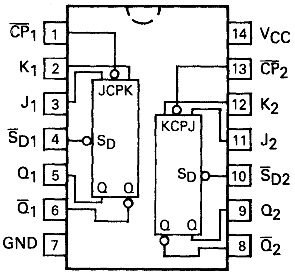
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL


4
3
J
SD
Q
5
1
CP
2
K
Q̄
6
10
11
J
SD
Q
9
13
CP
12
K
Q̄
8

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM


C̄P1
1
K1
2
J1
3
S̄D1
4
Q1
5
Q̄1
6
GND
7
14
VCC
13
C̄P2
12
K2
11
J2
10
S̄D2
9
Q2
8
Q̄2
JCPK
SD
Q
Q
KCPJ
SD
Q
Q

J Suffix — Case 632-08
(Ceramic)
N Suffix — Case 646-06
(Plastic)
D Suffix — Case 751A-02
(SOIC)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

*74F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					100	μA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current (J and K Inputs)				−0.6	mA	V_{CC} = MAX, $V_{IN} = 0.5$ V	
	($\overline{CP}$ Inputs)				−2.4	mA		
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				−3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, $V_{OUT} = 0$ V	
I_{CC}	Power Supply Current			12	19	mA	V_{CC} = MAX, $V_{CP} = 0$ V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

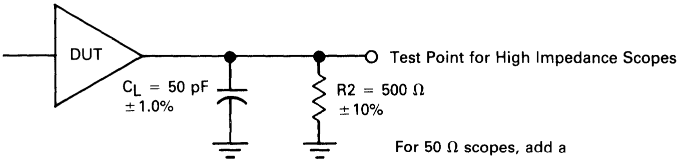
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	110						MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0 2.0	6.0 6.0			2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	6.5 6.5			2.0 2.0	7.5 7.5	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0					4.0 3.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0					0 0		
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width, HIGH or LOW	4.5 4.5					4.5 4.5		ns
t_w (L)	$\overline{S}_{Dn}$ Pulse Width LOW	4.5					4.5		ns
t_{rec}	Recovery Time $\overline{S}_{Dn}$ to $\overline{CP}$	4.0					5.0		ns

AC TEST CIRCUIT


DUT
Test Point for High Impedance Scopes
C_L = 50 pF ±1.0%
R2 = 500 Ω ±10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

MC54F/74F114

Product Preview

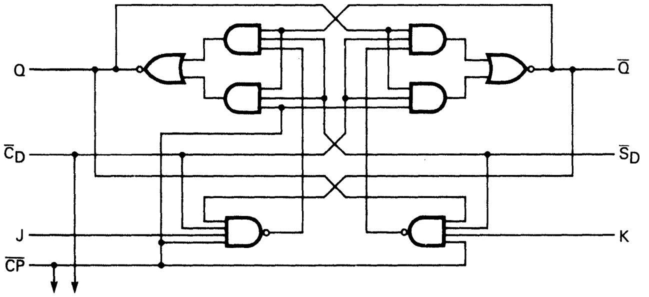
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP (WITH COMMON CLOCKS AND CLEARS)

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

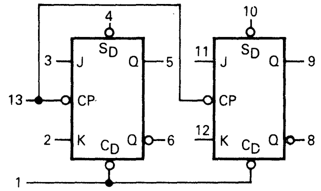
FAST™ SCHOTTKY TTL

DESCRIPTION — MC54F/74F114 contains two high-speed JK flip-flops with common clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

LOGIC DIAGRAM (one half shown)


Q
$\overline{Q}$
$\overline{C}_D$
$\overline{S}_D$
J
K
$\overline{CP}$

LOGIC SYMBOL


4
10
S_D
S_D
3
J
Q
5
11
J
Q
9
13
CP
CP
2
K
C_D
$\overline{Q}$
6
12
K
C_D
$\overline{Q}$
8
1

V_{CC} = Pin 14
GND = Pin 7

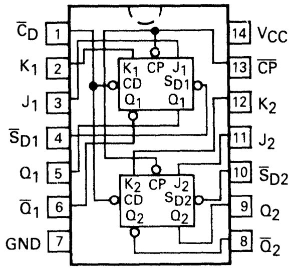
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CONNECTION DIAGRAM


$\overline{C}_D$ 1
K_1 2
J_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
GND 7
14 V_{CC}
13 $\overline{CP}$
12 K_2
11 J_2
10 $\overline{S}_{D2}$
9 Q_2
8 $\overline{Q}_2$
K_1 CP J_1
CD S_{D1}
Q_1 $\overline{Q}_1$
K_2 CP J_2
CD S_{D2}
Q_2 $\overline{Q}_2$

J Suffix — Case 632-08
(Ceramic)
N Suffix — Case 646-06
(Plastic)
D Suffix — Case 751A-02
(SOIC)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

*74F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					100	μA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current (J and K Inputs)				−0.6	mA	V_{CC} = MAX, $V_{IN} = 0.5$ V	
	($\overline{CP}$ Inputs)				−2.4	mA		
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				−3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, $V_{OUT} = 0$ V	
I_{CC}	Power Supply Current			12	19	mA	V_{CC} = MAX, $V_{CP} = 0$ V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

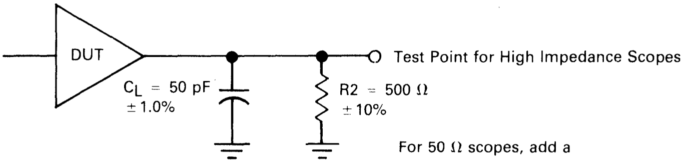
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50$ pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	110						MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	3.3 3.3	6.5 7.5			3.3 3.3	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	6.5 6.5			2.0 2.0	7.5 7.5	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		74F T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Set up Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0					4.0		ns
t_s (L)		3.0					3.0		
t_h (H)	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0					0		
t_h (L)		0					0		
t_w (H)	$\overline{CP}_n$ Pulse Width, HIGH or LOW	4.5					4.5		ns
t_w (L)		4.5					4.5		
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.5					4.5		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{CP}$	**4.0**					**5.0**		ns

AC TEST CIRCUIT



For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

MC54F/74F125
MC54F/74F126

QUAD BUFFERS, 3-STATE

FAST™ SCHOTTKY TTL

Advance Information

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			48 64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
		54	2.0			V	I_{OH} = −12 mA	V_{CC} = 4.5 V
		74	2.0			V	I_{OH} = −15 mA	
V_{OL}	Output LOW Voltage	54			0.55	V	I_{OL} = 48 mA	V_{CC} = MAX
		74			0.55	V	I_{OL} = 64 mA	
I_{OZH}	Output Off Current HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	V_{CC} = 0 V
I_{IL}	Input LOW Current				−20	μA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Drive Current Note 2		−100		−225	mA	V_{OUT} = GND	V_{CC} = MAX
I_{CC}	F125	I_{CCH}			24	mA	V_{CC} = MAX	
		I_{CCL}			40			
		I_{CCZ}			35			
	F126	I_{CCH}			30			
		I_{CCL}			48			
		I_{CCZ}			39			

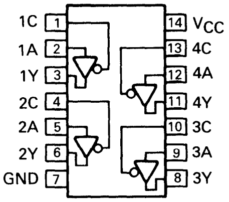
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

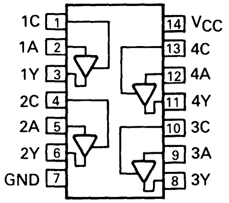
This document contains information on a new product. Specifications and information herein are subject to change without notice.

CONNECTION DIAGRAMS

F125



F126



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

TRUTH TABLES

F125

INPUTS		OUTPUT
$\overline{C}$	A	Y
L	L	L
L	H	H
H	X	(Z)

F126

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

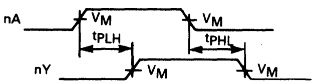
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

AC ELECTRICAL CHARACTERISTICS

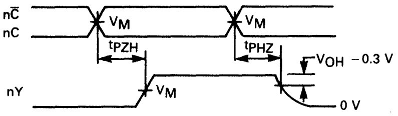
PARAMETER			TEST CONDITIONS	54/74F			54F		74F		UNIT
				$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$ $R_L = 500\ \Omega$			$T_A = 0$ to $70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50\ pF$ $R_L = 500\ \Omega$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0\ V \pm 10\%$ $C_L = 50\ pF$ $R_L = 500\ \Omega$		
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	F125	Waveform 1	1.5	4.0	6.0	1.5	7.5	1.5	6.5	ns
t_{PHL}	nA to nY			3.0	5.5	7.5	3.0	9.0	3.0	8.0	
t_{PZH}	Output enable time		Waveform 2	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t_{PZL}	to HIGH and LOW level		Waveform 3	3.0	6.0	8.0	3.0	10	3.0	9.0	
t_{PHZ}	Output disable time		Waveform 2	1.5	3.5	5.0	1.5	7.0	1.5	6.0	ns
t_{PLZ}	from HIGH and LOW level		Waveform 3	1.5	3.5	5.5	1.5	7.0	1.5	6.0	
t_{PLH}	Propagation delay	F126	Waveform 1	1.5	4.0	6.5	1.5	8.0	1.5	7.0	ns
t_{PHL}	nA to nY			3.0	5.5	8.0	3.0	9.5	3.0	8.5	
t_{PZH}	Output enable time		Waveform 2	3.0	6.0	7.5	3.0	9.5	3.0	8.5	ns
t_{PZL}	to HIGH and LOW level		Waveform 3	3.0	6.0	8.0	3.0	9.5	3.0	8.5	
t_{PHZ}	Output disable time		Waveform 2	2.0	4.5	6.5	2.0	8.5	2.0	7.5	ns
t_{PLZ}	from HIGH and LOW level		Waveform 3	3.0	5.5	7.5	3.0	9.0	3.0	8.0	

NOTE: Subtract 0.2 ns from minimum values for SO package.

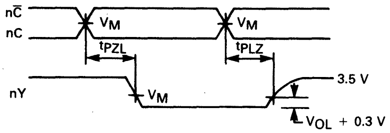
AC WAVEFORMS


nA
V_M
V_M
t_{PLH}
t_{PHL}
nY
V_M
V_M

Waveform 1. Propagation Delay For Input To Output

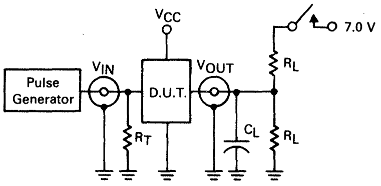

$n\overline{C}$
nC
V_M
V_M
t_{PZH}
t_{PHZ}
$V_{OH} - 0.3\ V$
nY
V_M
0 V

Waveform 2. 3-State Output Enable Time To HIGH Level And Output Disable Time From HIGH Level


$n\overline{C}$
nC
V_M
V_M
t_{PZL}
t_{PLZ}
3.5 V
nY
V_M
$V_{OL} + 0.3\ V$

Waveform 3. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5\ V$


V_{CC}
7.0 V
V_{IN}
V_{OUT}
R_L
Pulse Generator
D.U.T.
R_T
C_L
R_L

MC54F/74F132

Advance Information

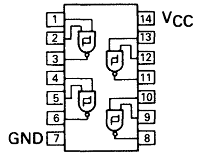
The MC54/74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

QUAD 2-INPUT
NAND
SCHMITT TRIGGER

FAST™ SCHOTTKY TTL

PIN CONFIGURATION



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−1.0	mA
I_{OL}	Output Current — Low	54,74			20	mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage level L = LOW voltage level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{T+}	Positive-Going Threshold Voltage		1.5		2.0	V	V_{CC} = 5.0 V	
V_{T-}	Negative-Going Threshold Voltage		0.7		1.1	V	V_{CC} = 5.0 V	
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54,74	2.5			V	I_{OH} = −1.0 mA	V_{CC} = 4.5
		74	2.7			V	I_{OH} = −1.0 mA	V_{CC} = 4.75
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{T+}	Input Current at Positive-Going Threshold			0		µA	V_{CC} = 5.0 V, V_{IN} = V_{T+}	
I_{T-}	Input Current at Negative-Going Threshold			−350		µA	V_{CC} = 5.0 V, V_{IN} = V_{T-}	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Total, Supply Current	I_{CCH}		8.5	12	mA	V_{IN} = GND	V_{CC} = MAX
		I_{CCL}		13	19.5		V_{IN} = 4.5 V	

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

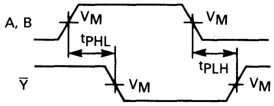
This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
			$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V ±10% $C_L = 50$ pF		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	3.5	5.5	7.0	3.5	9.0	3.5	8.0	ns
t_{PHL}	A, B to $\overline{Y}$		3.0	5.0	6.5	3.0	8.0	3.0	7.0	

NOTE: Subtract 0.2 ns from minimum values for SO package.

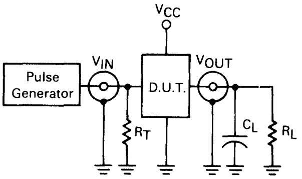
AC WAVEFORM


A, B
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M

Note: For all waveforms, $V_M = 1.5$ V.

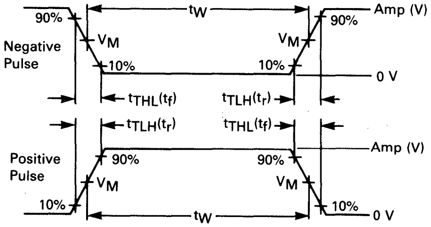
Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS


V_{CC}
Pulse Generator
V_{IN}
D.U.T.
V_{OUT}
R_T
C_L
R_L

Test Circuit For Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


90%
t_W
90%
Amp (V)
Negative Pulse
V_M
V_M
10%
10%
0 V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
Amp (V)
Positive Pulse
90%
90%
V_M
V_M
10%
10%
0 V
t_W

$V_M = 1.5$ V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

MOTOROLA

MC54F/74F138

1-OF-8 DECODER/ DEMULTIPLEXER

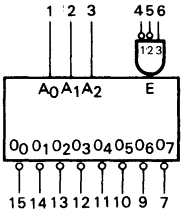
FAST™ SCHOTTKY TTL

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION — The MC54F/74F138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three F138 devices or to a 1-of-32 decoder using four F138s and one inverter.

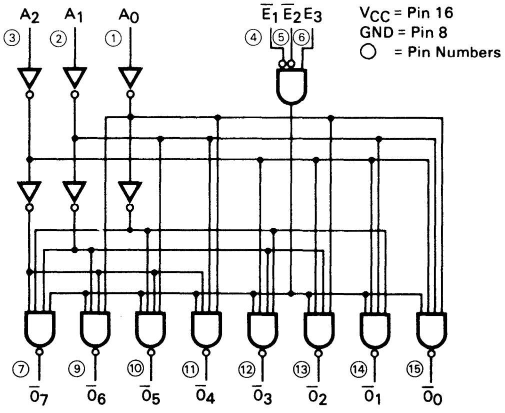
- DEMULTIPLEXING CAPABILITY
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

LOGIC SYMBOL

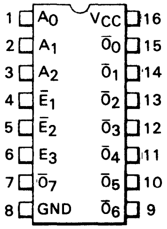

1
2
3
4
5
6
1
2
3
A_0
A_1
A_2
E
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
15
14
13
12
11
10
9
7

V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM


A_2
A_1
A_0
③
②
①
$\overline{E}_1$
$\overline{E}_2$
E_3
④
⑤
⑥
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers
⑦
⑨
⑩
⑪
⑫
⑬
⑭
⑮
$\overline{O}_7$
$\overline{O}_6$
$\overline{O}_5$
$\overline{O}_4$
$\overline{O}_3$
$\overline{O}_2$
$\overline{O}_1$
$\overline{O}_0$

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
A_0
V_{CC}
16
2
A_1
$\overline{O}_0$
15
3
A_2
$\overline{O}_1$
14
4
$\overline{E}_1$
$\overline{O}_2$
13
5
$\overline{E}_2$
$\overline{O}_3$
12
6
E_3
$\overline{O}_4$
11
7
$\overline{O}_7$
$\overline{O}_5$
10
8
GND
$\overline{O}_6$
9

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current				20	mA	V_{CC} = MAX	

AC CHARACTERISTICS

SYMBOL	PARAMETER	LEVELS OF DELAY	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = -55°C to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay,	3	3.0	7.5	3.0	12	3.0	8.5	ns
t_{PHL}	Address to Output		3.0	8.0	3.0	9.5	3.0	9.0	ns
t_{PLH}	Enable to Output	2	3.5	7.0	3.5	11	3.5	8.0	ns
t_{PHL}	$\overline{E}_1$ or $\overline{E}_2$		3.0	7.0	3.0	8.0	3.0	7.5	ns
t_{PLH}	Enable to Output	3	4.0	8.0	4.0	12.5	4.0	9.0	ns
t_{PHL}	E3		3.5	7.5	3.5	8.5	3.5	8.5	ns

NOTES.
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

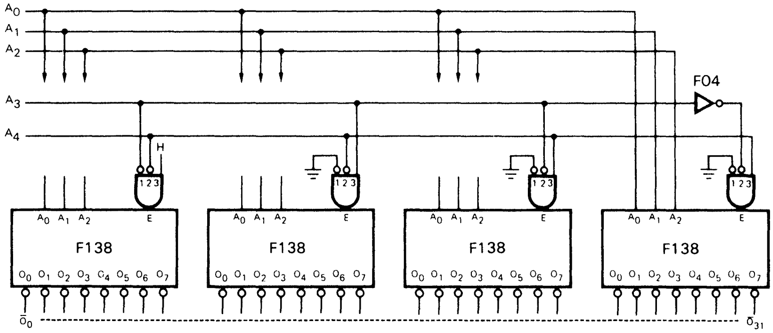
FUNCTIONAL DESCRIPTION — The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The F138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four F138s and one inverter.

The F138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care


A_0
A_1
A_2
A_3
A_4
F04
H
1 2 3
A_0 A_1 A_2
E
F138
O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7
$\overline{O}_0$
$\overline{O}_{31}$

AC TEST CIRCUIT

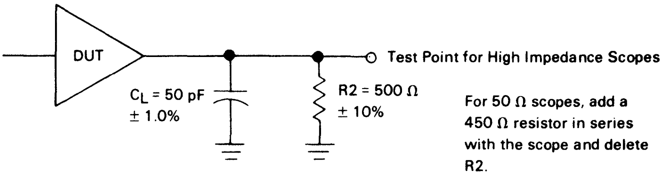

DUT
C_L = 50 pF
± 1.0%
R2 = 500 Ω
± 10%
Test Point for High Impedance Scopes
For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete
R2.

Fig. 1

AC WAVEFORMS

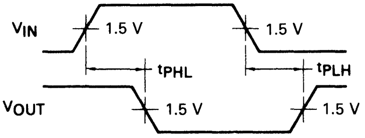

V_{IN}
1.5 V
1.5 V
t_{PHL}
t_{PLH}
V_{OUT}
1.5 V
1.5 V

Fig. 2

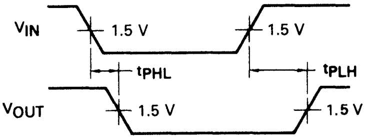

V_{IN}
1.5 V
1.5 V
t_{PHL}
t_{PLH}
V_{OUT}
1.5 V
1.5 V

Fig. 3

MOTOROLA

MC54F/74F139

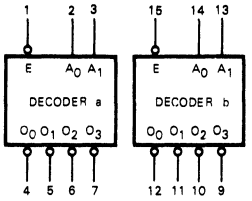
DUAL 1-OF-4 DECODER
FAST™ SCHOTTKY TTL

DUAL 1-OF-4 DECODER

DESCRIPTION — The MC54F/74F139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the F139 can be used as a function generator providing all four minterms of two variables.

- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

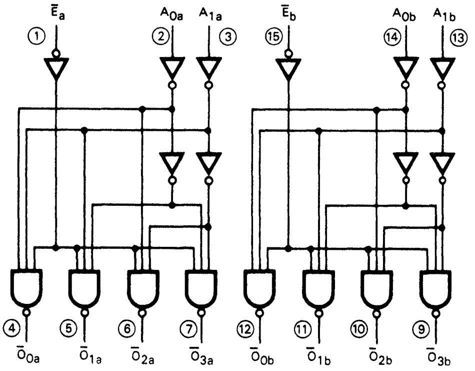
LOGIC SYMBOL



1 2 3
15 14 13
E A_0 A_1
DECODER a
O_0 O_1 O_2 O_3
E A_0 A_1
DECODER b
O_0 O_1 O_2 O_3
4 5 6 7
12 11 10 9

V_{CC} = Pin 16
GND = Pin 8

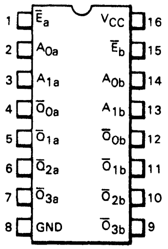
LOGIC DIAGRAM



$\overline{E}_a$
A_{0a}
A_{1a}
$\overline{E}_b$
A_{0b}
A_{1b}
①
②
③
⑮
⑭
⑬
④
⑤
⑥
⑦
⑫
⑪
⑩
⑨
$\overline{O}_{0a}$
$\overline{O}_{1a}$
$\overline{O}_{2a}$
$\overline{O}_{3a}$
$\overline{O}_{0b}$
$\overline{O}_{1b}$
$\overline{O}_{2b}$
$\overline{O}_{3b}$

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 $\overline{E}_a$
2 A_{0a}
3 A_{1a}
4 $\overline{O}_{0a}$
5 $\overline{O}_{1a}$
6 $\overline{O}_{2a}$
7 $\overline{O}_{3a}$
8 GND
16 V_{CC}
15 $\overline{E}_b$
14 A_{0b}
13 A_{1b}
12 $\overline{O}_{0b}$
11 $\overline{O}_{1b}$
10 $\overline{O}_{2b}$
9 $\overline{O}_{3b}$

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current				20	mA	V_{CC} = MAX	

AC CHARACTERISTICS:

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = -55°C to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay,	3.5	7.0	2.5	12.0	3.0	8.5	ns
t_{PHL}	Address to Output	3.5	8.0	3.5	9.5	3.5	9.0	ns
t_{PLH}	Enable to Output	3.5	7.0	3.0	9.0	3.5	8.0	ns
t_{PHL}		2.5	6.5	2.5	8.0	2.5	7.5	ns

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$–$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the F139 generates all four miniterms of two variables. These four miniterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

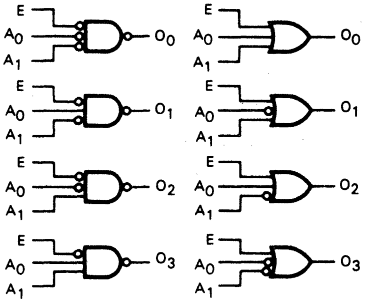

E
A_0
A_1
O_0
O_1
O_2
O_3

Fig. a

AC WAVEFORMS

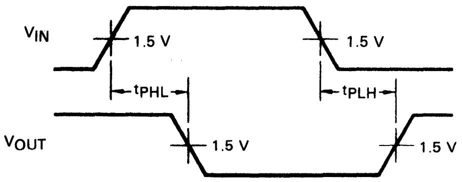

V_{IN}
1.5 V
1.5 V
t_{PHL}
t_{PLH}
V_{OUT}
1.5 V
1.5 V

Fig. 1

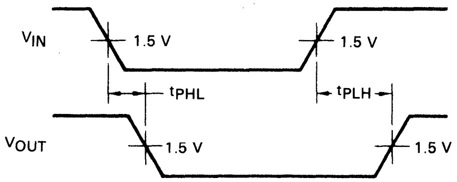
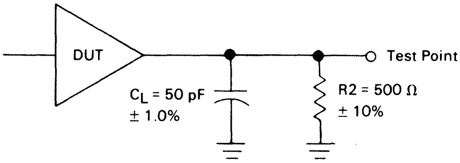

V_{IN}
1.5 V
1.5 V
t_{PHL}
t_{PLH}
V_{OUT}
1.5 V
1.5 V

Fig. 2

AC TEST CIRCUIT


DUT
C_L = 50 pF ± 1.0%
R2 = 500 Ω ± 10%

Test Point for High Impedance Scopes

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 3

MOTOROLA

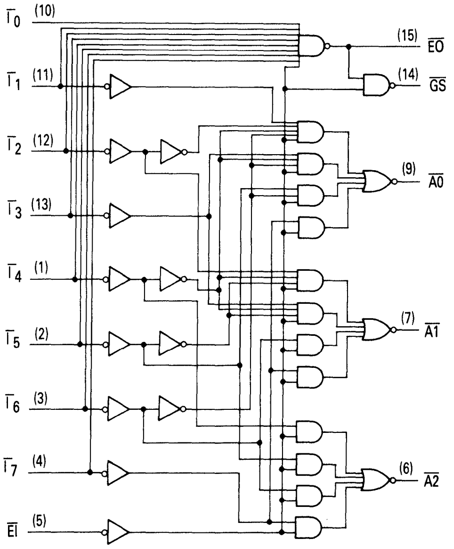
MC54F/74F148

Advance Information

8-LINE TO 3-LINE PRIORITY ENCODER

The MC54/74F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

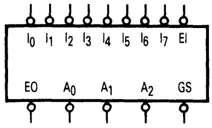
- Encodes Eight Data Lines in Priority
- Provides 3-Bit Binary Priority Code
- Input Enable Capability
- Signals When Data Present on Any Input
- Cascadable for Priority Encoding of n Bits



$\overline{I_0}$ (10)
$\overline{I_1}$ (11)
$\overline{I_2}$ (12)
$\overline{I_3}$ (13)
$\overline{I_4}$ (1)
$\overline{I_5}$ (2)
$\overline{I_6}$ (3)
$\overline{I_7}$ (4)
$\overline{EI}$ (5)
(15) $\overline{EO}$
(14) $\overline{GS}$
(9) $\overline{A0}$
(7) $\overline{A1}$
(6) $\overline{A2}$

Logic Diagram

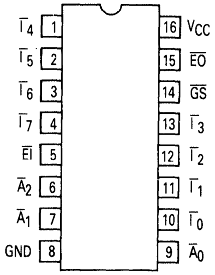
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 EI
EO A_0 A_1 A_2 GS

LOGIC SYMBOL

CONNECTION DIAGRAM



$\overline{I_4}$ 1
$\overline{I_5}$ 2
$\overline{I_6}$ 3
$\overline{I_7}$ 4
$\overline{EI}$ 5
$\overline{A_2}$ 6
$\overline{A_1}$ 7
GND 8
16 V_{CC}
15 $\overline{EO}$
14 $\overline{GS}$
13 $\overline{I_3}$
12 $\overline{I_2}$
11 $\overline{I_1}$
10 $\overline{I_0}$
9 $\overline{A_0}$

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION

The 'F148 8-input priority encoder accepts data from eight active LOW inputs ($\overline{I}_0$–$\overline{I}_7$) and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output ($\overline{GS}$) and Enable Output ($\overline{EO}$) are provided along with the three priority data outputs ($\overline{A}_2$, $\overline{A}_1$, $\overline{A}_0$). $\overline{GS}$ is active LOW when any input is LOW: this indicates when any input is active. $\overline{EO}$ is active LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows cascading for priority encoding on any number of input signals. Both $\overline{EO}$ and $\overline{GS}$ are in the inactive HIGH state when the Enable Input is HIGH.

TRUTH TABLE

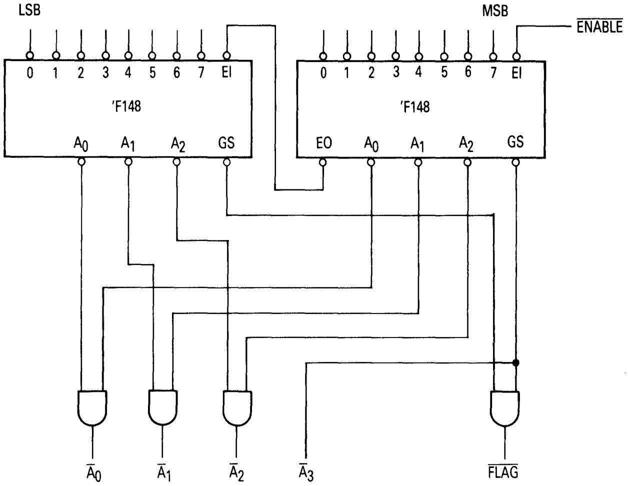
Inputs									Outputs				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Units	Test Conditions	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					100	μA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	$\overline{I}_0$, $\overline{EI}$				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
	$\overline{I}_1$–$\overline{I}_7$				−1.2	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			23	35	mA	V_{CC} = MAX, V_{IN} = 4.5 V	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.


LSB
MSB
$\overline{ENABLE}$
0 1 2 3 4 5 6 7 EI
'F148
A_0 A_1 A_2 GS
0 1 2 3 4 5 6 7 EI
'F148
EO A_0 A_1 A_2 GS
$\overline{A}_0$
$\overline{A}_1$
$\overline{A}_2$
$\overline{A}_3$
$\overline{FLAG}$

Application
16-Input Priority Encoder

AC CHARACTERISTICS

Symbol	Parameter	54F/74F			54F		74F		Units
		$T_A = +25°C$ $V_{CC} = +5$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{A}_n$	3.5 4	7 8	9 10.5	3.5 4	11 13	3.5 4	10 12	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{EO}$	2.5 2	5 5.5	6.5 7.5	2.5 2	8.5 9.5	2.5 2	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{GS}$	3 2	7 6	9 8	3 2	11 10	3 2	10 9	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{A}_n$	3.5 3	6.5 6	8.5 8	3.5 3	10.5 10	3.5 3	9.5 9	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{GS}$	2.5 3	5 6	7 7.5	2.5 3	9 10	2.5 3	8 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$	3 4.5	5.5 8	7 10.5	3 4.5	9 13	3 4.5	8 12	ns

MC54F/74F151

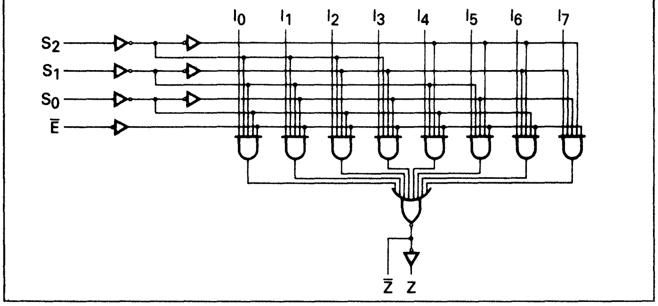
8-INPUT MULTIPLEXER

DESCRIPTION — The MC54F/74F151 is a high-speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The 'F151 can be used as a universal function generator to generate any logic function of four variables. Both asserted and negated outputs are provided.

The 'F151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. The Enable input ($\overline{E}$) is active LOW. The logic function provided at the output is:

$$
\begin{aligned}
Z = \overline{E} \bullet (&I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + \\
&I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + \\
&I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + \\
&I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)
\end{aligned}
$$

LOGIC DIAGRAM



I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
S_2
S_1
S_0
$\overline{E}$
$\overline{Z}$
Z

TRUTH TABLE

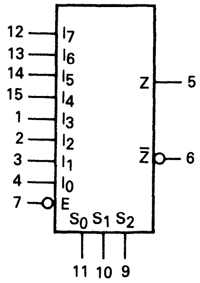
INPUTS				OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

8-INPUT MULTIPLEXER

FAST™ SCHOTTKY TTL

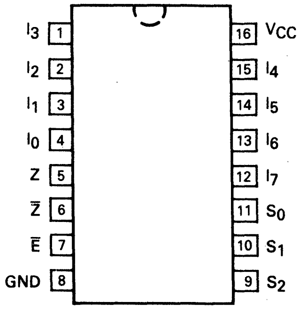
LOGIC SYMBOL



12
13
14
15
1
2
3
4
7
I_7
I_6
I_5
I_4
I_3
I_2
I_1
I_0
E
Z
5
$\overline{Z}$
6
S_0 S_1 S_2
11 10 9

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



I_3 1
I_2 2
I_1 3
I_0 4
Z 5
$\overline{Z}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					100	µA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			13.5	21	mA	V_{CC} = MAX, V_{IN} = 4.5 V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$	4.0 3.2	8.0 6.1	3.5 3.0	10 8.0	3.5 3.2	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to Z	4.5 4.5	13 9.0	3.0 4.0	17.5 11.5	4.0 4.0	14 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	3.0 3.0	6.1 8.5	2.5 2.5	7.5 10.5	2.5 2.5	7.0 10	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0 3.5	9.5 7.0	3.0 3.0	14.5 9.5	4.0 3.5	11 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	2.5 1.5	5.7 4.0	2.5 1.5	7.5 6.0	2.5 1.5	6.5 5.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z	3.0 3.0	9.5 6.5	2.5 3.0	11.5 8.0	2.5 3.0	11 7.5	ns

MOTOROLA

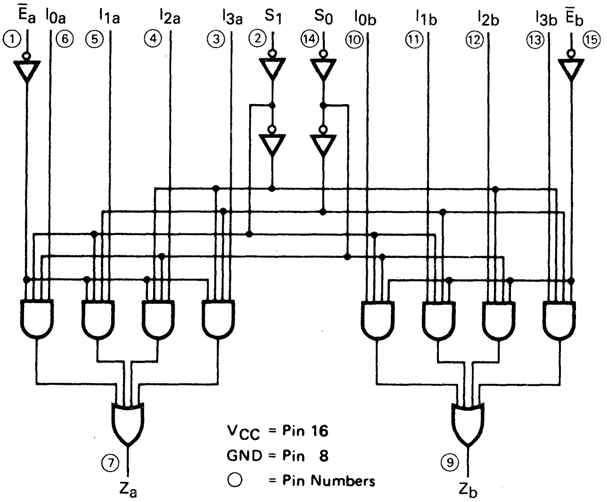
MC54F/74F153

DUAL 4-INPUT MULTIPLEXER

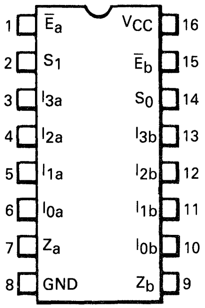
DESCRIPTION — The MC54F/74F153 is a high-speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the F153 can generate any two functions of three variables.

DUAL 4-INPUT MULTIPLEXER
FAST™ SCHOTTKY TTL

LOGIC DIAGRAM


$\overline{E}_a$ ①
I_{0a} ⑥
I_{1a} ⑤
I_{2a} ④
I_{3a} ③
S_1 ②
S_0 ⑭
I_{0b} ⑩
I_{1b} ⑪
I_{2b} ⑫
I_{3b} ⑬
$\overline{E}_b$ ⑮
⑦ Z_a
⑨ Z_b
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP
(TOP VIEW)


1 $\overline{E}_a$
2 S_1
3 I_{3a}
4 I_{2a}
5 I_{1a}
6 I_{0a}
7 Z_a
8 GND
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Z_b

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74	—	—	−1.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	20	mA

FUNCTIONAL DESCRIPTION

The F153 is a Dual 4-Input Multiplexer. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

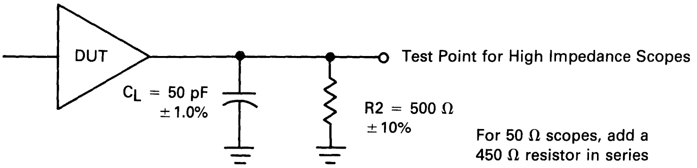
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA, V_{CC} = MIN	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OL} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V, V_{CC} = MAX	
					0.1	mA	V_{IN} = 7.0 V, V_{CC} = MAX	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V, V_{CC} = MAX	
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V, V_{CC} = MAX	
I_{CC}	Power Supply Current				20	mA	V_{IN} = GND, V_{CC} = MAX	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		74F $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.5 3.5	10.5 9.0	4.5 3.5	14 11	4.5 3.5	12 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	4.5 3.0	9.0 7.0	4.5 2.5	11.5 9.0	4.5 2.5	10.5 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	3.0 3.0	7.0 6.5	2.5 2.5	9.0 8.0	3.0 2.5	8.0 7.5	ns

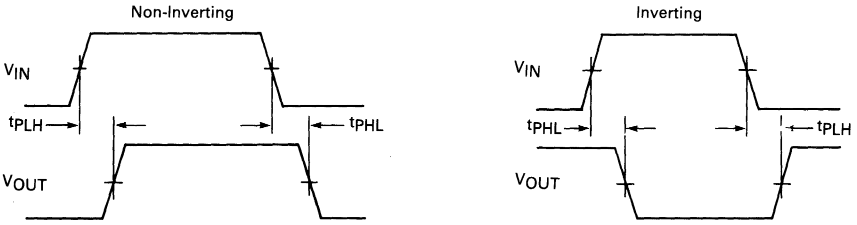
AC TEST CIRCUIT



DUT
$C_L = 50$ pF
±1.0%
Test Point for High Impedance Scopes
R2 = 500 Ω
±10%

For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete R2.

PROPAGATION DELAY MEASUREMENTS



Non-Inverting
Inverting
V_{IN}
t_{PLH}
t_{PHL}
V_{OUT}
V_{IN}
t_{PHL}
t_{PLH}
V_{OUT}

NOTES:

1. All input waveforms have the following characteristics:
   Low Level = 0 V
   High Level = 3.0 V
   Rise and Fall Times (10% to 90%) = 2.5 ns

2. All timing is measured at 1.5 V unless otherwise indicated.

MC54F/74F157

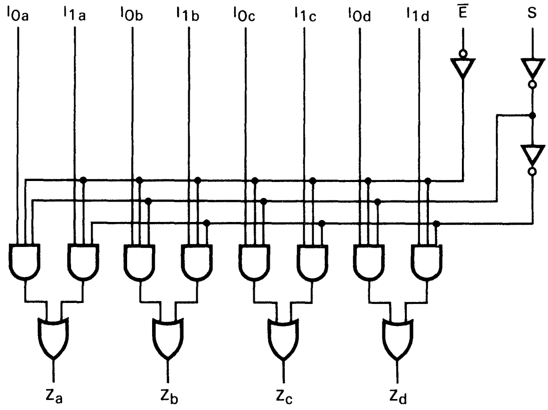
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The MC54F/74F157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157 can also be used to generate any four of the 16 different functions to two variables.

QUAD 2-INPUT MULTIPLEXER

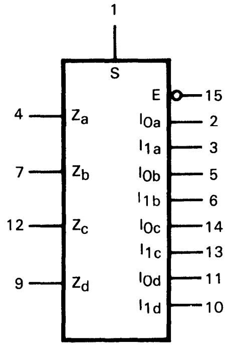
FAST™ SCHOTTKY TTL

LOGIC DIAGRAM



I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
$\overline{E}$
S
Z_a
Z_b
Z_c
Z_d

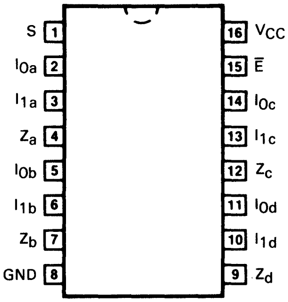
LOGIC SYMBOL



1
S
E
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



S 1
I_{0a} 2
I_{1a} 3
Z_a 4
I_{0b} 5
I_{1b} 6
Z_b 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN,
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.50$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			15	23	mA	All Inputs = 4.5 V	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	4.5 3.5	10.1 6.3	13 9.0	3.5 3.5	17 12.5	4.5 3.5	15 10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	5.0 3.8	7.6 5.3	10 7.0	5.0 3.8	15 8.5	5.0 3.8	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	3.0* 2.5	5.5 4.6	7.0 5.5	3.0 1.5	10 7.5	3.0 2.0	8.0 7.0	ns

FUNCTIONAL DESCRIPTION — The F157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the F157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

MOTOROLA

Advance Information

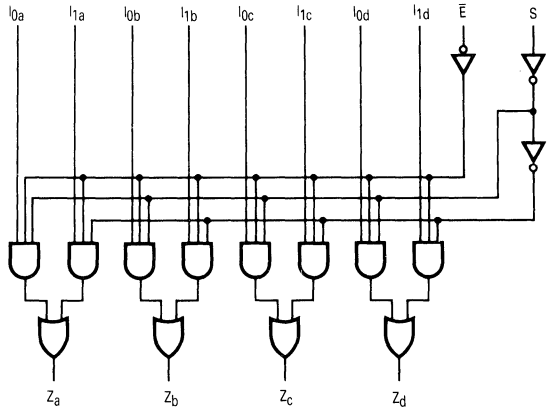
Quad 2-Input Multiplexer

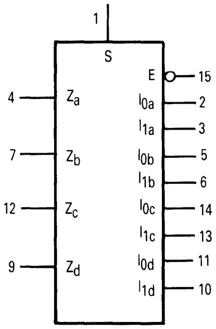
MC74F157A

QUAD 2-INPUT
MULTIPLEXER
FAST™ SCHOTTKY TTL

The MC74F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The F157A can also be used to generate any four of the 16 different functions to two variables.

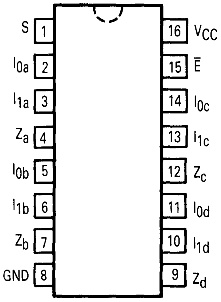
LOGIC DIAGRAM


I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
$\overline{E}$
S
Z_a
Z_b
Z_c
Z_d


1
S
E
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

LOGIC SYMBOL

CONNECTION DIAGRAM


S 1
I_{0a} 2
I_{1a} 3
Z_a 4
I_{0b} 5
I_{1b} 6
Z_b 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

J SUFFIX — CASE 620-09 (CERAMIC)
N SUFFIX — CASE 648-08 (PLASTIC)
D SUFFIX — CASE 751B-03 (SOIC)

TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This document contains information on a new product. Specifications and information herein are subject to change without notice.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−1	mA
I_{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Units	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75
		74	2.5					V_{CC} = 4.5
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			15	23	mA	All Inputs = 4.5 V	V_{CC} = MAX

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

		74F T_A = +25°C V_{CC} = +5 V C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5 V ±10% C_L = 50 pF		
Symbol	Parameter	Min	Max	Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	3.5 3	10 7	3.5 3	11 8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.5 2.5	9.5 6.5	3.5 2.5	11 7	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	2 2.5	6 5.5	2 2	6.5 7	ns

FUNCTIONAL DESCRIPTION

The F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

A common use of the F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

MOTOROLA

MC54F/74F158

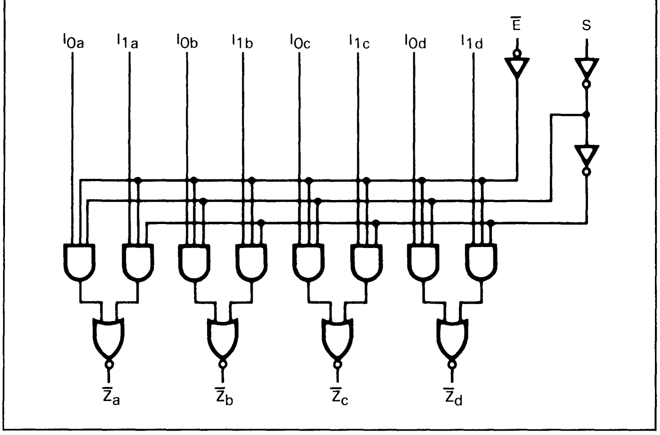
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The MC54F/74F158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'F158 can also generate any four of the 16 different functions of two variables.

QUAD 2-INPUT MULTIPLEXER

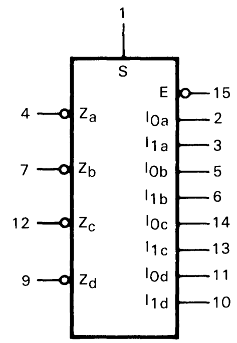
FAST™ SCHOTTKY TTL

LOGIC DIAGRAM



I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
$\overline{E}$
S
$\overline{Z}_a$
$\overline{Z}_b$
$\overline{Z}_c$
$\overline{Z}_d$

LOGIC SYMBOL



1
S
E
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

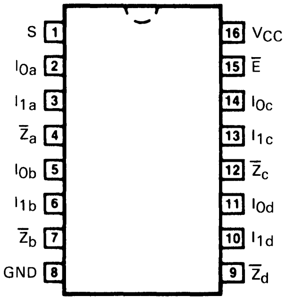
V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE

INPUTS				OUTPUTS
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CONNECTION DIAGRAM



S 1
I_{0a} 2
I_{1a} 3
$\overline{Z}_a$ 4
I_{0b} 5
I_{1b} 6
$\overline{Z}_b$ 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 $\overline{Z}_c$
11 I_{0d}
10 I_{1d}
9 $\overline{Z}_d$

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = −18 mA	V_{CC} = MIN,
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current*			10	15	mA	V_{CC} = MAX	V_{IN} = HIGH

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF MIN	54/74F MAX	54F T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF MIN	54F MAX	74F T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF MIN	74F MAX	UNITS
t_{PLH}	Propagation Delay	4.0	8.5	4.0	10.5	4.0	9.5	ns
t_{PHL}	S to $\overline{Z}$	4.0	9.0	4.0	10.5	4.0	10.5	
t_{PLH}	Propagation Delay	3.5	8.0	3.5	9.5	3.5	9.0	ns
t_{PHL}	$\overline{E}$ to $\overline{Z}_n$	3.5	8.5	3.5	9.5	3.5	9.5	
t_{PLH}	Propagation Delay	3.0	5.9	2.5	8.5	3.0	7.0	ns
t_{PHL}	I_n to $\overline{Z}$	1.5	4.5	1.5	6.0	1.5	5.5	

*I_{CC} measured with outputs open and 4.5 V applied to all inputs.

FUNCTIONAL DESCRIPTION — The F158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The F158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the F158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F158 can generate four functions of two variables with one variable n common. This is useful for implementing gating functions.

MOTOROLA

Advance Information

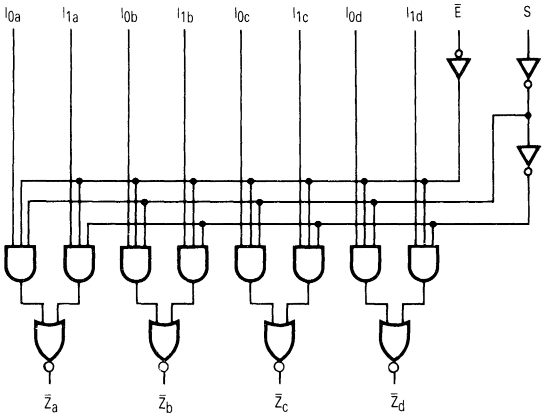
Quad 2-Input Multiplexer

MC74F158A

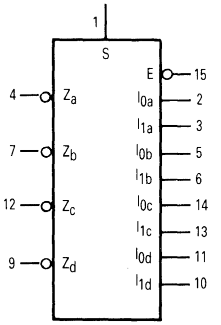
QUAD 2-INPUT
MULTIPLEXER
FAST™ SCHOTTKY TTL

The MC74F158A is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The F158A can also generate any four of the 16 different functions of two variables.

LOGIC DIAGRAM



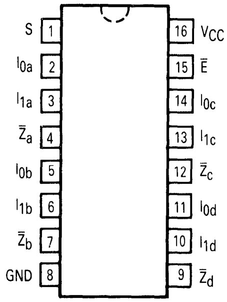
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
$\overline{E}$
S
$\overline{Z}_a$
$\overline{Z}_b$
$\overline{Z}_c$
$\overline{Z}_d$



1
S
E
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

LOGIC SYMBOL

CONNECTION DIAGRAM



S 1
I_{0a} 2
I_{1a} 3
$\overline{Z}_a$ 4
I_{0b} 5
I_{1b} 6
$\overline{Z}_b$ 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 $\overline{Z}_c$
11 I_{0d}
10 I_{1d}
9 $\overline{Z}_d$

J SUFFIX — CASE 620-09 (CERAMIC)
N SUFFIX — CASE 648-08 (PLASTIC)
D SUFFIX — CASE 751B-03 (SOIC)

TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This document contains information on a new product. Specifications and information herein are subject to change without notice.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−1	mA
I_{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Units	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75
		74	2.5					V_{CC} = 4.5
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current (Note 3)			10	15	mA	V_{CC} = MAX, V_{IN} = HIGH	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.
3. I_{CC} measured with outputs open and 4.5 V applied to all inputs.

AC CHARACTERISTICS

		74F T_A = +25°C V_{CC} = +5 V C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5 V ±10% C_L = 50 pF		
Symbol	Parameter	Min	Max	Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}$	3 2.5	8.5 6.5	3 2.5	9.5 7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	2.5 2	6 6	2.5 2	7 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	2 1	5.9 4	2 1	7 4.5	ns

FUNCTIONAL DESCRIPTION

The F158A quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The F158A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the F158A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F158A can generate four functions of two variables with one variable n common. This is useful for implementing gating functions.

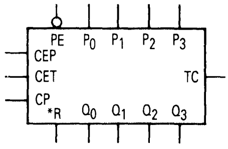
MOTOROLA

MC54F/74F160A
MC54F/74F162A

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

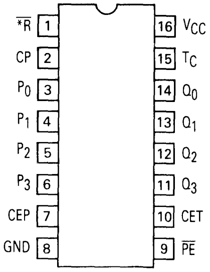
The MC54/74F160A and MC54/74F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC54/74F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC54/74F162A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The MC54 74F160A and MC54/74F162A are high-speed versions of the MC54/74F160 and MC54/74F162.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz


PE
P0
P1
P2
P3
CEP
CET
TC
CP
*R
Q0
Q1
Q2
Q3

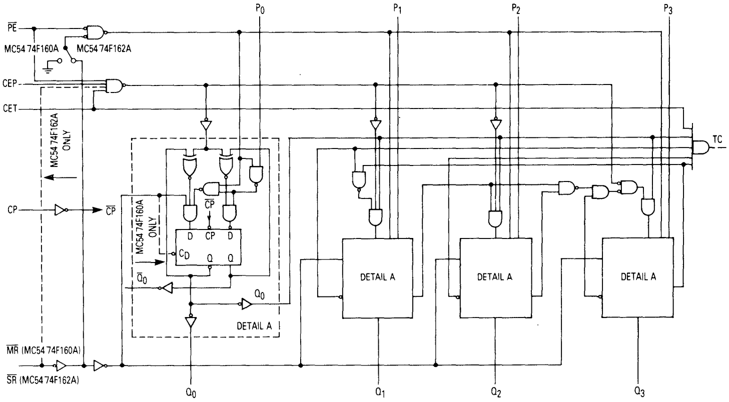
LOGIC SYMBOL

*$\overline{MR}$ for MC54/74F160A
*$\overline{SR}$ for MC54/74F162A


*R 1
CP 2
P0 3
P1 4
P2 5
P3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

CONNECTION DIAGRAM

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)


P0
P1
P2
P3
PE
MC54 74F160A
MC54 74F162A
CEP
CET
MC54 74F162A ONLY
CP
CP
MC54 74F160A ONLY
D CP D
CD Q Q
Q0
Q0
DETAIL A
DETAIL A
DETAIL A
DETAIL A
TC
MR (MC54 74F160A)
SR (MC54 74F162A)
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1	mA
I_{OL}	Output Current — Low	54, 74			20	mA

Functional Description

The MC54/74F160A and MC54/74F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the MC54/74F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC54/74F160A), synchronous reset (MC54/74F162A), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{\text{MR}}$, MC54/74F160A), Synchronous Reset ($\overline{\text{SR}}$. MC54/74F162A), Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{\text{MR}}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{\text{SR}}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{\text{PE}}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{\text{PE}}$ and $\overline{\text{MR}}$ (MC54/74F160A) or $\overline{\text{SR}}$ (MC54/74F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

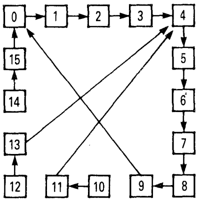
The MC54/74F160A and MC54/74F162A use D-type edge triggered flip-flops and changing the $\overline{\text{SR}}$, $\overline{\text{PE}}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

TRUTH TABLE

*$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	Action on the Rising Clock Edge (↑)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For MC54/74F162A only H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

State Diagram



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Units	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current $\overline{\text{MR}}$, Data, CEP, Clock $\overline{\text{PE}}$, CET, $\overline{\text{SR}}$				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	$\overline{\text{MR}}$, Data, CEP, Clock $\overline{\text{PE}}$, CET				0.1 0.1	mA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	Input LOW Current $\overline{\text{MR}}$, Data, CEP, Clock $\overline{\text{PE}}$, CET, $\overline{\text{SR}}$				−0.6 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Short Circuit Current		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			37	55	mA	V_{CC} = MAX	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC54/74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the MC54/74F160A and MC54/74F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

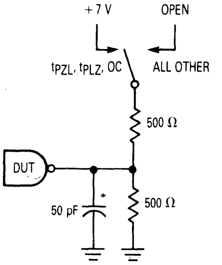
Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$
$TC = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$

AC CHARACTERISTICS See Page 5 for waveforms and load configurations

Symbol	Parameter	54/74F $T_A = +25°C$ $V_{CC} = +5$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5$ V ±10% $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5$ V ±10% $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	100		75		90		MHz
t_{PLH}	Propagation Delay, Count CP to Q_n ($\overline{PE}$ Input HIGH)	3.5	7.5	3.5	9	3.5	8.5	ns
t_{PHL}		3.5	10	3.5	11.5	3.5	11	
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.5	8.5	4	10	3.5	9.5	
t_{PHL}		4	8.5	4	10	4	9.5	
t_{PLH}	Propagation Delay CP to TC	5	14	5	16.5	5	15	ns
t_{PHL}		4.5	14	5	15	4.5	15	
t_{PLH}	Propagation Delay CET to TC	2.5	7.5	2.5	9	2.5	8.5	ns
t_{PHL}		2.5	7.5	2.5	9	2.5	8.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (MC54/74F160A)	5.5	12	5.5	14	5.5	13	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC (MC54/74F160A)	4.5	10.5	4.5	12.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS: See Page 5 for waveforms

Symbol	Parameter	54/74F $T_A = +25°C$ $V_{CC} = +5$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5$ V ±10% $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5$ V ±10% $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
t_s(H)	Setup Time, HIGH or LOW P_n to CP	5		5.5		5		ns
t_s(L)		5		5.5		5		
t_h(H)	Hold Time, HIGH or LOW P_n to CP	2		2.5		2		
t_h(L)		2		2.5		2		
t_s(H)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11		13.5		11.5		ns
t_s(L)		8.5		10.5		9.5		
t_h(H)	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2		2		2		
t_h(L)		0		0		0		
t_s(H)	Setup Time, HIGH or LOW CEP or CET to CP	11		13		11.5		ns
t_s(L)		5		6		5		
t_h(H)	Hold Time, HIGH or LOW CEP or CET to CP	0		0		0		
t_H(L)		0		0		0		
t_w(H)	Clock Pulse Width (Load) HIGH or LOW	5		5		5		ns
t_w(L)		5		5		5		
t_w(H)	Clock Pulse Width (Count) HIGH or LOW	4		5		4		ns
t_w(L)		6		8		7		
t_w(L)	$\overline{MR}$ Pulse Width, LOW (MC54/74F160A)	5		5		5		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP (MC54/74F160A)	6		6		6		


+7 V
OPEN
t_{PZL}, t_{PLZ}, OC
ALL OTHER
500 Ω
DUT
50 pF
*
500 Ω

*INCLUDES JIG AND PROBE CAPACITANCE

Figure 1. Test Load

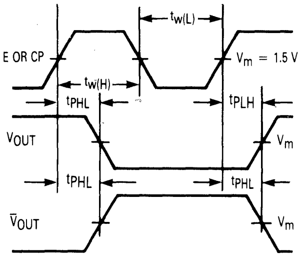

$t_{w(L)}$
E OR CP
V_m = 1.5 V
$t_{w(H)}$
t_{PHL}
t_{PLH}
V_{OUT}
V_m
t_{PHL}
t_{PHL}
$\overline{V}_{OUT}$
V_m

Figure 2. Propagation Delays from Rising-edge Clock or Enable

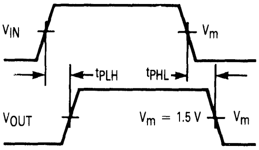

V_{IN}
V_m
t_{PLH}
t_{PHL}
V_{OUT}
V_m = 1.5 V
V_m

Figure 3. Waveform for Non-Inverting Functions

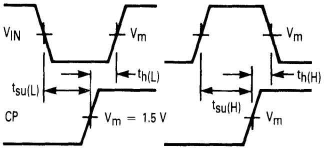

V_{IN}
V_m
V_m
$t_{h(L)}$
$t_{h(H)}$
$t_{su(L)}$
CP
V_m = 1.5 V
$t_{su(H)}$
V_m

Figure 4. Setup and Hold Times, Rising-edge Clock

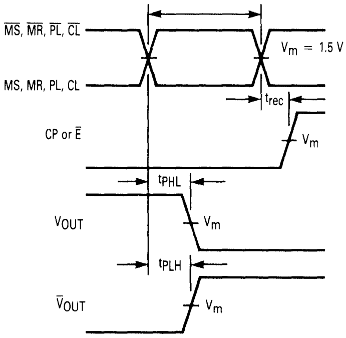

$\overline{MS}$, $\overline{MR}$, $\overline{PL}$, $\overline{CL}$
V_m = 1.5 V
MS, MR, PL, CL
t_{rec}
CP or $\overline{E}$
V_m
t_{PHL}
V_{OUT}
V_m
t_{PLH}
$\overline{V}_{OUT}$
V_m

Figure 5. Asychronous Set, Reset, Parallel Load or Clear, Active Rising-edge Clock or Active-LOW Enable

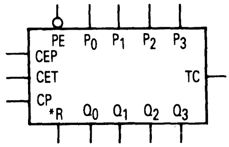
MOTOROLA

MC54F/74F161A
MC54F/74F163A

SYNCHRONOUS PRESETTABLE BINARY COUNTER

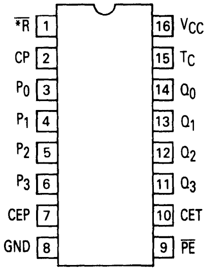
The MC54/74F161A and MC54/74F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC54/74F161A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC54/74F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The MC54/74F161A and MC54/74F163A are high-speed versions of the MC54/74F161 and MC54/74F163.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Frequency of 120 MHz


PE
P0
P1
P2
P3
CEP
CET
TC
CP
*R
Q0
Q1
Q2
Q3

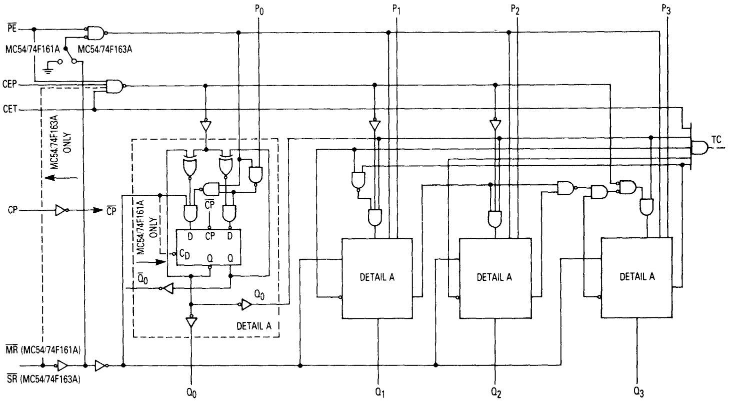
LOGIC SYMBOL

*$\overline{MR}$ for MC54/74F161A
*$\overline{SR}$ for MC54/74F163A


*R 1
CP 2
P0 3
P1 4
P2 5
P3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

CONNECTION DIAGRAM

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)


P0
P1
P2
P3
PE
MC54/74F161A
MC54/74F163A
CEP
CET
MC54/74F163A ONLY
TC
CP
CP
MC54/74F161A ONLY
D CP D
CD Q Q
Q0
Q0
DETAIL A
DETAIL A
DETAIL A
DETAIL A
MR (MC54/74F161A)
SR (MC54/74F163A)
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1	mA
I_{OL}	Output Current — Low	54, 74			20	mA

Functional Description

The MC54/74F161A and MC54/74F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the MC54/74F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC54/74F161A), synchronous reset (MC54/74F163A), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{\text{MR}}$, MC54/74F161A), Synchronous Reset ($\overline{\text{SR}}$, MC54/74F163A), Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{\text{MR}}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{\text{SR}}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{\text{PE}}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{\text{PE}}$ and $\overline{\text{MR}}$ (MC54/74F161A) or $\overline{\text{SR}}$ (MC54/74F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

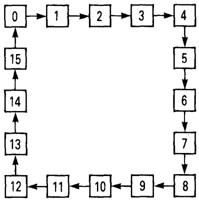
The MC54/74F161A and MC54/74F163A use D-type edge triggered flip-flops and changing the $\overline{\text{SR}}$, $\overline{\text{PE}}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

TRUTH TABLE

*$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	Action on the Rising Clock Edge (_/‾)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For MC54/74F163A only H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

State Diagram



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Units	Test Conditions	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current Data, CEP, Clock $\overline{\text{PE}}$, CET, $\overline{\text{SR}}$				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, CEP, Clock $\overline{\text{PE}}$, CET, $\overline{\text{SR}}$				0.1 0.1	mA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	Input LOW Current Data, CEP, Clock $\overline{\text{PE}}$, CET, $\overline{\text{SR}}$				−0.6 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Short Circuit Current		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			37	55	mA	V_{CC} = MAX	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

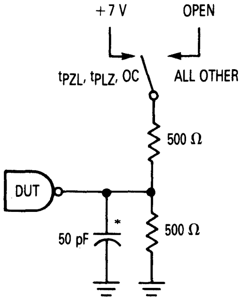
Logic Equations: Count Enable = $CEP \bullet CET \bullet \overline{PE}$
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

AC CHARACTERISTICS

Symbol	Parameter	54/74F $T_A = +25°C$ $V_{CC} = +5\ V$ $C_L = 50\ pF$		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	100		75		90		MHz
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.5	6.0	3.5	9	3.5	7.0	ns
t_{PHL}		3.5	10	3.5	11.5	3.5	11	
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.5	7.0	4	10	3.5	8.0	
t_{PHL}		4	8.5	4	10	4	9.5	
t_{PLH}	Propagation Delay CP to TC	5	14	5	16.5	5	15	ns
t_{PHL}		4.5	14	5	15	4.5	15	
t_{PLH}	Propagation Delay CET to TC	2.5	7.5	2.5	9	2.5	8.5	ns
t_{PHL}		2.5	7.5	2.5	9	2.5	8.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (MC54/74F161A)	5.5	12	5.5	14	5.5	13	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	4.5	10.5	4.5	12.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F $T_A = +25°C$ $V_{CC} = +5\ V$ $C_L = 50\ pF$		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW P_n to CP	5		5.5		5		ns
$t_s(L)$		5		5.5		5		
$t_h(H)$	Hold Time, HIGH or LOW P_n to CP	2		2.5		2		
$t_h(L)$		2		2.5		2		
$t_s(H)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11		13.5		11.5		ns
$t_s(L)$		8.5		10.5		9.5		
$t_h(H)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2		2		2		
$t_h(L)$		0		0		0		
$t_s(H)$	Setup Time, HIGH or LOW CEP or CET to CP	11		13		11.5		ns
$t_s(L)$		5		6		5		
$t_h(H)$	Hold Time, HIGH or LOW CEP or CET to CP	0		0		0		
$t_H(L)$		0		0		0		
$t_w(H)$	Clock Pulse Width (Load) HIGH or LOW	5		5		5		ns
$t_w(L)$		5		5		5		
$t_w(H)$	Clock Pulse Width (Count) HIGH or LOW	4		5		4		ns
$t_w(L)$		6		8		7		
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW (MC54/74F161A)	5		5		5		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP (MC54/74F161A)	6		6		6		


+7 V
OPEN
tPZL, tPLZ, OC
ALL OTHER
500 Ω
DUT
*
50 pF
500 Ω

*INCLUDES JIG AND PROBE CAPACITANCE

Figure 1. Test Load

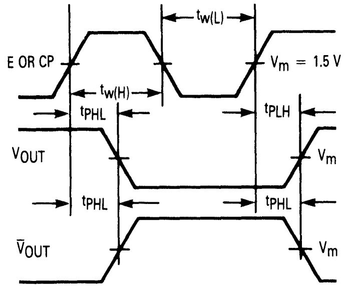

tw(L)
E OR CP
Vm = 1.5 V
tw(H)
tPHL
tPLH
VOUT
Vm
tPHL
tPHL
V̄OUT
Vm

Figure 2. Propagation Delays from Rising-edge Clock or Enable

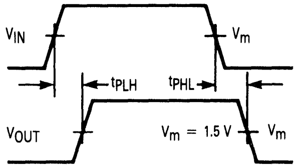

VIN
Vm
tPLH
tPHL
VOUT
Vm = 1.5 V
Vm

Figure 3. Waveform for Non-Inverting Functions

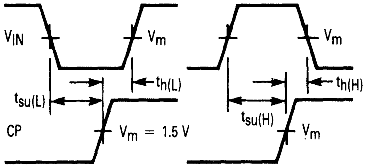

VIN
Vm
th(L)
tsu(L)
CP
Vm = 1.5 V
Vm
th(H)
tsu(H)
Vm

Figure 4. Setup and Hold Times, Rising-edge Clock

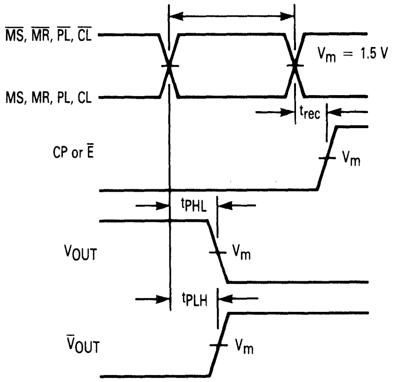

M̄S̄, M̄R̄, P̄L̄, C̄L̄
Vm = 1.5 V
MS, MR, PL, CL
trec
CP or Ē
Vm
tPHL
VOUT
Vm
tPLH
V̄OUT
Vm

Figure 5. Asychronous Set, Reset, Parallel Load or Clear, Active Rising-edge Clock or Active-LOW Enable

MOTOROLA

MC54F/74F168
MC54F/74F169

Advance Information

4-STAGE SYNCHRONOUS BIDIRECTIONAL COUNTERS

DESCRIPTION — The MC54/74F168 and MC54/74F169 are fully synchronous 4-stage up/down counters. The F168 is a BCD decade counter; the F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

- **Asynchronous Counting and Loading**
- **Built-In Lookahead Carry Capability**
- **Presettable for Programmable Operation**

GUARANTEED OPERATING RANGES

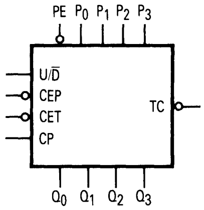
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

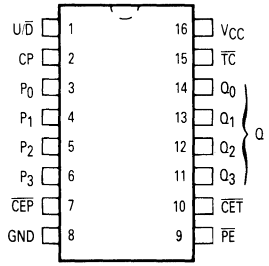
4-STAGE SYNCHRONOUS BIDIRECTIONAL COUNTERS

FAST™ SCHOTTKY TTL

LOGIC SYMBOL



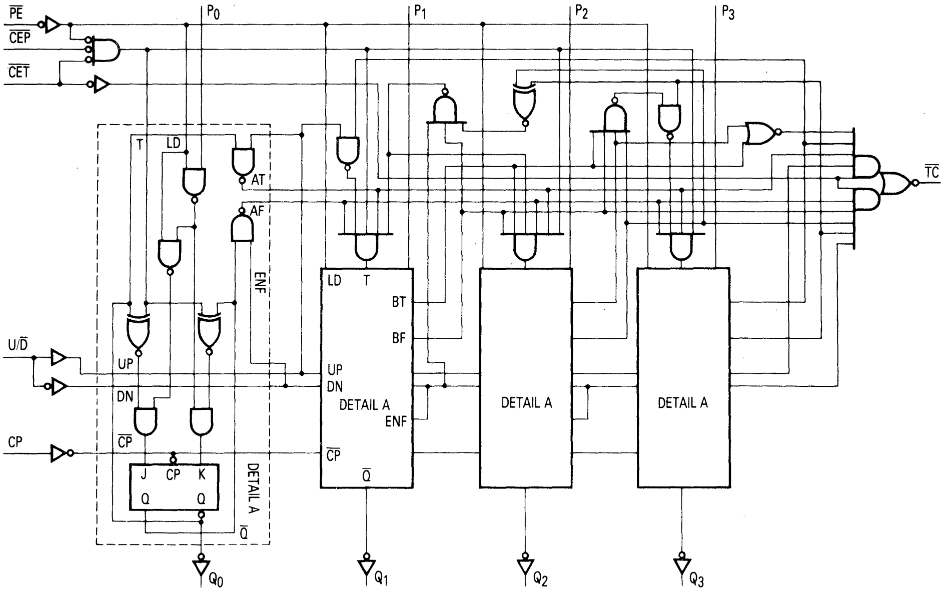
CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

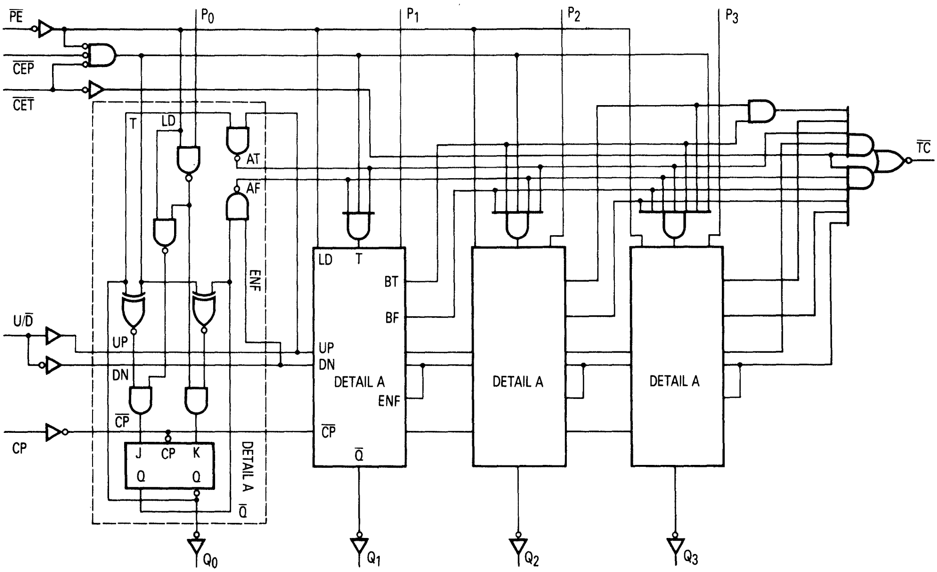
LOGIC DIAGRAMS

MC54/74F168



PE
CEP
CET
P0
P1
P2
P3
T
LD
AT
AF
ENF
U/D
UP
DN
CP
CP
J
CP
K
Q
Q
DETAIL A
Q
LD
T
BT
BF
UP
DN
DETAIL A
ENF
CP
Q
DETAIL A
DETAIL A
TC
Q0
Q1
Q2
Q3

MC54/74F169



PE
CEP
CET
P0
P1
P2
P3
T
LD
AT
AF
ENF
U/D
UP
DN
CP
CP
J
CP
K
Q
Q
DETAIL A
Q
LD
T
BT
BF
UP
DN
DETAIL A
ENF
CP
Q
DETAIL A
DETAIL A
TC
Q0
Q1
Q2
Q3

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F168 and F169 use edge-triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the F169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the F168 decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot PE$
2) Up: ('F168): $\overline{TC} = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
('F169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
3) Down: $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (Down) \cdot \overline{CET}$

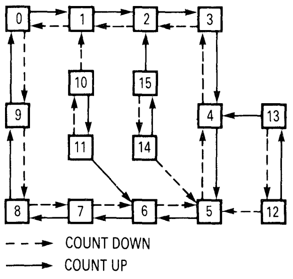
MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

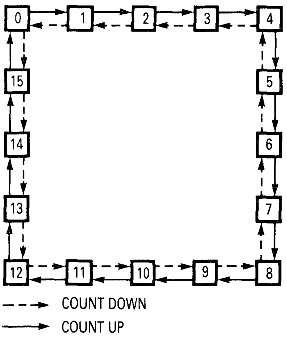
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAMS

MC54/74F168



MC54/74F169



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{\text{CET}}$ Other Inputs				−1.2 −0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Short Circuit Current		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current				52	mA	V_{CC} = MAX	

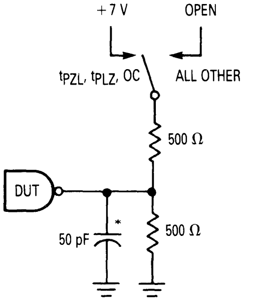
NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54F/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100		60		85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{\text{PE}}$ HIGH or LOW)	3.0 4.0	8.5 11.5	3.0 4.0	10.5 14	3.0 4.0	9.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{\text{TC}}$ (F168)	5.5 4.0	15.5 11	5.5 4.0	18 13.5	5.5 4.0	17 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{\text{TC}}$ (F169)	5.0 4.0	15.5 11	5.0 4.0	18 13.5	5.0 4.0	17 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CET}}$ to $\overline{\text{TC}}$	2.5 2.5	6.0 8.0	2.5 2.5	8.0 10	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{\text{D}}$ to $\overline{\text{TC}}$ (F168)	3.5 4.0	11 16	3.5 4.0	13.5 18.5	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{\text{D}}$ to $\overline{\text{TC}}$ (F169)	3.5 4.0	11 10.5	3.5 4.0	13.5 13	3.5 4.0	12.5 12	ns

AC OPERATING REQUIREMENTS

		54F/74F		54F		74F		
SYMBOL	PARAMETER	T_A = +25°C V_{CC} = +5.0 V		T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10%		T_A = 0°C to +70°C V_{CC} = 5.0 V ± 10%		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		5.5 5.5		4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0		7.0 7.0		6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0		0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0		10 10		9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW (F168) $U/\overline{D}$ to CP	11 16.5		13.5 19		12.5 18		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW (F169) $U/\overline{D}$ to CP	11 7.0		13.5 9.0		12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW $U/\overline{D}$ to CP	0 0		0 0		0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0		8.0 8.0		5.5 5.5		ns


+7 V
OPEN
tPZL, tPLZ, OC
ALL OTHER
500 Ω
DUT
*
50 pF
500 Ω

*INCLUDES JIG AND PROBE CAPACITANCE

FIGURE 1 — TEST LOAD

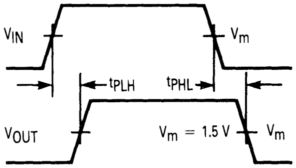

VIN
Vm
tPLH
tPHL
VOUT
Vm = 1.5 V
Vm

FIGURE 2 — WAVEFORM FOR NON-INVERTING FUNCTIONS

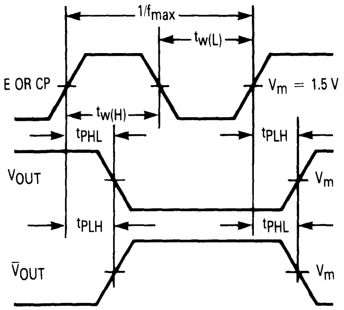

1/fmax
tw(L)
E OR CP
Vm = 1.5 V
tw(H)
tPHL
tPLH
VOUT
Vm
tPLH
tPHL
V̄OUT
Vm

FIGURE 3 — PROPAGATION DELAYS FROM RISING-EDGE CLOCK OR ENABLE

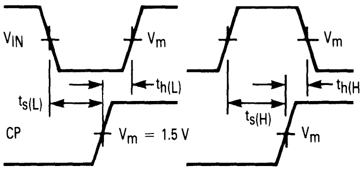

VIN
Vm
th(L)
ts(L)
CP
Vm = 1.5 V
Vm
th(H)
ts(H)
Vm

FIGURE 4 — SETUP AND HOLD TIMES, RISING-EDGE CLOCK

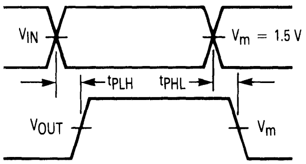

VIN
Vm = 1.5 V
tPLH
tPHL
VOUT
Vm

FIGURE 5 — WHETHER RESPONSE IS INVERTING OR NON-INVERTING DEPENDS ON SPECIFIC TRUTH TABLE CONDITIONS

MOTOROLA

MC54F/74F174

HEX D FLIP-FLOP WITH MASTER RESET

FAST™ SCHOTTKY TTL

HEX D FLIP-FLOP WITH MASTER RESET

DESCRIPTION — The MC54F/74F174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

The 'F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

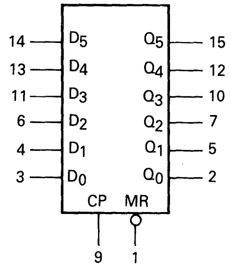
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**

TRUTH TABLE

INPUTS	OUTPUTS
@ t_n, $\overline{MR}$ = H	@ t_{n+1}
D_n	Q_n
H L	H L

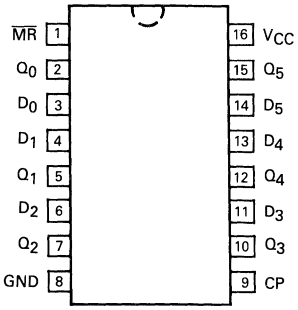
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL



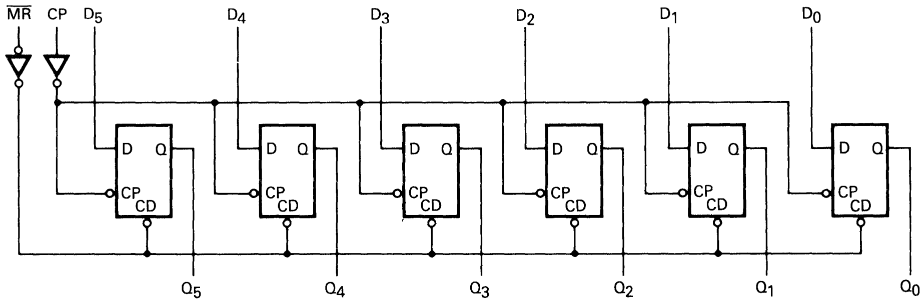
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OL} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			30	45	mA	V_{CC} = MAX, D_n = $\overline{MR}$ = 4.5 V, CP = ⎍	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100	140		80		80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 4.5	5.5 7.0	8.0 10	3.5 4.5	10.0 12.0	3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	10	14	5.0	16.0	5.0	15.0	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW D_n to CP	4.0 4.0			4.0 4.0		4.0 4.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	0 0			1.0 1.0		0 0		
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.0 6.0			4.0 6.0		4.0 6.0		ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0			5.0		5.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0			5.0		5.0		ns

AC TEST CIRCUIT

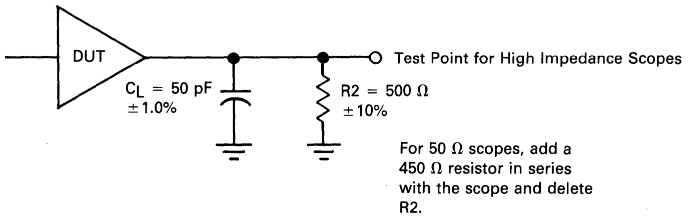

DUT
Test Point for High Impedance Scopes
C_L = 50 pF
±1.0%
R2 = 500 Ω
±10%
For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete
R2.

Fig. 1

MOTOROLA

MC54F/74F175

QUAD D FLIP-FLOP

QUAD D FLIP-FLOP

FAST™ SCHOTTKY TTL

DESCRIPTION — The MC54F/74F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**

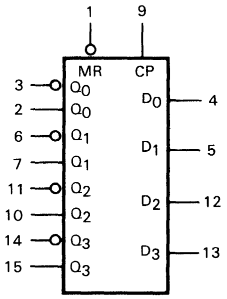
FUNCTIONAL DESCRIPTION — The F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and Q outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and Q outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

INPUTS	OUTPUTS	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

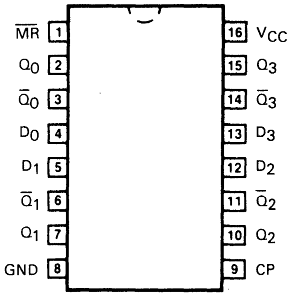
t_n = Bit time before clock positive-going transition
t_{n+1} = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL


1
9
MR
CP
3
2
6
7
11
10
14
15
$\overline{Q}_0$
Q_0
$\overline{Q}_1$
Q_1
$\overline{Q}_2$
Q_2
$\overline{Q}_3$
Q_3
D_0
D_1
D_2
D_3
4
5
12
13

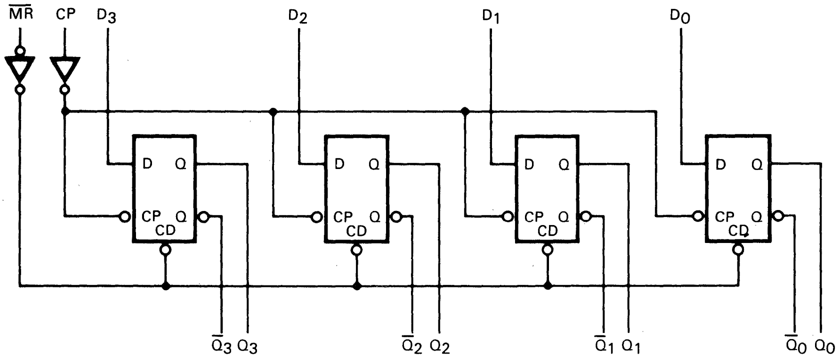
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM


$\overline{MR}$ 1
Q_0 2
$\overline{Q}_0$ 3
D_0 4
D_1 5
$\overline{Q}_1$ 6
Q_1 7
GND 8
16 V_{CC}
15 Q_3
14 $\overline{Q}_3$
13 D_3
12 D_2
11 $\overline{Q}_2$
10 Q_2
9 CP

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.50$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	V_{CC} = MAX
I_{IL}	Input LOW Current				-0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			22.5	34	mA	$D_n = \overline{MR} = 4.5$ V CP = _┌	V_{CC} = Max

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V $\pm10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V $\pm$ 10% $C_L = 50$ pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100	140		100		100		MHz
t_{PLH}	Propagation Delay	3.5	5.0	6.5	3.5	8.5	3.5	7.5	ns
t_{PHL}	CP to Q_n or $\overline{Q}_n$	4.0	6.5	8.5	4.0	10.5	4.0	9.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	9.0	11.5	4.5	15	4.5	13	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.5	4.0	10	4.0	9.0	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V $\pm10\%$		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V $\pm$ 10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Set up Time, HIGH or LOW	3.0			3.0		3.0		ns
t_s (L)	D_n to CP	3.0			3.0		3.0		
t_h (H)	Hold Time, HIGH or LOW	1.0			1.0		1.0		
t_h (L)	D_n to CP	1.0			1.0		1.0		
t_w (H)	CP Pulse Width, HIGH	4.0			4.0		4.0		ns
t_w (L)	or LOW	5.0			5.0		5.0		
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0			5.0		5.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0			5.0		5.0		ns

MOTOROLA

MC54F/74F181

Advance Information

4-BIT ARITHMETIC LOGIC UNIT

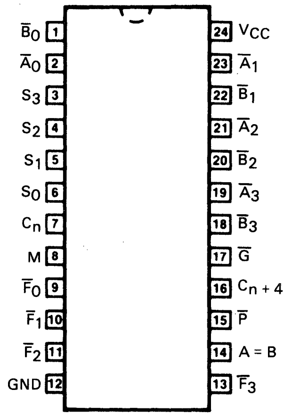
4-BIT ARITHMETIC LOGIC UNIT

FAST™ SCHOTTKY TTL

DESCRIPTION — The MC54F/74F181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

- **PROVIDES 16 ARITHMETIC OPERATIONS ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS**
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS**
- **FULL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION ON LONG WORDS**

CONNECTION DIAGRAM


$\overline{B}_0$ 1
$\overline{A}_0$ 2
S_3 3
S_2 4
S_1 5
S_0 6
C_n 7
M 8
$\overline{F}_0$ 9
$\overline{F}_1$ 10
$\overline{F}_2$ 11
GND 12
24 V_{CC}
23 $\overline{A}_1$
22 $\overline{B}_1$
21 $\overline{A}_2$
20 $\overline{B}_2$
19 $\overline{A}_3$
18 $\overline{B}_3$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A = B
13 $\overline{F}_3$

N Suffix — Case 724-02
(Plastic)

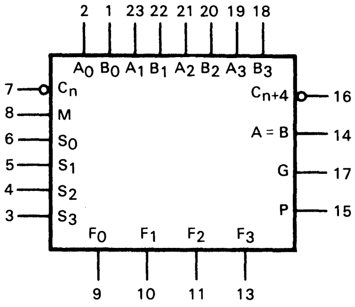
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
V_{OH}	Output Voltage — High A = B output	54, 74			5.5	V
I_{OL}	Output Current — Low	54, 74			20	mA

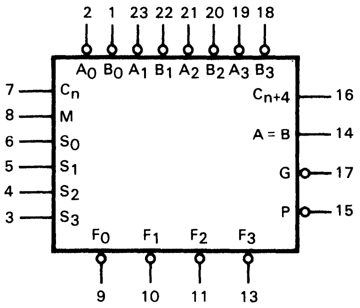
This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC SYMBOLS

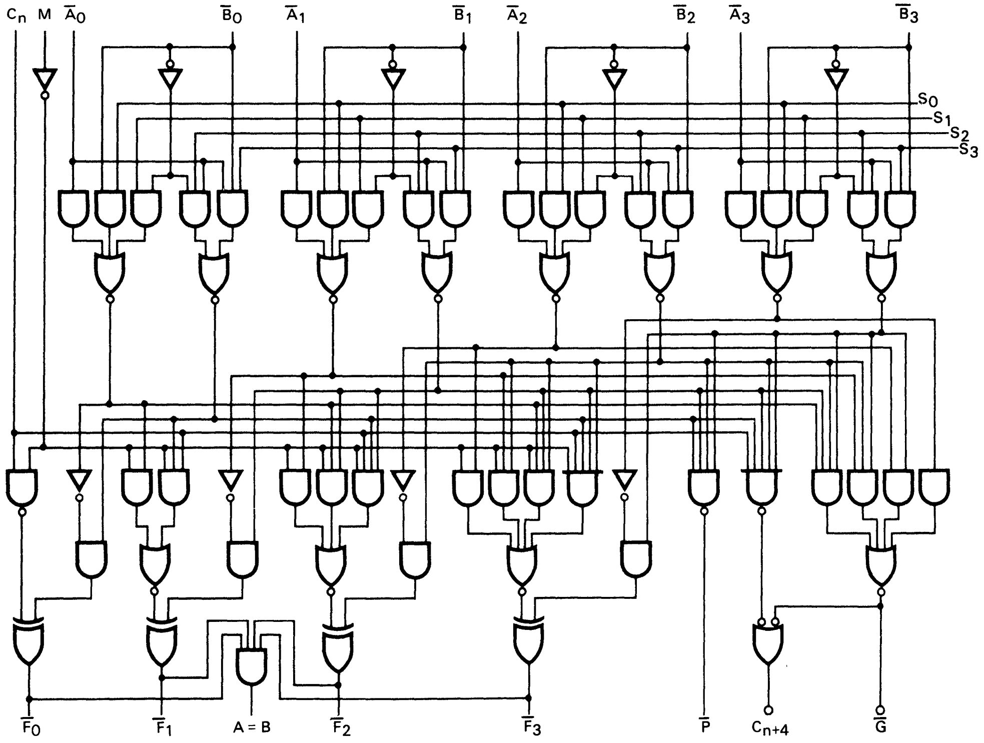
ACTIVE-HIGH OPERANDS


2 1 23 22 21 20 19 18
A0 B0 A1 B1 A2 B2 A3 B3
7 Cn
8 M
6 S0
5 S1
4 S2
3 S3
Cn+4 16
A = B 14
G 17
P 15
F0 F1 F2 F3
9 10 11 13

V_{CC} = Pin 24
GND = Pin 12


2 1 23 22 21 20 19 18
A0 B0 A1 B1 A2 B2 A3 B3
7 Cn
8 M
6 S0
5 S1
4 S2
3 S3
Cn+4 16
A = B 14
G 17
P 15
F0 F1 F2 F3
9 10 11 13

LOGIC DIAGRAM


Cn
M
Ā0
B̄0
Ā1
B̄1
Ā2
B̄2
Ā3
B̄3
S0
S1
S2
S3
F̄0
F̄1
A = B
F̄2
F̄3
P̄
Cn+4
Ḡ

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
I_{OH}	Output Current — HIGH				250	μA	V_{OH} = 5.5 V	V_{CC} = MIN, A=B
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	M Input			-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
		A and B Inputs			-1.8	mA		
		S_{0-3} Inputs			-2.4	mA		
		C_n Input			-3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			43	65	mA	V_{CC} = MAX	

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0–S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active—LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four F181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means $\overline{\text{borrow}}$; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

AC CHARACTERISTICS

SYMBOL	PARAMETER		54/74F		54F		74F		UNITS
			T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
	PATH	MODE	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n to C_{n+4}		3.0	8.5	3.0	10.5	3.0	9.5	ns
t_{PHL}			3.0	8.0	3.0	10	3.0	9.0	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	5.0	13	5.0	15	5.0	14	ns
t_{PHL}			5.0	12	5.0	14	5.0	13	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	5.0	14	5.0	16	5.0	15	ns
t_{PHL}			5.0	13	5.0	15	5.0	14	
t_{PLH}	C_n to $\overline{F}$	Any	3.0	8.5	3.0	10.5	3.0	9.5	ns
t_{PHL}			3.0	8.5	3.0	10.5	3.0	9.5	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Sum	3.0	7.5	3.0	9.5	3.0	8.5	ns
t_{PHL}			3.0	7.5	3.0	9.5	3.0	8.5	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	3.0	8.5	3.0	10.5	3.0	9.5	ns
t_{PHL}			3.0	9.5	3.0	11.5	3.0	10.5	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	3.0	7.0	3.0	9.0	3.0	8.0	ns
t_{PHL}			3.0	7.5	3.0	9.5	3.0	8.5	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	4.0	7.5	4.0	9.5	4.0	8.5	ns
t_{PHL}			3.5	8.5	3.5	10.5	3.5	9.5	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3.0	9.0	3.0	11	3.0	10	ns
t_{PHL}			3.0	10	3.0	11	3.0	10	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Dif	3.0	11	3.0	13	3.0	12	ns
t_{PHL}			3.0	11	3.0	13	3.0	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0	10.5	4.0	12.5	4.0	11.5	ns
t_{PHL}			4.0	10	4.0	12	4.0	11	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	4.5	12	4.5	14	4.5	13	ns
t_{PHL}			4.5	12	4.5	14	4.5	13	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	4.0	9.0	4.0	11	4.0	10	ns
t_{PHL}			4.0	10	4.0	12	4.0	11	
t_{PLH}	$\overline{A}$ or $\overline{B}$ to A = B	Dif	11	27	11	31	11	29	ns
t_{PHL}			7.0	12.5	7.0	14.5	7.0	13.5	

FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE-LOW OPERANDS & F_n OUTPUTS		ACTIVE-HIGH OPERANDS & F_n OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A} + B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.

H = HIGH Voltage Level
L = LOW Voltage Level

MOTOROLA

MC54F/74F182

CARRY LOOKAHEAD GENERATOR

CARRY LOOKAHEAD GENERATOR

FAST™ SCHOTTKY TTL

DESCRIPTION — The MC54F/74F182 is a high-speed carry lookahead generator. It is generally used with the F181, F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

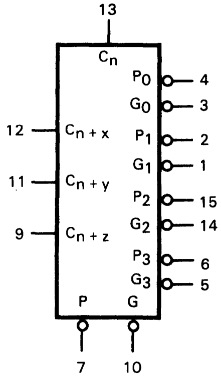
- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALUs**
- **MULTI-LEVEL LOOKAHEAD HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

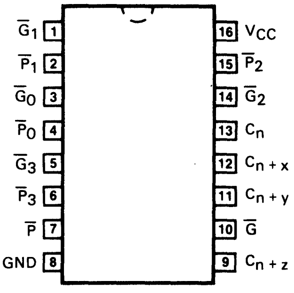
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC SYMBOL


13
C_n
P_0 4
G_0 3
12 C_{n+x}
P_1 2
G_1 1
11 C_{n+y}
P_2 15
G_2 14
9 C_{n+z}
P_3 6
G_3 5
P
G
7
10

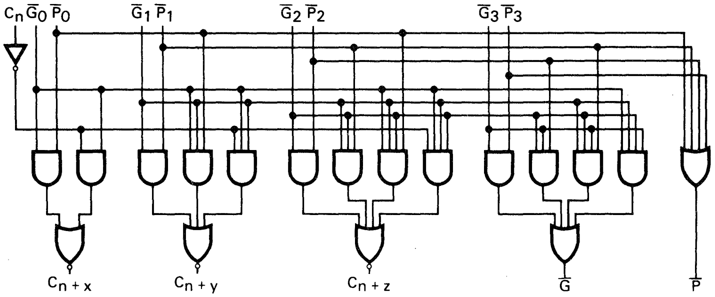
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM


$\overline{G}_1$ 1
$\overline{P}_1$ 2
$\overline{G}_0$ 3
$\overline{P}_0$ 4
$\overline{G}_3$ 5
$\overline{P}_3$ 6
$\overline{P}$ 7
GND 8
16 V_{CC}
15 $\overline{P}_2$
14 $\overline{G}_2$
13 C_n
12 C_{n+x}
11 C_{n+y}
10 $\overline{G}$
9 C_{n+z}

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

LOGIC DIAGRAM


C_n $\overline{G}_0$ $\overline{P}_0$
$\overline{G}_1$ $\overline{P}_1$
$\overline{G}_2$ $\overline{P}_2$
$\overline{G}_3$ $\overline{P}_3$
C_{n+x}
C_{n+y}
C_{n+z}
$\overline{G}$
$\overline{P}$

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7.0 V	V_{CC} = MAX
I_{IL}	Input LOW Current	C_n Input			-1.2	mA	V_{IN} = 0.5 V	V_{CC} = MAX
		$\overline{P}_3$ Input			-2.4			
		$\overline{P}_2$ Input			-3.6			
		$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$ Inputs			-4.8			
		$\overline{G}_0$, $\overline{G}_2$ Inputs			-8.4			
		$\overline{G}_1$ Input			-9.6			
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current (All Outputs HIGH)			18.4	28	mA	$\overline{P}_3$, $\overline{G}_3$ = 4.5 V All Other Inputs = GND	V_{CC} = MAX
I_{CCL}	Power Supply Current (All Outputs LOW)			23.5	36	mA	$\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ = 4.5 V All Other Inputs = GND	V_{CC} = MAX

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			54F $T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		74F $T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	3.0 3.0	6.6 6.8	8.5 9.0	3.0 3.0	10.5 11	3.0 3.0	9.5 10	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	2.5 1.5	6.2 3.7	8.0 5.0	2.5 1.5	10.7 6.5	2.5 1.5	9.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	2.5 1.5	6.5 3.9	8.5 5.2	2.5 1.5	10.5 6.5	2.5 1.5	9.5 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	2.0 2.0	7.9 6.0	10 8.0	2.0 2.0	12.5 9.5	2.0 2.0	11 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$	2.0 1.5	8.3 5.7	10.5 7.5	2.0 1.5	12.5 9.5	2.0 1.5	11.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$	2.5 2.5	5.7 4.1	7.5 5.5	2.5 2.5	11 7.5	2.5 2.5	8.5 6.5	ns

FUNCTIONAL DESCRIPTION — The F182 carry lookahead generator accepts up to four pairs of active-LOW Carry Propagate ($\overline{P}_0$–$\overline{P}_3$) and Carry Generate ($\overline{G}_0$–$\overline{G}_3$) signals and an active-HIGH Carry input (C_n) and provides anticipated active-HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The F182 also has active-LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the output are:

$C_{n+x} = G_0 + P_0C_n$

$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$

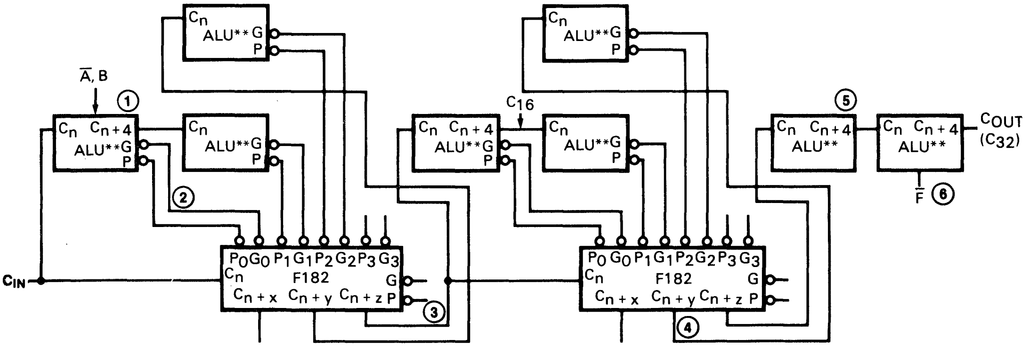
$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$

$\overline{P} = \overline{P_3P_2P_1P_0}$

Also, the F182 can be used with binary ALUs in an active-LOW or active-HIGH input operand mode. The connections (Figure A) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last F181 or F381.

FIGURE A — 32-Bit ALU with Ripple Carry between 16-Bit Lookahead ALUs



**ALUs may be either F181, F381 or 2901A.

MOTOROLA

MC54F/74F190

Product Preview

UP/DOWN DECADE COUNTER
(With Preset and Ripple Clock)

DESCRIPTION — The MC54F/74F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH-SPEED — 110 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

$\overline{RC}$ TRUTH TABLE

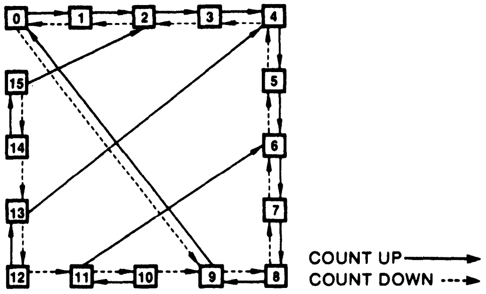
INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

STATE DIAGRAM

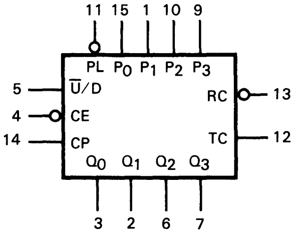

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
COUNT UP
COUNT DOWN

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

UP/DOWN DECADE COUNTER
(With Preset and Ripple Clock)

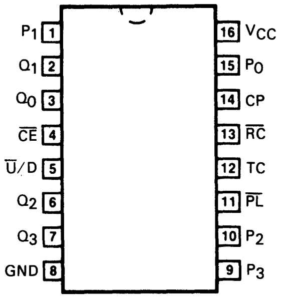
FAST™ SCHOTTKY TTL

LOGIC SYMBOL


11 15 1 10 9
PL P0 P1 P2 P3
5
U/D
4
CE
14
CP
RC
13
TC
12
Q0 Q1 Q2 Q3
3 2 6 7

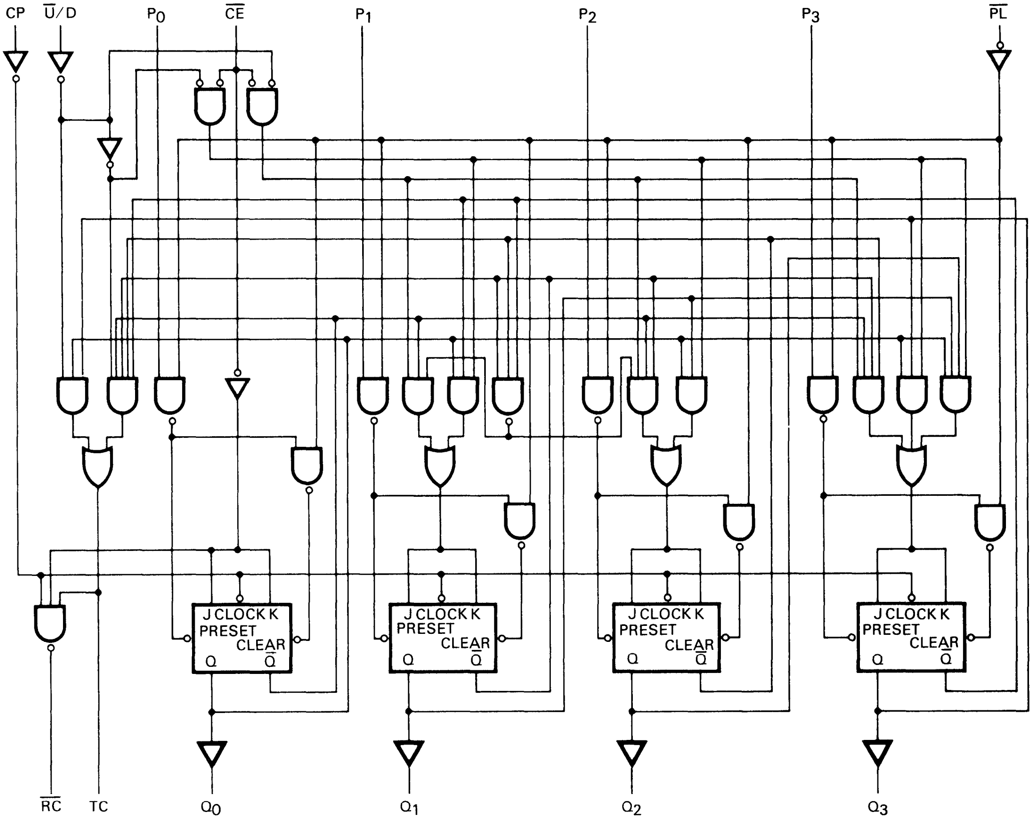
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM


P1 1
Q1 2
Q0 3
CE 4
U/D 5
Q2 6
Q3 7
GND 8
16 VCC
15 P0
14 CP
13 RC
12 TC
11 PL
10 P2
9 P3

J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

LOGIC DIAGRAM


CP
U/D
P0
CE
P1
P2
P3
PL
J CLOCK K
PRESET
CLEAR
Q
Q
RC
TC
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

FUNCTIONAL DESCRIPTION — The F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{\text{PL}}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the $\overline{\text{CE}}$ input inhibits counting. When $\overline{\text{CE}}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{\text{U}}$/D input signal, as indicated in the Mode Select Table. $\overline{\text{CE}}$ and $\overline{\text{U}}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{\text{U}}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ($\overline{\text{RC}}$) output. The $\overline{\text{RC}}$ output is normally HIGH. When $\overline{\text{CE}}$ is LOW and TC is HIGH, the $\overline{\text{RC}}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the F191 data sheet.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	$I_{IN} = -18$ mA	$V_{CC} =$ MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.50$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	$V_{CC} =$ MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	$V_{CC} =$ MAX
					100	μA	$V_{IN} = 7.0$ V	$V_{CC} =$ MAX
I_{IL}	Input LOW Current Other Inputs				-0.6	mA	$V_{IN} = 0.5$ V	$V_{CC} =$ MAX
	$\overline{\text{CE}}$ Input				-1.8			
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	$V_{OUT} = 0$ V	$V_{CC} =$ MAX
I_{CC}	Power Supply Current			38	55	mA	$V_{CC} =$ MAX	

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Count Frequency	80	110		80		80		MHz
t_{PLH}	Propagation Delay	3.0	5.5	9.0	3.0	12.5	3.0	10	ns
t_{PHL}	CP to Q_n	3.0	6.5	10	3.0	14	3.0	11	
t_{PLH}	Propagation Delay	8.0	12.5	16	8.0	22.5	8.0	17	ns
t_{PHL}	CP to TC	5.0	9.5	13	5.0	18	5.0	14	
t_{PLH}	Propagation Delay	4.0	7.0	9.5	4.0	13.5	4.0	10.5	ns
t_{PHL}	CP to $\overline{RC}$	3.0	5.0	8.0	3.0	11	3.0	9.0	
t_{PLH}	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	ns
t_{PHL}	$\overline{CE}$ to $\overline{RC}$	3.0	4.5	7.0	3.0	10	3.0	8.0	
t_{PLH}	Propagation Delay	7.0	11	18	7.0	25.5	7.0	19	ns
t_{PHL}	$\overline{U}$/D to $\overline{RC}$	5.0	9.0	12	5.0	17	5.0	13	
t_{PLH}	Propagation Delay	3.0	6.0	11	3.0	15.5	3.0	12	ns
t_{PHL}	$\overline{U}$/D to TC	3.0	6.5	11	3.0	15.5	3.0	12	
t_{PLH}	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	ns
t_{PHL}	P_n to Q_n	8.0	13.4	17	8.0	24	8.0	18	
t_{PLH}	Propagation Delay	3.0	6.7	11	3.0	15.5	3.0	12	ns
t_{PHL}	$\overline{PL}$ to Q_n	4.0	7.2	15	4.0	21	4.0	16	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ± 10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Set up Time, HIGH or LOW	5.0			5.0		5.0		ns
t_s (L)	P_n to $\overline{PL}$	8.0			8.0		8.0		
t_h (H)	Hold Time, HIGH or LOW	3.0			3.0		3.0		
t_h (L)	P_n to $\overline{PL}$	3.0			3.0		3.0		
t_s (L)	Set up Time LOW $\overline{CE}$ to CP	10			10		10		ns
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0			0		0		
t_w (L)	$\overline{PL}$ Pulse Width, LOW	6.0			6.0		6.0		ns
t_w (L)	CP Pulse Width LOW	6.0			6.0		6.0		ns
t_{rec}	Recovery Time $\overline{PL}$ to CP	7.0			7.0		7.0		ns

MOTOROLA

MC54F/74F191

UP/DOWN BINARY COUNTER
(With Preset and Ripple Clock)

FAST™ SCHOTTKY TTL

Product Preview

UP/DOWN BINARY COUNTER
(With Preset and Ripple Clock)

DESCRIPTION — The MC54F/74F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH-SPEED — 110 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

FUNCTIONAL DESCRIPTION — The F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

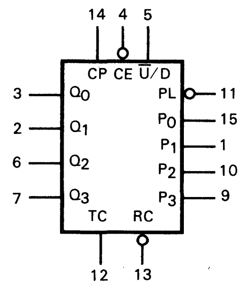
INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RC TRUTH TABLE

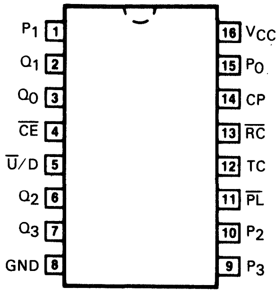
INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION (continued)

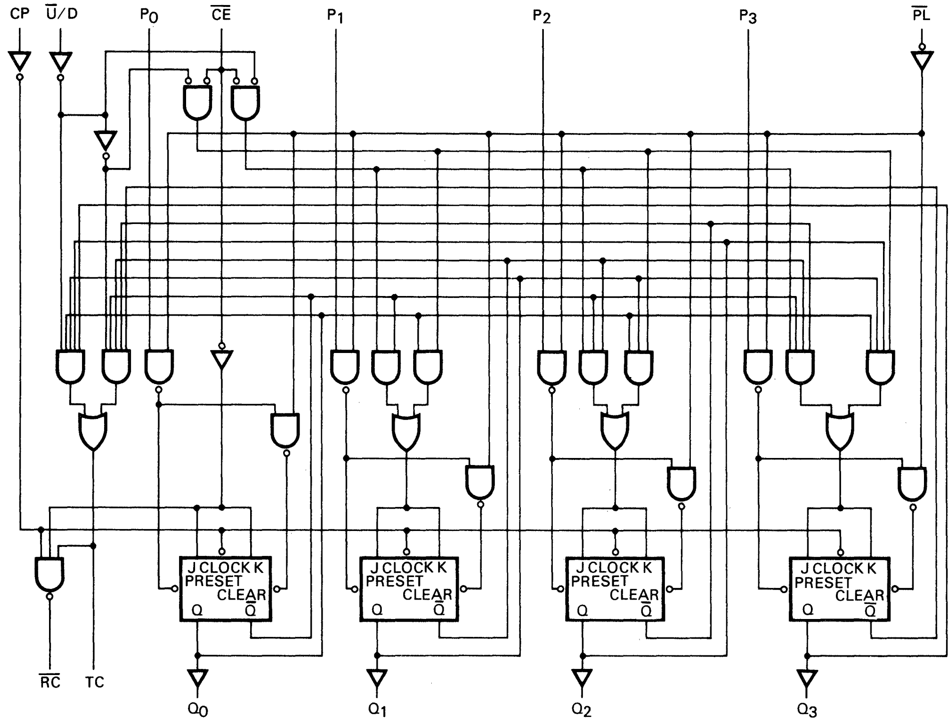
Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{\text{U}}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{\text{RC}}$) output. The $\overline{\text{RC}}$ output is normally HIGH. When $\overline{\text{CE}}$ is LOW and TC is HIGH, the $\overline{\text{RC}}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{\text{RC}}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{\text{CE}}$ inhibits the $\overline{\text{RC}}$ output pulse, as indicated in the $\overline{\text{RC}}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure B. All clock inputs are driven in parallel and the $\overline{\text{RC}}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{\text{RC}}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure C avoids ripple delays and their associated restrictions. The $\overline{\text{CE}}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures A and B doesn't apply, because the TC output of a given stage is not affected by its own $\overline{\text{CE}}$.

LOGIC DIAGRAM


CP
U/D
P0
CE
P1
P2
P3
PL
J CLOCK K
PRESET
CLEAR
Q
Q
RC
TC
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

FIGURE A — N-Stage Counter Using Ripple Clock

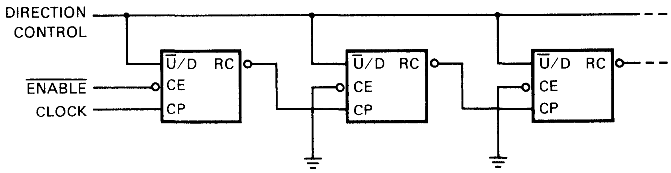

DIRECTION CONTROL
$\overline{\text{ENABLE}}$
CLOCK
$\overline{\text{U}}$/D RC
CE
CP
$\overline{\text{U}}$/D RC
CE
CP
$\overline{\text{U}}$/D RC
CE
CP

FIGURE B — Synchronous N-Stage Counter Using Ripple Carry/Borrow

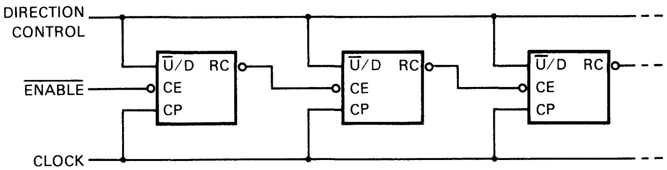
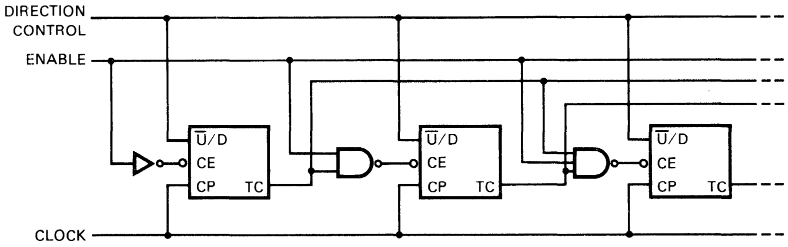

DIRECTION CONTROL
$\overline{\text{ENABLE}}$
CLOCK
$\overline{\text{U}}$/D RC
CE
CP
$\overline{\text{U}}$/D RC
CE
CP
$\overline{\text{U}}$/D RC
CE
CP

FIGURE C — Synchronous N-Stage Counter with Parallel Gated Carry/Borrow


DIRECTION CONTROL
ENABLE
CLOCK
$\overline{\text{U}}$/D
CE
CP TC
$\overline{\text{U}}$/D
CE
CP TC
$\overline{\text{U}}$/D
CE
CP TC

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Other Inputs				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
	$\overline{CE}$ Input				-1.8			
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			38	55	mA	V_{CC} = MAX	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Count Frequency	80	110		80		80		MHz
t_{PLH}	Propagation Delay CP to Q_n	3.0	5.5	9.0	3.0	12.5	3.0	10	ns
t_{PHL}		3.0	6.5	10	3.0	14	3.0	11	
t_{PLH}	Propagation Delay CP to TC	8.0	12.5	16	8.0	22.5	8.0	17	ns
t_{PHL}		5.0	9.5	13	5.0	18	5.0	14	
t_{PLH}	Propagation Delay CP to $\overline{RC}$	4.0	7.0	9.5	4.0	13.5	4.0	10.5	ns
t_{PHL}		3.0	5.0	8.0	3.0	11	3.0	9.0	
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.0	4.6	7.0	3.0	10	3.0	8.0	ns
t_{PHL}		3.0	4.5	7.0	3.0	10	3.0	8.0	
t_{PLH}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	7.0	11	18	7.0	25.5	7.0	19	ns
t_{PHL}		5.0	9.0	12	5.0	17	5.0	13	
t_{PLH}	Propagation Delay $\overline{U}$/D to TC	3.0	6.0	11	3.0	15.5	3.0	12	ns
t_{PHL}		3.0	6.5	11	3.0	15.5	3.0	12	
t_{PLH}	Propagation Delay P_n to Q_n	3.0	4.6	7.0	3.0	10	3.0	8.0	ns
t_{PHL}		8.0	13.4	17	8.0	24	8.0	18	
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.0	6.7	11	3.0	15.5	3.0	12	ns
t_{PHL}		4.0	7.2	15	4.0	21	4.0	16	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ± 10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Set up Time, HIGH or LOW P_n to $\overline{PL}$	5.0			5.0		5.0		ns
t_s (L)		8.0			8.0		8.0		
t_h (H)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0			3.0		3.0		
t_h (L)		3.0			3.0		3.0		
t_s (L)	Set up Time LOW $\overline{CE}$ to CP	10			10		10		ns
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0			0		0		
t_w (L)	$\overline{PL}$ Pulse Width, LOW	6.0			6.0		6.0		ns
t_w (L)	CP Pulse Width LOW	6.0			6.0		6.0		ns
t_{rec}	Recovery Time $\overline{PL}$ to CP	7.0			7.0		7.0		ns

MOTOROLA

MC54F/74F192
MC54F/74F193

Product Preview

UP/DOWN COUNTERS WITH SEPARATE UP/DOWN CLOCKS

DESCRIPTION — The MC54F/74F192 is an up/down BCD decade (8241) counter. The MC54F/74193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

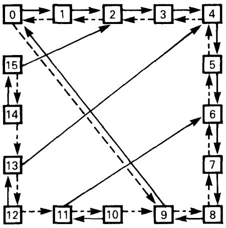
FUNCTION TABLE

MR

	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAMS


F192

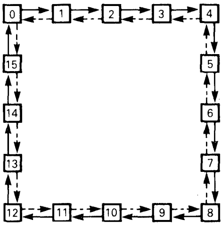
F192 Logic Equations for Terminal Count

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$
$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

F193 Logic Equations for Terminal Count

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$
$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

Count Up ——▶
Count Down - - -▶

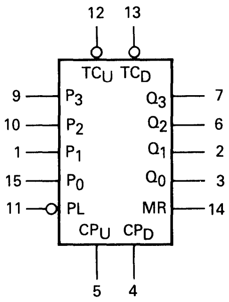

F193

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

UP/DOWN COUNTERS WITH SEPARATE UP/DOWN CLOCKS

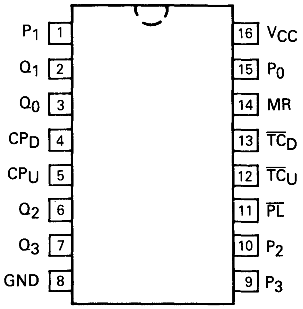
FAST™ **SCHOTTKY TTL**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

FUNCTIONAL DESCRIPTION

The 'F192, 193 are asynchronously presettable counters. The 'F192 is a decade counter while the 'F193 is organized for 4-bit binary operation. They both contain four edge triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state; 9 ('F192) or 16 ('F193), the reset HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Both the 'F192 and the 'F193 have an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0–P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

*74F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = MIN
		74	2.7			V	I_{OL} = −1.0 mA	
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current ($\overline{MR}$, $\overline{PL}$ and P_n inputs)				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
	(CP inputs)				−1.2			
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			38	55	mA	V_{CC} = MAX	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

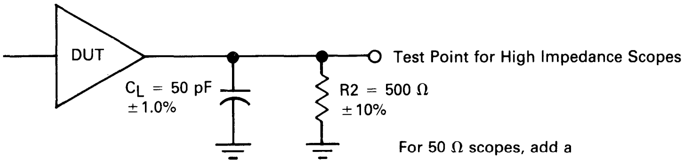
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Count Frequency	100	125				90		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$	4.0 3.5	7.0 6.0	9.0 8.0			4.0 3.5	10 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n	4.0 5.5	6.5 9.5	8.5 12.5			4.0 5.5	9.5 13.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 6.0	4.5 11	7.0 14.5			3.0 6.0	8.0 15.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	5.0 5.5	8.5 10	11 13			5.0 5.5	12 14	ns
t_{PHL}	Propagation Delay MR to Q_n	6.5	11	14.5			6.5	15.5	ns
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	6.0	10.5	13.5			6.0	14.5	
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	7.0	11.5	14.5			7.0	15.5	
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to TC_U or $\overline{TC}_D$	7.0 7.0	12 11.5	15.5 14.5			7.0 7.0	16.5 15.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 6.5	11.5 11	14.5 14			7.0 6.5	15.5 15	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW P_n to $\overline{PL}$	6.0 6.0					6.0 6.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	4.0 4.0					4.0 4.0		
t_w (L)	$\overline{PL}$ Pulse Width LOW	6.0					6.0		ns
t_w (L)	CP_U or CP_D Pulse Width LOW	5.0					5.0		ns
t_w (L)	CP_U or CP_D Pulse Width LOW (Change of Direction)	10					10		ns
t_w (H)	MR Pulse Width HIGH	6.0					6.0		ns
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	6.0					6.0		ns
t_{rec}	Recovery Time MR to CP_U or CP_D	4.0					4.0		ns

AC TEST CIRCUIT



For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

MC54F/74F194

Advance Information

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION — The MC54F/74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The F194 is similar in operation to the S195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- **TYPICAL SHIFT FREQUENCY OF 150 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**

FUNCTIONAL DESCRIPTION — The F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0-P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H H	h h	l l	X X	l h	X X	q_1 q_1	q_2 q_2	q_3 q_3	L H
Shift Right	H H	l l	h h	l h	X X	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

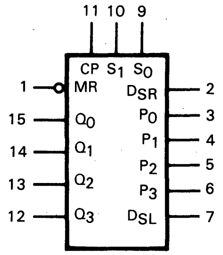
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

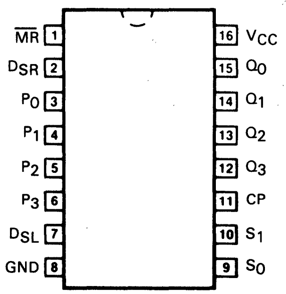
FAST™ SCHOTTKY TTL

LOGIC SYMBOL



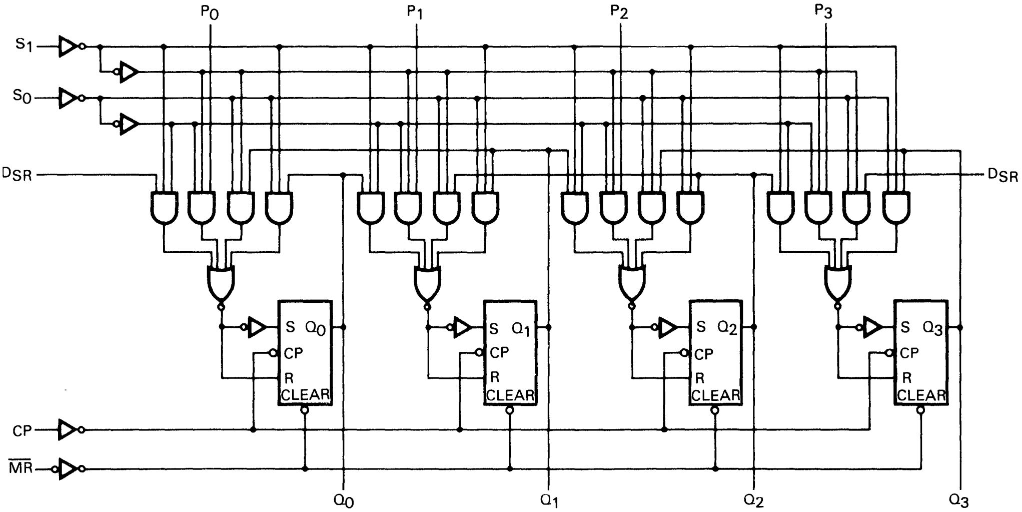
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09
(Ceramic)
N Suffix — Case 648-08
(Plastic)
D Suffix — Case 751B-03
(SOIC)

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.50$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				-0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			33	46	mA	S_n, $\overline{MR}$, D_{SR}, $D_{SL} = 4.5$ V P_n = Gnd, CP = ⎍	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Shift Frequency	105		80		90		MHz
t_{PLH}	Propagation Delay CP to Q_n	3.0	7.0	3.0	8.5	3.5	8.0	ns
t_{PHL}		3.5	7.5	3.0	8.5	3.5	8.0	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	12	4.5	14.5	4.5	14	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V		T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Set up Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	4.0		4.0		4.0		ns
t_s (L)		4.0		4.0		4.0		
t_h (H)	Hold Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	0		1.0		1.0		
t_h (L)		0		1.0		1.0		
t_s (H)	Set up Time, HIGH or LOW S_n to CP	8.0		9.0		9.0		ns
t_s (L)		8.0		8.0		8.0		
t_h (H)	Hold Time, HIGH or LOW S_n to CP	0		0		0		
t_h (L)		0		0		0		
t_w (H)	CP Pulse Width HIGH	5.0		5.5		5.5		ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0		5.0		5.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0		9.0		8.0		ns

MOTOROLA

MC54F/74F240
MC54F/74F241
MC54F/74F244

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

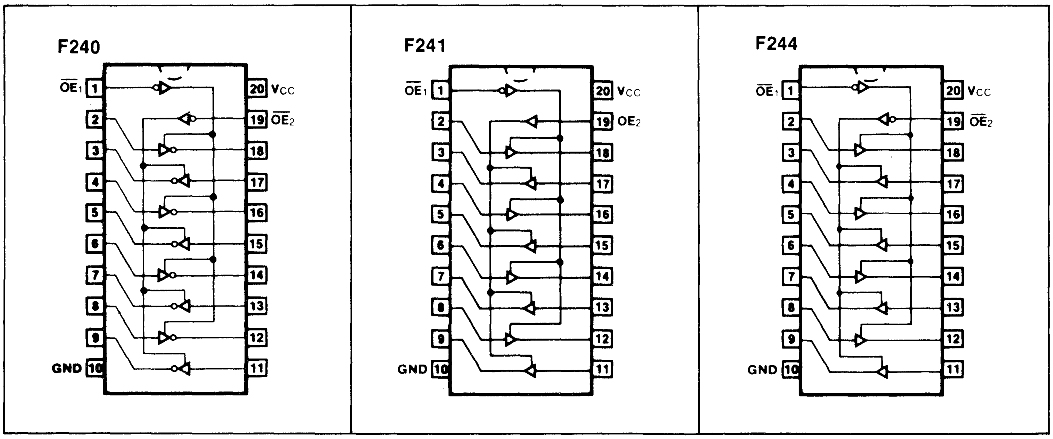
DESCRIPTION — The F240, F241 and F244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density.

- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- OUTPUTS SINK 64 mA
- 15 mA SOURCE CURRENT
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

OCTAL BUFFER/LINE DRIVER with 3-STATE OUTPUTS

FAST™ SCHOTTKY TTL

CONNECTION DIAGRAMS



J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

TRUTH TABLES

F240

INPUTS		OUTPUT
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	H
L	H	L
H	X	Z

F241

INPUTS			OUTPUT
$\overline{OE}_1$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

F244

INPUTS		OUTPUT
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impendance

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			-12 -15	mA
I_{OL}	Output Current — Low	54 74			48 64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	I_{OH} = -3.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -3.0 mA	V_{CC} = 4.75 V
		54	2.0			V	I_{OH} = -12 mA	V_{CC} = 4.50 V
		74	2.0			V	I_{OH} = -15 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	54			0.55	V	I_{OL} = 48 mA	V_{CC} = MIN
		74			0.55	V	I_{OL} = 64 mA	
I_{OZH}	Output Off Current HIGH				50	µA	V_{OUT} = 2.7V	V_{CC} = MAX
I_{OZL}	Output Off Current LOW				-50	µA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	Data Inputs F241, F244			-1.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
		Other			-1.0			
I_{OS}	Output Drive Current Note 2	54	-100		-275	mA	V_{OUT} = GND	V_{CC} = MAX
		74	-100		-275			
I_{CCH}	Power Supply Current HIGH	F240			35	mA	V_{CC} = MAX	
		F241,F244			60			
I_{CCL}	Power Supply Current LOW	F240			75			
		F241,F244			90			
I_{CCZ}	Power Supply Current OFF	F240			75			
		F241,F244			90			

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

F240
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10% C_L = 50 pF		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output	2.5 1.5	5.1 3.5	7.0 4.7	2.5 1.5	9.0 6.0	2.5 1.5	8.0 5.7	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 4.0	3.5 6.9	5.2 9.0	2.0 4.0	6.5 13.5	2.0 4.0	5.7 10	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.0 6.0	5.3 8.0	2.0 2.0	6.5 12.5	2.0 2.0	6.3 9.5	ns

F241
AC CHARACTERISTICS

t_{PLH} t_{PHL}	Propagation Delay, Data to Output	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.5 7.0	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	4.3 5.4	5.7 7.0	2.0 2.0	7.0 8.5	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.5 4.5	6.0 6.5	2.0 2.0	7.0 12.5	2.0 2.0	7.0 7.5	ns

F244
AC CHARACTERISTICS

t_{PLH} t_{PHL}	Propagation Delay, Data to Output	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.5 7.0	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	4.3 5.4	5.7 7.0	2.0 2.0	7.0 8.5	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.5 4.5	6.0 6.0	2.0 2.0	7.0 10.0	2.0 2.0	7.0 7.0	ns

MOTOROLA

MC54F/74F242
MC54F/74F243

QUAD BUS TRANSCEIVERS (WITH 3-STATE OUTPUTS) FAST™ SCHOTTKY TTL

QUAD BUS TRANSCEIVERS (with 3-State Outputs)

DESCRIPTION — The MC54F/74F242 and MC54F/74F243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communication between data buses.

- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

TRUTH TABLES
MC54F242/MC74F242

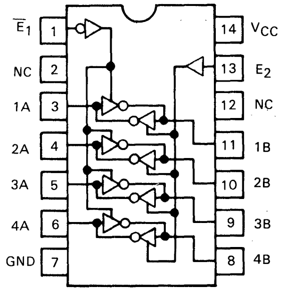
INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	H	L	X	(Z)
L	H	L	L	X	(Z)
H	X	(Z)	H	L	H
H	X	(Z)	H	H	L

MC54F243/MC74F243

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	L	L	X	(Z)
L	H	H	L	X	(Z)
H	X	(Z)	H	L	L
H	X	(Z)	H	H	H

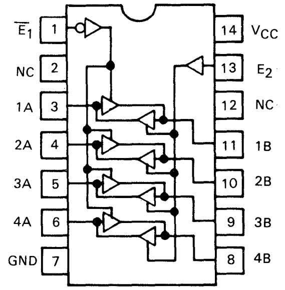
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

MC54F242/MC74F242
(TOP VIEW)



$\overline{E}_1$ 1
NC 2
1A 3
2A 4
3A 5
4A 6
GND 7
14 V_{CC}
13 E_2
12 NC
11 1B
10 2B
9 3B
8 4B

MC54F243/MC74F243
(TOP VIEW)



$\overline{E}_1$ 1
NC 2
1A 3
2A 4
3A 5
4A 6
GND 7
14 V_{CC}
13 E_2
12 NC
11 1B
10 2B
9 3B
8 4B

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			-12 -15	mA
I_{OL}	Output Current — Low	54 74			48 64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54	2.0			V	I_{OH} = -12 mA	V_{CC} = 4.50 V
		74	2.0			V	I_{OH} = -15 mA	V_{CC} = 4.50 V
		54, 74	2.4			V	I_{OH} = -3.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = -3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage	54			0.55	V	I_{OL} = 48 mA	V_{CC} = MIN
		74			0.55	V	I_{OL} = 64 mA	
I_{OZH}	Output Off Current HIGH				70	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
					1.0	mA	V_{OUT} = 5.5 V	
I_{OZL}	Output Off Current LOW				-1.6	mA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current	Enable			20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
		Data			70	μA	V_{IN} = 2.7 V	
		Data			1.0	mA	V_{IN} = 5.5 V	
		Enable			0.1	mA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	Enable			-1.0	mA	V_{IN} = 0.5 V	V_{CC} = MAX
		Data*			-1.6	mA	V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		-100		-275	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current HIGH	F242			60	mA	Outputs HIGH	V_{CC} = MAX
		F243			80	mA		
I_{CCL}	Power Supply Current LOW	F242			75	mA	Outputs LOW	V_{CC} = MAX
		F243			90	mA		
I_{CCZ}	Power Supply Current OFF	F242			75	mA	Outputs OFF	V_{CC} = MAX
		F243			90	mA		

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

F242
AC CHARACTERISTICS

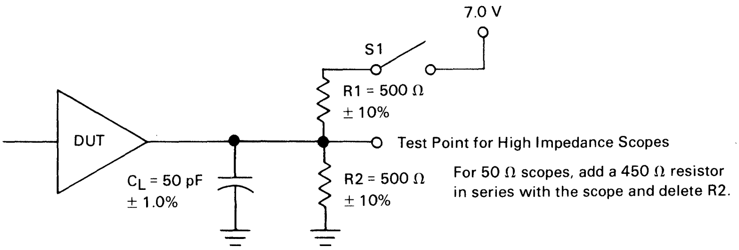
SYMBOL	PARAMETER	54F/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0°C to 70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay, Data to Output	2.5	7.0	2.5	9.0	2.5	8.0	ns
t_{PHL}		1.5	4.7	1.5	6.0	1.5	5.7	
t_{PZH}	Output Enable Time	2.0	4.7	2.0	6.5	2.0	5.7	ns
t_{PZL}		4.0	9.0	4.0	12	4.0	10	
t_{PHZ}	Output Disable Time	2.0	5.3	2.0	6.5	2.0	6.3	ns
t_{PLZ}		2.0	6.5	2.0	12.5	2.0	8.0	

F243
AC CHARACTERISTICS

t_{PLH}	Propagation Delay, Data to Output	2.5	5.2	2.0	6.5	2.0	6.2	ns
t_{PHL}		2.5	5.2	2.0	8.5	2.0	6.5	
t_{PZH}	Output Enable Time	2.0	5.7	2.0	8.0	2.0	6.7	ns
t_{PZL}		2.0	7.5	2.0	10.5	2.0	8.5	
t_{PHZ}	Output Disable Time	2.0	6.0	1.5	7.5	1.5	7.0	ns
t_{PLZ}		2.0	6.5	2.0	12.5	2.0	7.5	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

Fig. 1



For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

MOTOROLA

MC54F/74F245

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

DESCRIPTION — The F245 contains eight noninverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-Z condition.

- NONINVERTING BUFFERS
- BIDIRECTIONAL DATA PATH
- B OUTPUTS SINK 64 mA

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

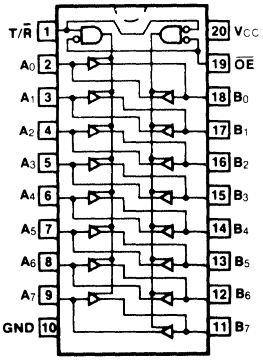
FAST™ SCHOTTKY TTL

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CONNECTION DIAGRAM



J Suffix — Case 732-03
(Ceramic)
N Suffix — Case 738-03
(Plastic)
DW Suffix — Case 751D-03
(SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range		54	-55	25	125	°C
			74	0	25	70	
I_{OH}	Output Current — High	An Outputs	54, 74			-3.0	mA
I_{OL}	Output Current — Low	An Outputs	54, 74			20	mA
I_{OH}	Output Current — High	Bn Outputs	54			-12	mA
			74			-15	
I_{OL}	Output Current — Low	Bn Outputs	54			48	mA
			74			64	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage An Outputs	54, 74	2.4	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$
		74	2.7	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$
V_{OH}	Output HIGH Voltage Bn Outputs	54, 74	2.4	3.4		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$
		74	2.7	3.4		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$
		54	2.0			V	$I_{OH} = -12$ mA	$V_{CC} = 4.5$
		74	2.0			V	$I_{OH} = -15$ mA	
V_{OL}	Output LOW Voltage An Outputs	54		0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
		74		0.35	0.5	V	$I_{OL} = 24$ mA	
V_{OL}	Output LOW Voltage Bn Outputs	54			0.55	V	$I_{OL} = 48$ mA	V_{CC} = MIN
		74			0.55	V	$I_{OL} = 64$ mA	
I_{OZH}	Output Off Current HIGH				70	µA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
					1.0	mA	$V_{OUT} = 5.5$ V	
I_{OZL}	Output Off Current LOW				−650	mA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current	OE, T/R Inputs			20	µA	$V_{IN} = 2.7$ V	V_{CC} = MAX
		An, Bn Inputs			70	µA		
		OE, T/R Inputs			100	µA	$V_{IN} = 7.0$ V	
		An, Bn Inputs			1.0	mA	$V_{IN} = 5.5$ V	
I_{IL}	Input LOW Current	T/R Input			−0.8	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
		An, Bn Inputs			−650	mA		
		OE Input			−1.2	mA		
I_{OS}	Output Drive Current (Note 2)	An Outputs	−60		−150	mA	V_{OUT} = GND	V_{CC} = MAX
		Bn Outputs	−100		−225	mA	V_{OUT} = GND	V_{CC} = MAX
I_{CCH}	Power Supply Current				90	mA	V_{CC} = MAX	
I_{CCL}					120			
I_{CCZ}					110			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = -55$ to $+125°C$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50$ pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay An to Bn or Bn to An	2.5 2.5	6.0 6.0	2.5 2.5	8.0 8.0	2.5 2.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.5	7.0 8.0	3.0 3.5	9.0 10	3.0 3.5	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.5 2.0	6.5 6.5	2.5 2.0	8.5 8.5	2.5 2.0	7.5 7.5	ns

MOTOROLA

MC54F/74F251

8-INPUT MULTIPLEXER
(With 3-State Outputs)

FAST™ SCHOTTKY TTL

8-INPUT MULTIPLEXER
(With 3-State Outputs)

DESCRIPTION — The MC54F/74F251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **MULTIFUNCTIONAL CAPACITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INVERTING AND NON-INVERTING 3-STATE OUTPUTS**

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$\begin{aligned} Z = \overline{OE} \cdot (&I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + \\ &I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + \\ &I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + \\ &I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2 + \end{aligned}$$

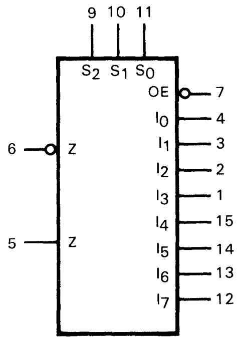
When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by typing the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

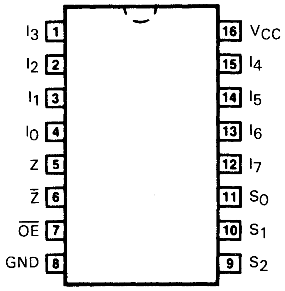
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC SYMBOL



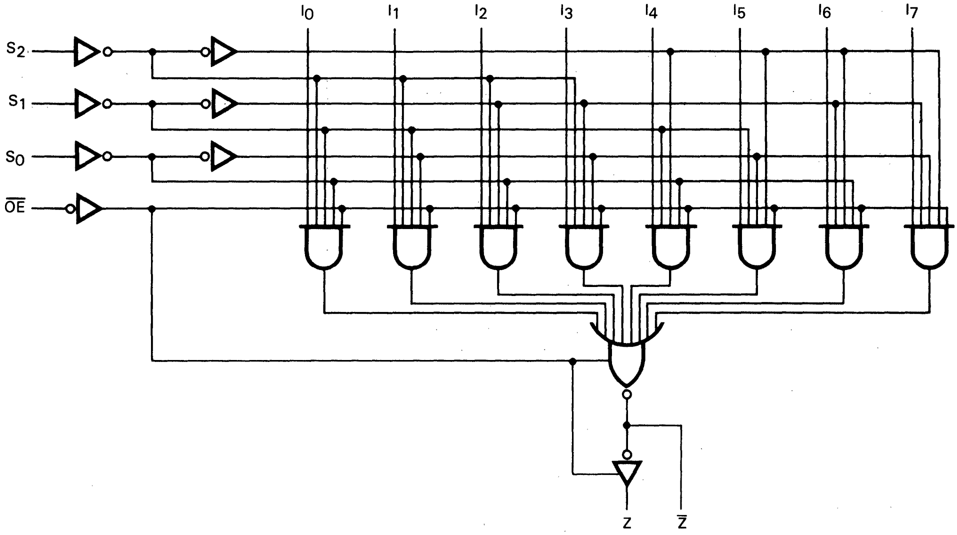
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

LOGIC DIAGRAM


I0
I1
I2
I3
I4
I5
I6
I7
S2
S1
S0
OE
Z
Z̄

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = 18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	I_{OH} = -3.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output Off Current—HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current—LOW				-50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current	ON		15	22	mA	I_n, S_n = 4.5 V $\overline{OE}$ = GND	V_{CC} = MAX
		OFF		16	24		$\overline{OE}$, I_n = 4.5 V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	4.0 3.2	8.0 7.5	3.5 3.2	9.5 9.5	4.0 3.2	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.5 4.5	13 9.0	3.5 3.0	16.5 10.5	4.5 4.0	14 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	3.0 1.5	5.7 4.0	2.5 1.5	8.0 6.0	3.0 1.5	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z	4.0 3.0	9.5 6.5	3.5 3.0	11.5 7.5	4.0 3.0	10.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{Z}$	3.0 3.0	7.0 8.5	3.0 3.0	9.5 10.5	3.0 3.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{Z}$	3.0 2.0	6.5 4.5	3.0 2.0	8.5 8.0	3.0 2.0	7.5 5.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z	4.0 3.5	9.0 8.0	4.0 3.5	10 10	4.0 3.5	10 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Z	3.0 2.0	6.0 4.5	3.0 2.0	7.0 8.0	3.0 2.0	7.0 5.5	ns

MOTOROLA

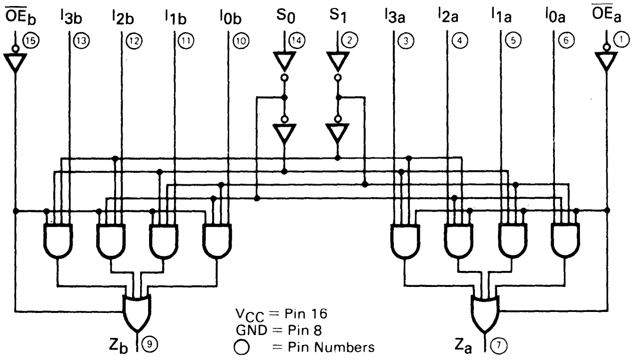
MC54F/74F253

DUAL 4-INPUT MULTIPLEXER
(with 3-State Outputs)

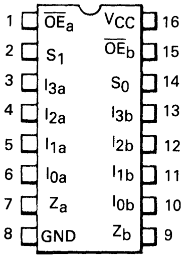
DESCRIPTION — The MC54F/74F253 is a Dual 4-Input Multiplexer with 3-State Outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable $\overline{OE}$ inputs, allowing the outputs to interface directly with bus oriented systems.

DUAL 4-INPUT MULTIPLEXER
WITH 3-STATE OUTPUTS
FAST™ SCHOTTKY TTL

LOGIC DIAGRAM


$\overline{OE}_b$ ⑮
I_{3b} ⑬
I_{2b} ⑫
I_{1b} ⑪
I_{0b} ⑩
S_0 ⑭
S_1 ②
I_{3a} ③
I_{2a} ④
I_{1a} ⑤
I_{0a} ⑥
$\overline{OE}_a$ ①
Z_b ⑨
Z_a ⑦
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP
(TOP VIEW)


1 $\overline{OE}_a$
2 S_1
3 I_{3a}
4 I_{2a}
5 I_{1a}
6 I_{0a}
7 Z_a
8 GND
16 V_{CC}
15 $\overline{OE}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Z_b

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74	—	—	−3.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	24	mA

FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-Input Multiplexers with 3-State Outputs. They select two bits from four sources selected by common Select Inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Immaterial
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

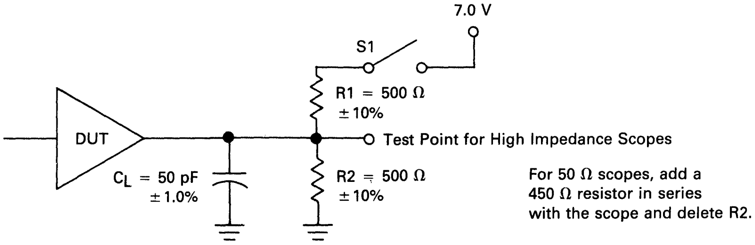
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = 18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4			V	I_{OH} = −3.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output Off Current—HIGH				50	µA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current—LOW				-50	µA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					0.1	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				16	mA	OE_n = GND I_0 = 4.5 V; S_n, I_1 - I_3 = GND	
	Total, Output LOW				23		I_n, S_n, OE_n = GND V_{CC} = MAX	
	Total at HIGH-Z				23		OE_n = 4.5 V, V_{CC} = MAX I_n, S_n = GND	

AC CHARACTERISTICS

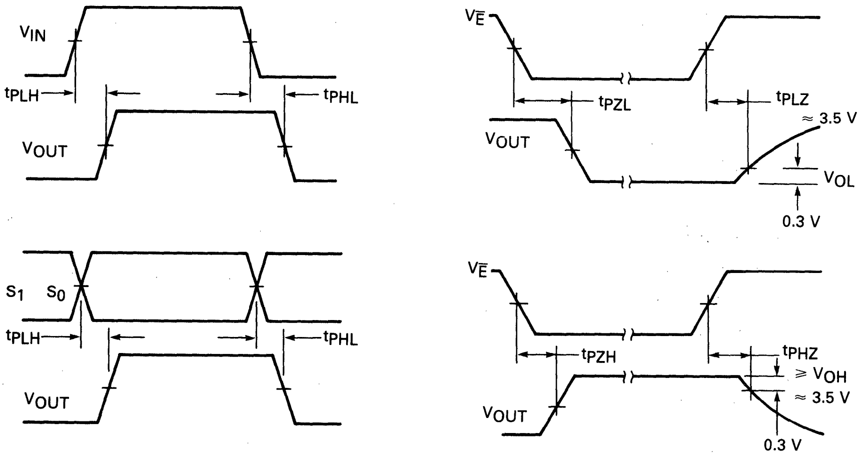
SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		74F $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay S_n to Z_n	4.5	11.5	3.5	15	4.5	13.5	ns
t_{PHL}		3.0	9.0	2.5	11	3.0	10	
t_{PLH}	Propagation Delay I_n to Z_n	3.0	7.0	2.5	9.0	3.0	8.0	ns
t_{PHL}		2.5	6.0	2.5	8.0	2.5	7.0	
t_{PZH}	Output Enable Time	3.0	8.0	2.5	10	3.0	9.0	ns
t_{PZL}		3.0	8.0	2.5	10	3.0	9.0	
t_{PHZ}	Output Disable Time	2.0	5.0	2.0	6.5	2.0	6.0	ns
t_{PLZ}		2.0	6.0	2.0	8.0	2.0	7.0	

AC TEST CIRCUIT


7.0 V
S1
R1 = 500 Ω
±10%
DUT
Test Point for High Impedance Scopes
C_L = 50 pF
±1.0%
R2 = 500 Ω
±10%

For 50 Ω scopes, add a
450 Ω resistor in series
with the scope and delete R2.

PROPAGATION DELAY MEASUREMENTS


V_{IN}
t_{PLH}
t_{PHL}
V_{OUT}
S_1 S_0
t_{PLH}
t_{PHL}
V_{OUT}
$V_{\overline{E}}$
t_{PZL}
t_{PLZ}
≈ 3.5 V
V_{OUT}
V_{OL}
0.3 V
$V_{\overline{E}}$
t_{PZH}
t_{PHZ}
≥ V_{OH}
≈ 3.5 V
V_{OUT}
0.3 V

NOTES:

1. All input waveforms have the following characteristics:
   Low Level = 0V
   High Level = 3.0 V
   Rise and Fall Times (10% to 90%) = 2.5 ns
2. All timing is measured at 1.5 V unless otherwise indicated.

MOTOROLA

MC54F/74F256

Advance Information

DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION — The MC54F/74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

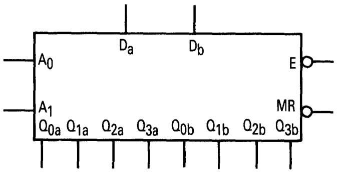
In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

- **Combines Dual Demultiplexer and 8-Bit Latch**
- **Serial-to-Parallel Capability**
- **Output from Each Storage Bit Available**
- **Random (Addressable) Data Entry**
- **Easily Expandable**
- **Common Clear Input**
- **Useful as Dual 1-of-4 Active HIGH Decoder**

DUAL 4-BIT ADDRESSABLE LATCH

FAST™ SCHOTTKY TTL

LOGIC SYMBOL

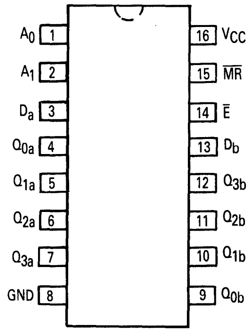


MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs					Outputs			
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Master Reset	L	H	X	X	X	L	L	L	L
Demultiplex (Active HIGH Decoder when D=H)	L	L	d	L	L	Q=d	L	L	L
	L	L	d	H	L	L	Q=d	L	L
	L	L	d	L	H	L	L	Q=d	L
	L	L	d	H	H	L	L	L	Q=d
Store (Do Nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable Latch	H	L	d	L	L	Q=d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q=d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q=d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q=d

H = HIGH Voltage Level Steady State
L = LOW Voltage Level Steady State
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

CONNECTION DIAGRAM

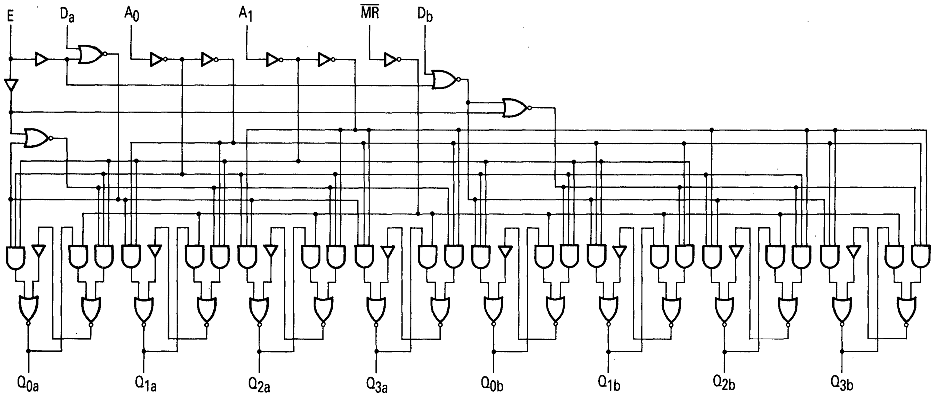


PIN ASSIGNMENT
TOP VIEW

J SUFFIX — CASE 620-09 (CERAMIC DIP)
N SUFFIX — CASE 648-08 (PLASTIC DIP)
D SUFFIX — CASE 751B-03 (SOIC)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM

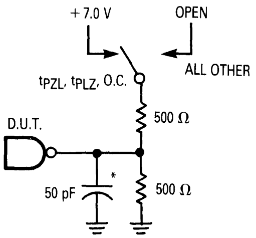


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

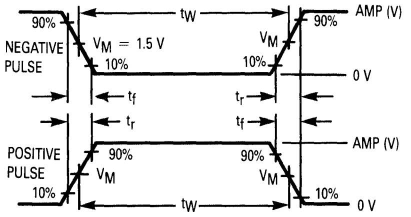
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

AC TEST CONDITIONS


+7.0 V
OPEN
ALL OTHER
tPZL, tPLZ, O.C.
D.U.T.
500 Ω
50 pF
*
500 Ω

*Includes jig and probe capacitance

FIGURE 1 — TEST LOAD


90%
NEGATIVE PULSE
tW
VM = 1.5 V
10%
VM
10%
90%
AMP (V)
0 V
tf
tr
tr
tf
POSITIVE PULSE
90%
VM
10%
90%
VM
10%
tW
AMP (V)
0 V

Amplitude	**Rep. Rate**	**Pulse Width**	**t_r**	**t_f**
3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2 — INPUT PULSE DEFINITION

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = MIN
		74	2.7			V	I_{OL} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.8	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				10.2	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC WAVEFORMS

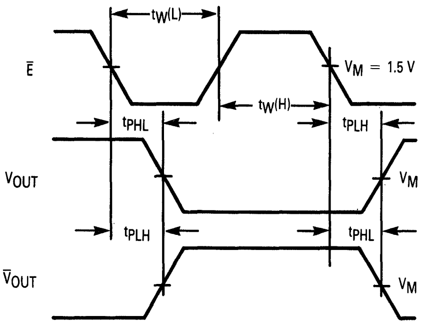

t_W(L)
E̅
V_M = 1.5 V
t_W(H)
t_PHL
t_PLH
V_OUT
V_M
t_PLH
t_PHL
V̅_OUT
V_M

FIGURE 1 — PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH

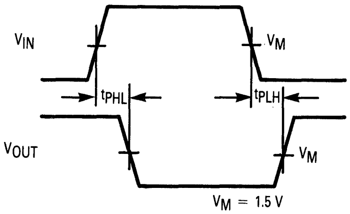

V_IN
V_M
t_PHL
t_PLH
V_OUT
V_M
V_M = 1.5 V

FIGURE 2 — PROPAGATION DELAY DATA TO OUTPUT

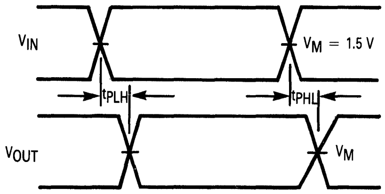

V_IN
V_M = 1.5 V
t_PLH
t_PHL
V_OUT
V_M

FIGURE 3 — PROPAGATION DELAY DATA TO OUTPUT

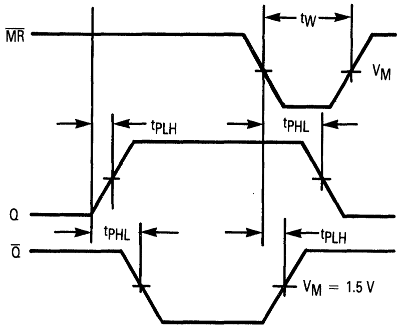

t_W
M̅R̅
V_M
t_PLH
t_PHL
Q
t_PHL
t_PLH
Q̅
V_M = 1.5 V

FIGURE 4 — PROPAGATION DELAY MASTER RESET TO OUTPUT AND MASTER RESET PULSE WIDTH

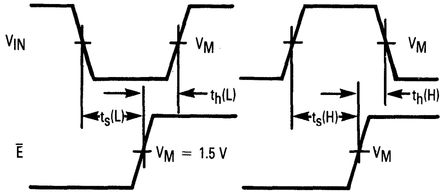

V_IN
V_M
V_M
t_h(L)
t_h(H)
t_s(L)
t_s(H)
E̅
V_M = 1.5 V
V_M

FIGURE 5 — SETUP AND HOLD TIME DATA TO ENABLE

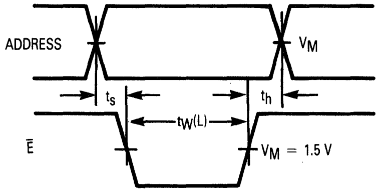

ADDRESS
V_M
t_s
t_h
t_W(L)
E̅
V_M = 1.5 V

FIGURE 6 — SETUP AND HOLD TIME ADDRESS TO ENABLE

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V $\pm$ 10% $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V $\pm$ 5% $C_L = 50$ pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n	4.0 3.0	10.5 7.0	4.0 3.0	13 8.5	4.0 3.0	12 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	3.5 3.0	9.0 7.0	3.5 2.5	11.5 8.5	3.5 2.5	10 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	3.5 4.0	14 9.5	3.5 4.0	15.5 11	3.5 4.0	14.5 10	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	9.0	4.5	11.5	4.5	10	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V		$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V $\pm$ 10%		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V $\pm$ 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{E}$	4.0 4.0		5.0 5.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{E}$	2.0 2.0		2.0 2.0		2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A to $\overline{E}$(a)	4.0 4.0		4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A to $\overline{E}$(b)	0 0		0 0		0 0		ns
t_W	$\overline{E}$ Pulse Width	4.0		4.0		4.0		ns
t_W	$\overline{MR}$ Pulse Width	4.0		4.0		4.0		ns

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

MOTOROLA

MC54F/74F257

QUAD 2-INPUT MULTIPLEXER
(With 3-State Outputs)

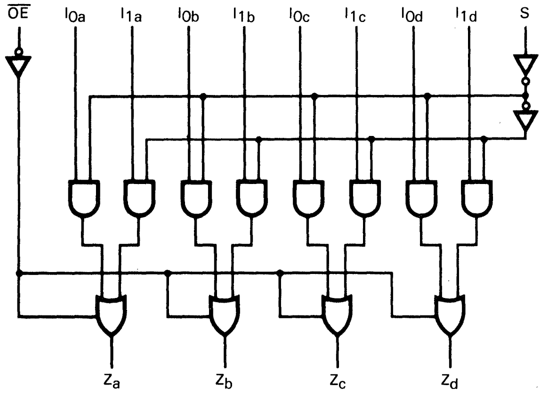
DESCRIPTION — The MC54F/74F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

QUAD 2-INPUT MULTIPLEXER
(With 3-State Outputs)

FAST™ SCHOTTKY TTL

LOGIC DIAGRAM

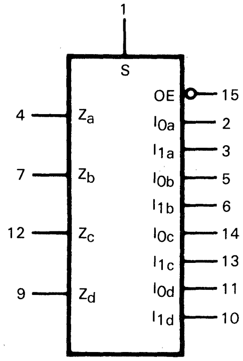

$\overline{OE}$
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
S
Z_a
Z_b
Z_c
Z_d

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

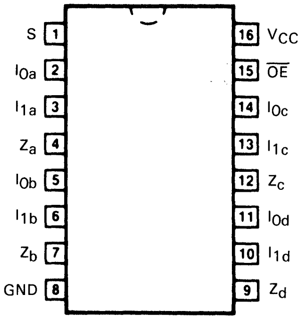
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

LOGIC SYMBOL


1
S
OE
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM


S 1
I_{0a} 2
I_{1a} 3
Z_a 4
I_{0b} 5
I_{1b} 6
Z_b 7
GND 8
16 V_{CC}
15 $\overline{OE}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current			9.0	15	mA	S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd	V_{CC} = MAX
I_{CCL}				14.5	22		I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd	
I_{CCZ}				15	23		S, I_{0x} = Gnd $\overline{OE}$, I_{1x} = 4.5 V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay I_n to Z_n	3.0	6.0	3.0	8.0	3.0	7.0	ns
t_{PHL}		2.0	5.5	1.5	8.0	2.0	6.5	
t_{PLH}	Propagation Delay S to Z_n	4.5	13	4.5	15.5	4.5	15	ns
t_{PHL}		3.5	8.5	3.5	10.5	3.5	9.5	
t_{PZH}	Output Enable Time	3.0	7.5	3.0	9.5	3.0	8.5	ns
t_{PZL}		3.0	7.5	3.0	10	3.0	8.5	
t_{PHZ}	Output Disable Time	2.0	6.0	2.0	7.0	2.0	7.0	ns
t_{PLZ}		2.0	6.0	2.0	9.5	2.0	7.0	

Advance Information

Quad 2-Input Multiplexer (With 3-State Outputs)

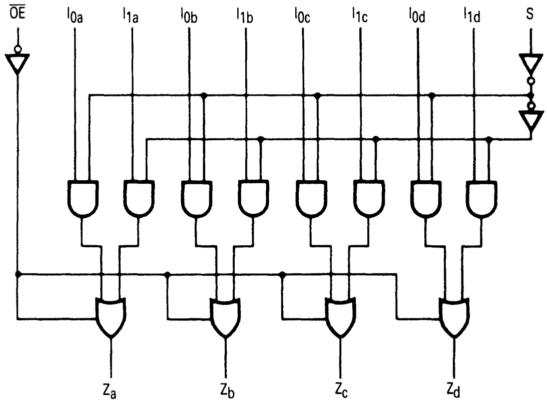
MC74F257A

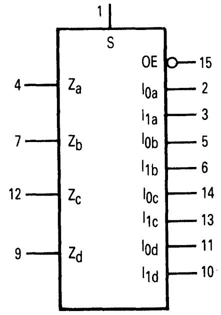
QUAD 2-INPUT MULTIPLEXER (WITH 3-STATE OUTPUTS) FAST™ SCHOTTKY TTL

The MC74F257A is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in the true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

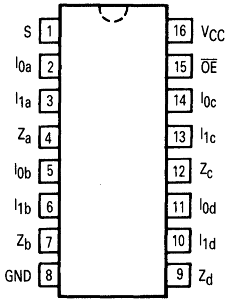
LOGIC DIAGRAM


$\overline{OE}$
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
S
Z_a
Z_b
Z_c
Z_d


1
S
OE
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

LOGIC SYMBOL

CONNECTION DIAGRAM


S 1
I_{0a} 2
I_{1a} 3
Z_a 4
I_{0b} 5
I_{1b} 6
Z_b 7
GND 8
16 V_{CC}
15 $\overline{OE}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

J SUFFIX — CASE 620-09 (CERAMIC)
N SUFFIX — CASE 648-08 (PLASTIC)
D SUFFIX — CASE 751B-03 (SOIC)

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−3	mA
I_{OL}	Output Current — Low	74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Units	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	74	2.7	3.3		V	$I_{OH} = -3$ mA	$V_{CC} = 4.75$ V
		74	2.4					V_{CC} = MIN
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	µA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	µA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	µA	$V_{IN} = 7$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCH}	Power Supply Current			9	15	mA	S, $I_{1x} = 4.5$ V $\overline{OE}$, I_{0x} = Gnd	V_{CC} = MAX
I_{CCL}				14.5	22		$I_{1x} = 4.5$ V $\overline{OE}$, I_{0x}, S = Gnd	
I_{CCZ}				15	23		S, I_{0x} = Gnd $\overline{OE}$, $I_{1x} = 4.5$ V	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

		74F $T_A = +25°C$ $V_{CC} = +5$ V $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5$ V ±10% $C_L = 50$ pF		
Symbol	Parameter	Min	Max	Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	1.5 2	5.5 5.5	1.5 2	6 6	ns
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	3 2.5	9.5 7	3 2.5	10.5 8	ns
t_{PZH} t_{PZL}	Output Enable Time	2 2.5	6.5 7	2 2.5	7 8	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2 2	6 6	2 2	7 7	ns

FUNCTIONAL DESCRIPTION

The F257A is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Z_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Z_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

MOTOROLA

MC54F/74F258

QUAD 2-INPUT MULTIPLEXER
(With 3-State Outputs)

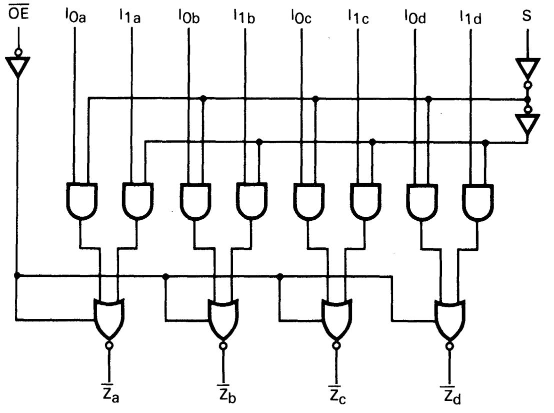
FAST™ SCHOTTKY TTL

QUAD 2-INPUT MULTIPLEXER
(With 3-State Outputs)

DESCRIPTION — The MC54F/74F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **INVERTING 3-STATE OUTPUTS**

LOGIC DIAGRAM

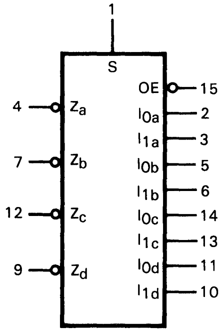

$\overline{OE}$
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
S
$\overline{Z}_a$
$\overline{Z}_b$
$\overline{Z}_c$
$\overline{Z}_d$

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

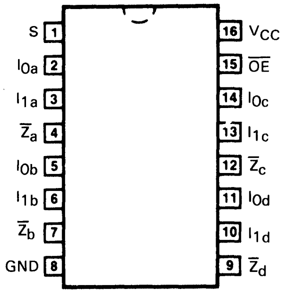
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC SYMBOLS


1
S
OE
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM


S 1
I_{0a} 2
I_{1a} 3
$\overline{Z}_a$ 4
I_{0b} 5
I_{1b} 6
$\overline{Z}_b$ 7
GND 8
16 V_{CC}
15 $\overline{OE}$
14 I_{0c}
13 I_{1c}
12 $\overline{Z}_c$
11 I_{0d}
10 I_{1d}
9 $\overline{Z}_d$

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100		$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCH}	Power Supply Current			6.2	9.5	mA	S, $I_{1X} = 4.5$ V $\overline{OE}$, I_{0X} = Gnd	V_{CC} = MAX
I_{CCL}				15.1	23		$I_{1X} = 4.5$ V $\overline{OE}$, I_{0X}, S = Gnd	
I_{CCZ}				11.3	17		S, I_{0X} = Gnd $\overline{OE}$, $I_{1X} = 4.5$ V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operaitng ranges.
2. Not more than one output shoudl be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad \overline{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad \overline{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.5	5.3	2.0	7.5	2.5	6.0	ns
t_{PHL}	I_n to $\overline{Z}_n$	1.5	4.7	1.5	6.0	1.5	5.5	
t_{PLH}	Propagation Delay	4.0	8.5	4.0	12	4.0	9.5	ns
t_{PHL}	S to $\overline{Z}_n$	4.0	9.5	4.0	11.5	4.0	11	
t_{PZH}	Output Enable Time	3.0	7.5	3.0	11	3.0	8.5	ns
t_{PZL}		3.0	7.5	3.0	9.5	3.0	8.5	
t_{PHZ}	Output Disable Time	2.0	6.0	1.5	7.0	2.0	7.0	ns
t_{PLZ}		2.0	6.0	2.0	9.0	2.0	7.0	

MOTOROLA

MC74F258A

Advance Information

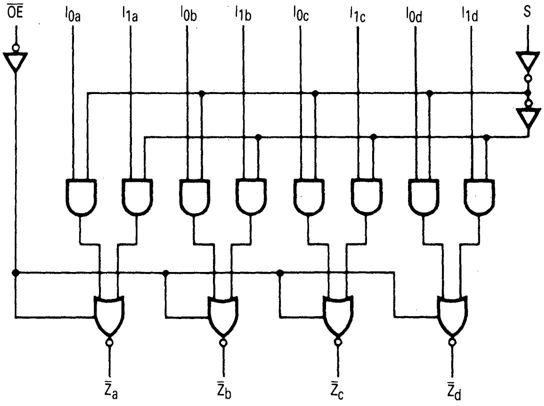
Quad 2-Input Multiplexer (With 3-State Outputs)

QUAD 2-INPUT MULTIPLEXER (WITH 3-STATE OUTPUTS) FAST™ SCHOTTKY TTL

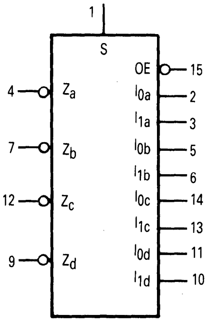
The MC74F258A is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Inverting 3-State Outputs

LOGIC DIAGRAM



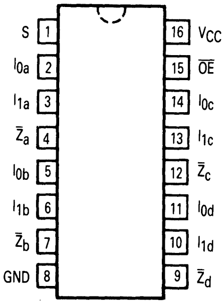
$\overline{OE}$
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
S
$\bar{Z}_a$
$\bar{Z}_b$
$\bar{Z}_c$
$\bar{Z}_d$



1
S
OE
15
4
Z_a
I_{0a}
2
I_{1a}
3
7
Z_b
I_{0b}
5
I_{1b}
6
12
Z_c
I_{0c}
14
I_{1c}
13
9
Z_d
I_{0d}
11
I_{1d}
10

LOGIC SYMBOL

CONNECTION DIAGRAM



S 1
I_{0a} 2
I_{1a} 3
$\bar{Z}_a$ 4
I_{0b} 5
I_{1b} 6
$\bar{Z}_b$ 7
GND 8
16 V_{CC}
15 $\overline{OE}$
14 I_{0c}
13 I_{1c}
12 $\bar{Z}_c$
11 I_{0d}
10 I_{1d}
9 $\bar{Z}_d$

J SUFFIX — CASE 620-09 (CERAMIC)
N SUFFIX — CASE 648-08 (PLASTIC)
D SUFFIX — CASE 751B-03 (SOIC)

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\bar{Z}$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−3	mA
I_{OL}	Output Current — Low	74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Units	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	74	2.7	3.3		V	$I_{OH} = -3$ mA	$V_{CC} = 4.75$ V
		74	2.4					V_{CC} = MIN
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	µA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	µA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	µA	$V_{IN} = 7$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCH}	Power Supply Current			6.2	9.5	mA	S, $I_{1x} = 4.5$ V $\overline{OE}$, I_{0x} = GND	V_{CC} = MAX
I_{CCL}				15.1	23		$I_{1x} = 4.5$ V $\overline{OE}$, I_{0x}, S = GND	
I_{CCZ}				11.3	17		S, I_{0x} = GND $\overline{OE}$, $I_{1x} = 4.5$ V	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5$ V $C_L = 50$ pF		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5$ V ±10% $C_L = 50$ pF		Units
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	2.5 1	5.3 4	2 1	6 5	ns
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3 2.5	7.5 7	3 2.5	8.5 8	ns
t_{PZH} t_{PZL}	Output Enable Time	2 2.5	6 7	2 2.5	7 8	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2 1.5	6 6	2 1.5	7 7	ns

FUNCTIONAL DESCRIPTION

The F258A is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

MOTOROLA

MC54F/74F259

Advance Information

8-BIT ADDRESSABLE LATCH

DESCRIPTION — The MC54F/74F259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

- **Serial-to-Parallel Conversion**
- **Eight Bits of Storage with Output of Each Bit Available**
- **Random (Addressable) Data Entry**
- **Active High Demultiplexing or Decoding Capability**
- **Easily Expandable**
- **Common Clear**

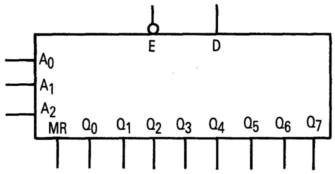
FUNCTIONAL DESCRIPTION — The MC54F/74F259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC54F/74F259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the MC54F/74F259.

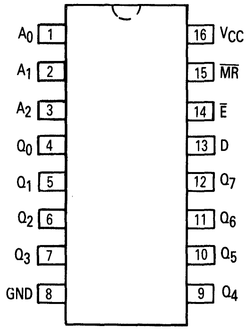
8-BIT ADDRESSABLE LATCH

FAST™ SCHOTTKY TTL

LOGIC SYMBOL



CONNECTION DIAGRAM



PIN ASSIGNMENT

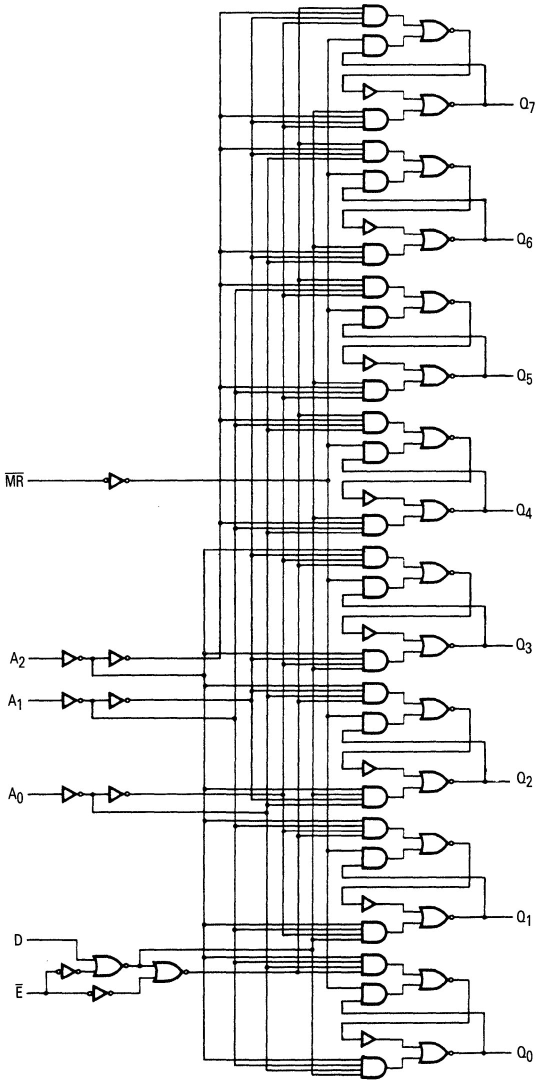
TOP VIEW

J SUFFIX — CASE 620-09 (CERAMIC DIP)
N SUFFIX — CASE 648-08 (PLASTIC DIP)
D SUFFIX — CASE 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.



MR
A2
A1
A0
D
E
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT TABLE

$\overline{E}$	$\overline{MR}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs													
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (Do Nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable Latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = MIN
		74	2.7			V	I_{OL} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.8	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				10.2	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n	4.0 3.0	10.5 7.0	4.0 3.0	13 8.5	4.0 3.0	12 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	3.5 3.0	9.0 6.5	3.5 2.5	11.5 8.5	3.5 2.5	10 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	3.5 4.0	13 9.0	3.5 4.0	15.5 11	3.5 4.0	14.5 9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	9.0	4.5	11.5	4.5	10	ns

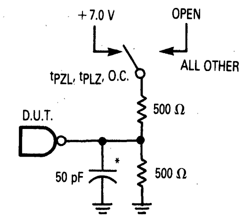
AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V		T_A = −55 to +125°C V_{CC} = 5.0 V ± 10%		T_A = 0 to +70°C V_{CC} = 5.0 V ± 10%		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{E}$	4.0 4.0		5.0 5.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{E}$	2.0 2.0		2.0 2.0		2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A to $\overline{E}$(a)	4.0 4.0		4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A to $\overline{E}$(b)	0 0		0 0		0 0		ns
t_W	$\overline{E}$ Pulse Width	4.0		4.0		4.0		ns
t_W	$\overline{MR}$ Pulse Width	4.0		4.0		4.0		ns

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

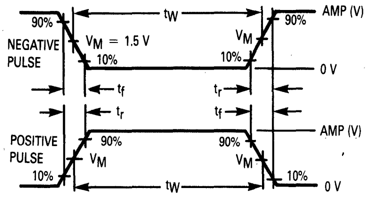
b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC TEST CONDITIONS


+7.0 V
OPEN
ALL OTHER
tPZL, tPLZ, O.C.
500 Ω
D.U.T.
50 pF
*
500 Ω

*Includes jig and probe capacitance

FIGURE 1 — TEST LOAD


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM = 1.5 V
VM
10%
10%
0 V
tf
tr
tr
tf
AMP (V)
POSITIVE PULSE
90%
90%
VM
VM
10%
10%
tW
0 V

Amplitude	Rep. Rate	Pulse Width	t_r	t_f
3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2 — INPUT PULSE DEFINITION

AC WAVEFORMS

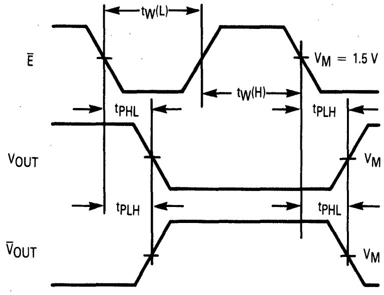

tW(L)
Ē
VM = 1.5 V
tW(H)
tPHL
tPLH
VOUT
VM
tPLH
tPHL
V̄OUT
VM

FIGURE 1 — PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH

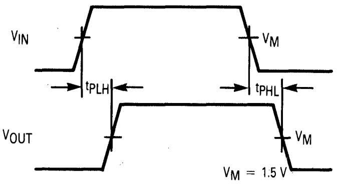

VIN
VM
tPLH
tPHL
VOUT
VM
VM = 1.5 V

FIGURE 2 — PROPAGATION DELAY DATA TO OUTPUT

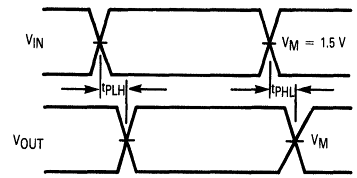

VIN
VM = 1.5 V
tPLH
tPHL
VOUT
VM

FIGURE 3 — PROPAGATION DELAY DATA TO OUTPUT

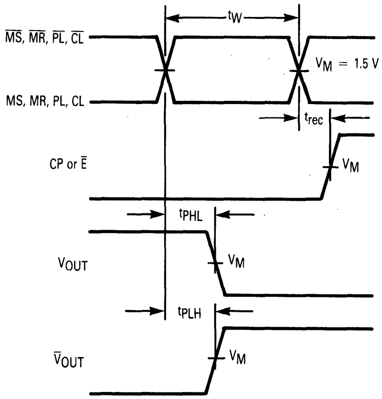

tW
M̄S̄, M̄R̄, P̄L̄, C̄L̄
VM = 1.5 V
MS, MR, PL, CL
trec
CP or Ē
VM
tPHL
VOUT
VM
tPLH
V̄OUT
VM

FIGURE 4 — PROPAGATION DELAY MASTER RESET TO OUTPUT AND MASTER RESET PULSE WIDTH

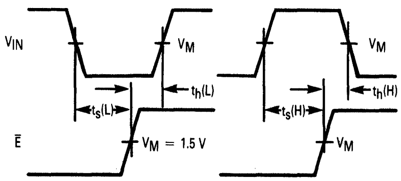

VIN
VM
VM
th(L)
th(H)
ts(L)
ts(H)
Ē
VM = 1.5 V
VM

FIGURE 5 — SETUP AND HOLD TIME DATA TO ENABLE

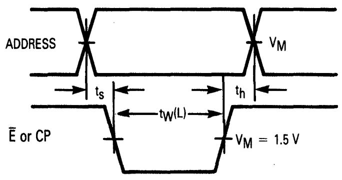
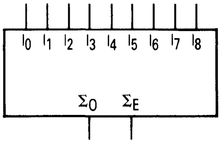

ADDRESS
VM
ts
th
tW(L)
Ē or CP
VM = 1.5 V

FIGURE 6 — SETUP AND HOLD TIME ADDRESS TO ENABLE

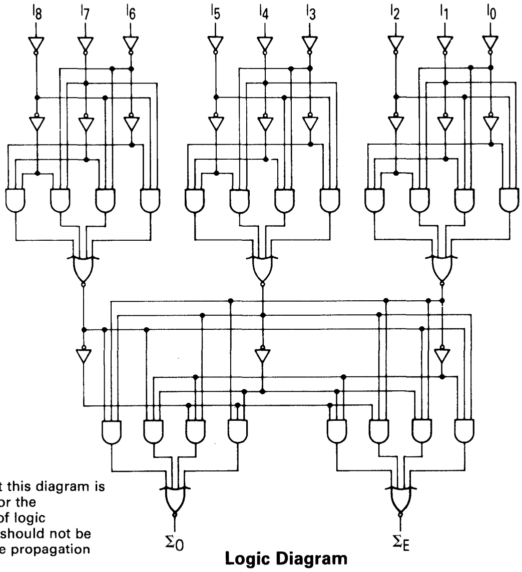
MC54F/74F280

9-Bit Parity Generator/Checker

The MC54/74F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

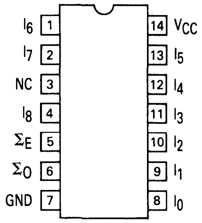

I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
I_8
Σ_O
Σ_E

LOGIC SYMBOL


I_8
I_7
I_6
I_5
I_4
I_3
I_2
I_1
I_0
Σ_O
Σ_E

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram


I_6 1
I_7 2
NC 3
I_8 4
Σ_E 5
Σ_O 6
GND 7
14 V_{CC}
13 I_5
12 I_4
11 I_3
10 I_2
9 I_1
8 I_0

CONNECTION DIAGRAM

J Suffix — Case 632-08
(Ceramic)
N Suffix — Case 646-06
(Plastic)
D Suffix — Case 751A-02
(SOIC)

TRUTH TABLE

Number of HIGH Inputs I_0–I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1	mA
I_{OL}	Output Current — Low	54, 74			20	mA

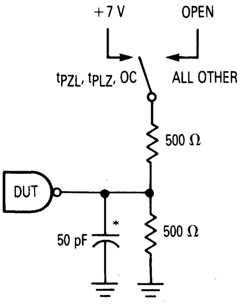
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Units	Test Conditions	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					100	μA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			25	38	mA	V_{CC} = MAX	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5 V C_L = 50 pF Min	54/74F Max	54F T_A = −55 to +125°C V_{CC} = 5 V ±10% C_L = 50 pF Min	54F Max	74F T_A = 0 to +70°C V_{CC} = 5 V ±10% C_L = 50 pF Min	74F Max	Units
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E	4.5 4.5	15 16	4.5 4.5	20 21	4.5 4.5	16 17	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O	4.5 4.5	15 16	4.5 4.5	20 21	4.5 4.5	16 17	ns



*INCLUDES JIG AND PROBE CAPACITANCE

Figure 1. Test Load

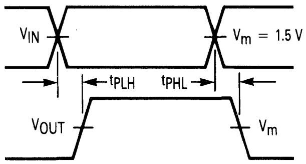


Figure 2. Whether Response Is Inverting or Non-Inverting Depends on Specific Truth Table Conditions

MOTOROLA

MC54F/74F283

Advance Information

4-BIT BINARY FULL ADDER
(With Fast Carry)

DESCRIPTION — MC54F/74F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0 - A_3, B_0 - B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0 - S_3) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

FUNCTIONAL DESCRIPTION — The 'F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0. The binary sum appears on the Sum (S_0 - S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0(A_0+B_0+C_0)+2^1(A_1+B_1)$$
$$+2^2(A_2+B_2)+2^3(A_3+B_3)$$
$$= S_0+2S_1+4S_2+8S_3+16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if C_0 is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

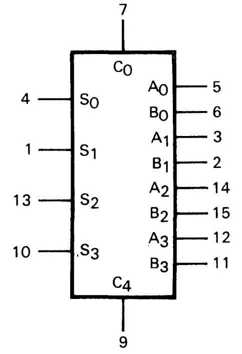
Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1 - I_5 that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1 - I_5 are true, the output M_5 is true.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4-BIT BINARY FULL ADDER
(With Fast Carry)

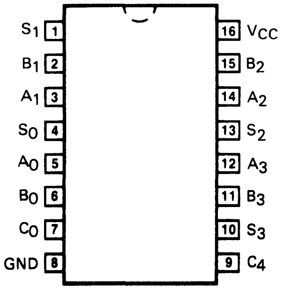
FAST™ SCHOTTKY TTL

LOGIC SYMBOL



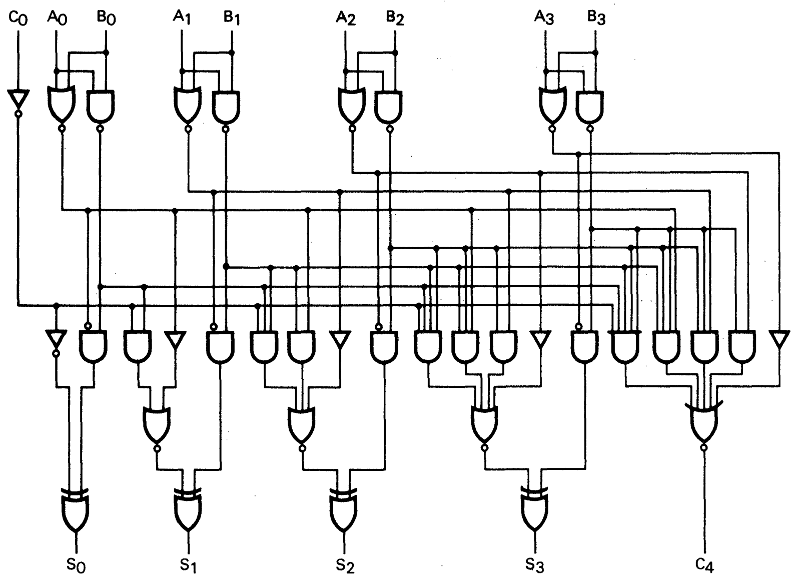
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74	—	—	-1.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	20	mA

FIGURE A — Active-HIGH versus Active-LOW Interpretation

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

FIGURE B — 3-Bit Adder

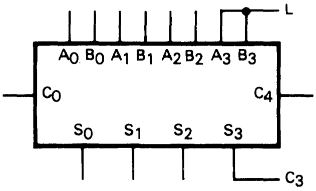

L
A0 B0 A1 B1 A2 B2 A3 B3
C0
C4
S0 S1 S2 S3
C3

FIGURE C — 2-Bit and 1-Bit Adders

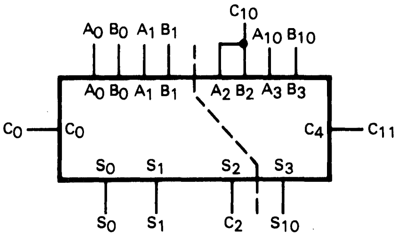

C10
A0 B0 A1 B1
A10 B10
A0 B0 A1 B1 A2 B2 A3 B3
C0
C0
C4
C11
S0 S1 S2 S3
S0 S1 C2 S10

FIGURE D — 5-Input Encoder

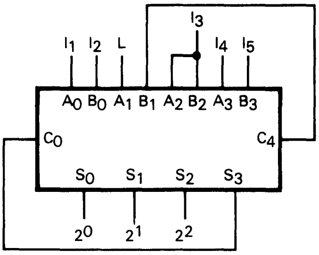
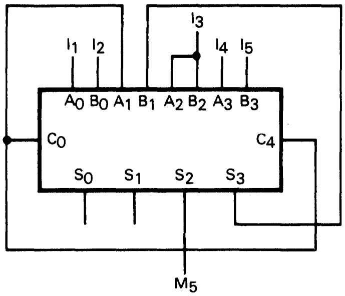

I3
I1 I2 L
I4 I5
A0 B0 A1 B1 A2 B2 A3 B3
C0
C4
S0 S1 S2 S3
2^0 2^1 2^2

FIGURE E — 5-Input Majority Gate


I3
I1 I2
I4 I5
A0 B0 A1 B1 A2 B2 A3 B3
C0
C4
S0 S1 S2 S3
M5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current C_0 Input				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
	A and B Inputs				-1.2	mA		
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			36	55	mA	Inputs = 4.5 V	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V $\pm 10\%$ $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V $\pm 10\%$ $C_L = 50$ pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	3.5	7.0	9.5	3.5	14	3.5	10.5	ns
t_{PHL}	C_0 to S_n	4.0	7.0	9.5	4.0	14	4.0	10.5	
t_{PLH}	Propagation Delay	4.0	7.0	9.5	4.0	14	4.0	10.5	ns
t_{PHL}	A_n or B_n to S_n	3.5	7.0	9.5	3.5	14	3.5	10.5	
t_{PLH}	Propagation Delay	3.5	5.7	7.5	3.5	10.5	3.5	8.5	ns
t_{PHL}	C_0 to C_4	3.0	5.4	7.0	3.0	10	3.0	8.0	
t_{PLH}	Propagation Delay	3.5	5.7	7.5	3.5	10.5	3.5	8.5	ns
t_{PHL}	A_n or B_n to C_4	3.0	5.3	7.0	3.0	10	3.0	8.0	

MOTOROLA

MC54F/74F350

4-BIT SHIFTER
(With 3-State Outputs)

FAST™ SCHOTTKY TTL

Advance Information

4-BIT SHIFTER
(With 3-State Outputs)

DESCRIPTION — MC54F/74F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable ($\overline{OE}$) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

- **Linking Inputs for Word Expansion**
- **3-State Outputs for Extending Shift Range**

FUNCTIONAL DESCRIPTION — The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1. Outputs O_0-O_3 are 3-state, controlled by an active-LOW output enable ($\overline{OE}$). When $\overline{OE}$ is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC EQUATIONS

$$O_0 = \overline{S}_0 \overline{S}_1 I_0 + S_0 \overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$
$$O_1 = \overline{S}_0 \overline{S}_1 I_1 + S_0 \overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$
$$O_2 = \overline{S}_0 \overline{S}_1 I_2 + S_0 \overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$
$$O_3 = \overline{S}_0 \overline{S}_1 I_3 + S_0 \overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

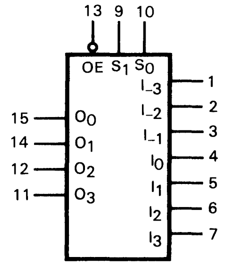
TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

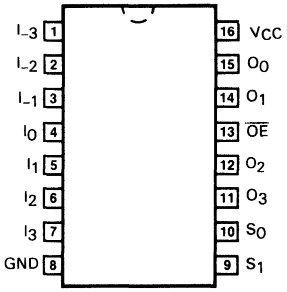
This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC SYMBOL



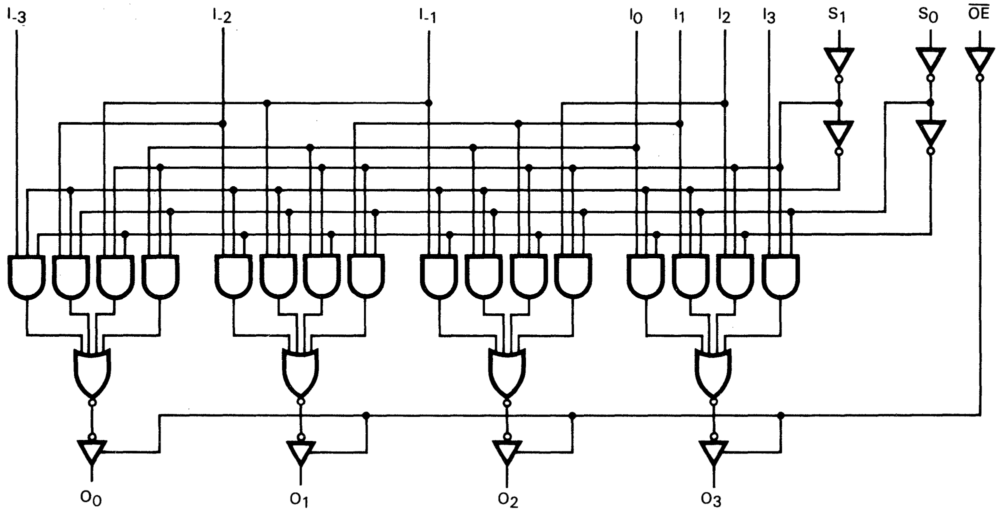
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74	—	—	-3.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−1.2	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current			22	35	mA	Outputs HIGH	V_{CC} = MAX
I_{CCL}				26	41		Outputs LOW	
I_{CCZ}				26	42		Outputs OFF	

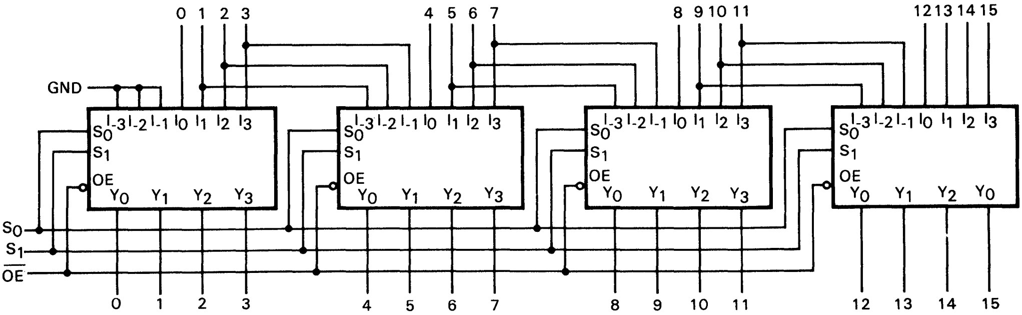
NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay I_n to O_n	3.0 2.5	6.0 5.5	3.0 2.5	7.5 7.0	3.0 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to O_n	4.0 3.0	10 8.5	4.0 3.0	13 10	4.0 3.0	11 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time	2.5 4.0	7.0 9.0	2.5 4.0	8.5 11	2.5 4.0	8.0 10	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 1.5	5.5 5.5	2.0 1.5	7.0 8.5	2.0 1.5	6.5 6.5	ns

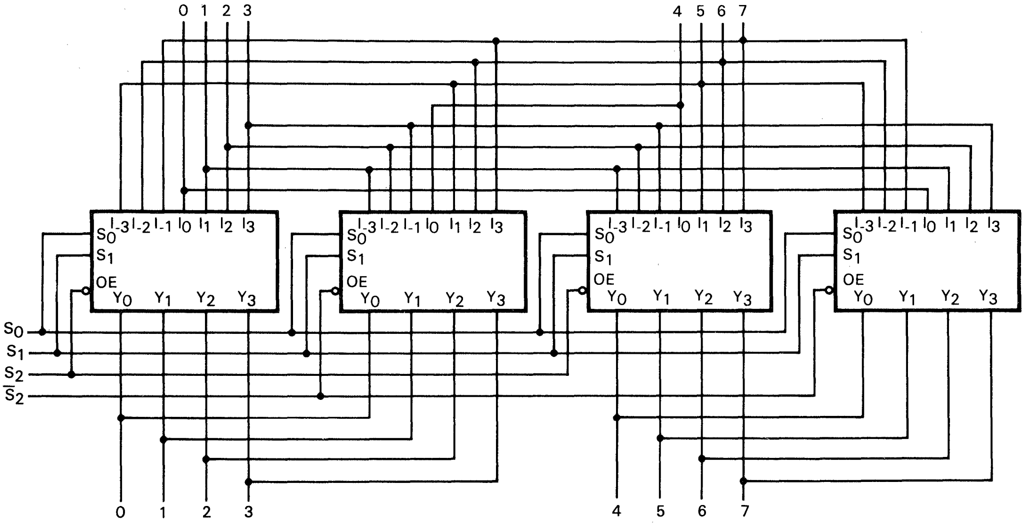
APPLICATIONS

16-Bit Shift-Up 0 to 3 Places, Zero Backfill


0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
GND
S_0 I_{-3} I_{-2} I_{-1} I_0 I_1 I_2 I_3
S_1
OE
Y_0 Y_1 Y_2 Y_3
Y_0 Y_1 Y_2 Y_0
S_0
S_1
$\overline{OE}$
0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15

S_1	S_0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

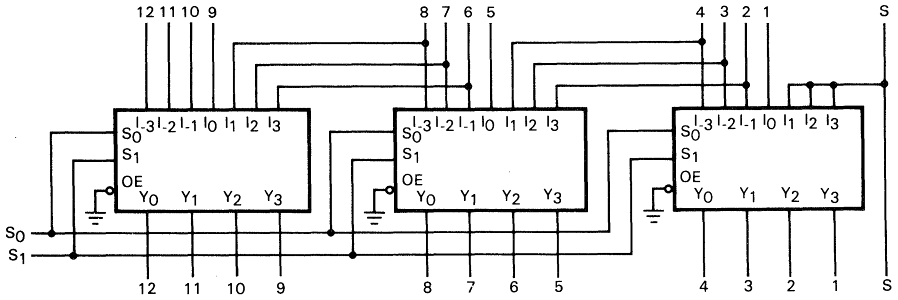
8-Bit End Around Shift 0 to 7 Places


0 1 2 3
4 5 6 7
S_0 I_{-3} I_{-2} I_{-1} I_0 I_1 I_2 I_3
S_1
OE
Y_0 Y_1 Y_2 Y_3
S_0
S_1
S_2
$\overline{S_2}$
0 1 2 3
4 5 6 7

S_2	S_1	S_0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4

S_2	S_1	S_0	
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-Bit Twos Complement Scaler


12 11 10 9
8 7 6 5
4 3 2 1
S
S_0 I_{-3} I_{-2} I_{-1} I_0 I_1 I_2 I_3
S_1
OE
Y_0 Y_1 Y_2 Y_3
S_0
S_1
12 11 10 9
8 7 6 5
4 3 2 1
S

S_1	S_0	SCALE
L	L ÷ 8	1/8
L	H÷4	1/4
H	L ÷ 2	1/2
H	H NO CHANGE	1

MOTOROLA

MC54F/74F352

DUAL 4-INPUT MULTIPLEXER

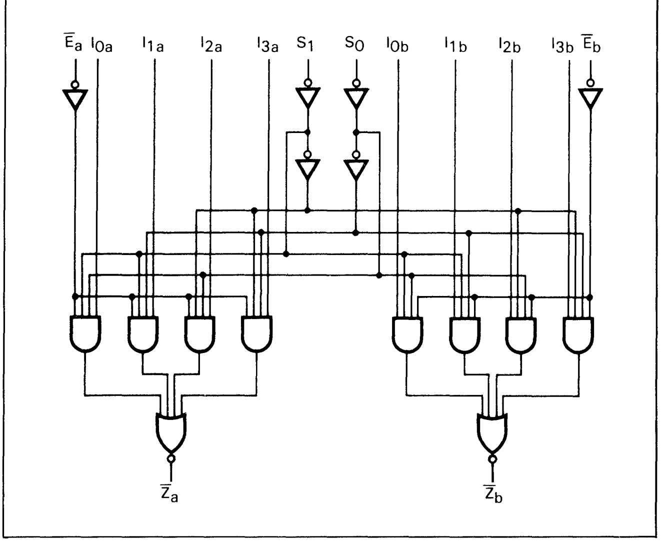
DESCRIPTION — The MC54F/74F352 is a very high speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

- **Inverted Version of the 'F153**
- **Separate Enables for Each Multiplexer**
- **Input Clamp Diode Limits High Speed Termination Effects**

DUAL 4-INPUT MULTIPLEXER

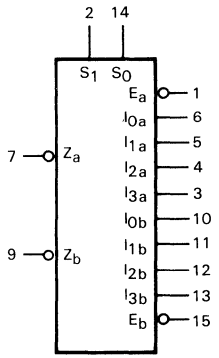
FAST™ SCHOTTKY TTL

LOGIC DIAGRAM



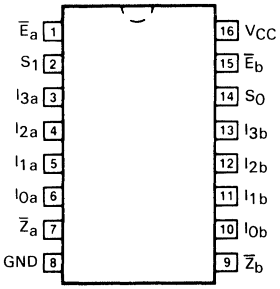
$\overline{E}_a$
I_{0a}
I_{1a}
I_{2a}
I_{3a}
S_1
S_0
I_{0b}
I_{1b}
I_{2b}
I_{3b}
$\overline{E}_b$
$\overline{Z}_a$
$\overline{Z}_b$

LOGIC SYMBOL



2
14
S_1
S_0
E_a
1
I_{0a}
6
I_{1a}
5
7
Z_a
I_{2a}
4
I_{3a}
3
I_{0b}
10
9
Z_b
I_{1b}
11
I_{2b}
12
I_{3b}
13
E_b
15

CONNECTION DIAGRAM



$\overline{E}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
$\overline{Z}_a$ 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Z}_b$

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

FUNCTIONAL DESCRIPTION — The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$
$$\overline{Z}_b = \overline{E_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current			9.3	14	mA	V_{IN} = Gnd	V_{CC} = MAX
I_{CCL}				13.3	20		V_{IN} = HIGH	

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF MIN	TYP	MAX	54F T_A = -55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF MIN	MAX	74F T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF MIN	MAX	UNITS
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.5 3.0	7.4 7.0	11 8.5	3.0 2.5	14 11	3.0 2.5	12.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	2.5 3.0	5.0 5.0	7.0 7.0	2.0 2.5	10 9.0	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	2.5 1.5	4.9 3.0	7.0 3.5	2.0 1.0	9.0 5.0	2.0 1.0	8.0 4.0	ns

MOTOROLA

MC54F/74F353

DUAL 4-INPUT MULTIPLEXER (With 3-State Outputs)

DUAL 4-INPUT MULTIPLEXER
(With 3-State Outputs)

DESCRIPTION — The MC54F/74F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- **Inverted Version of 'F253**
- **Multifunction Capability**
- **Separate Enables for Each Multiplexer**

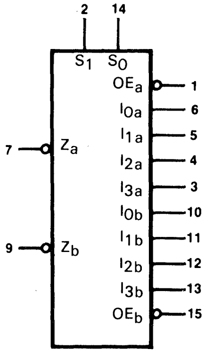
FUNCTIONAL DESCRIPTION — The 'F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

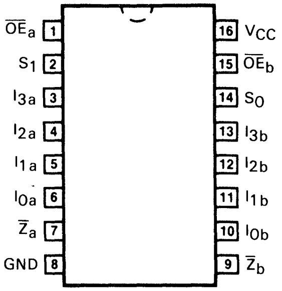
TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

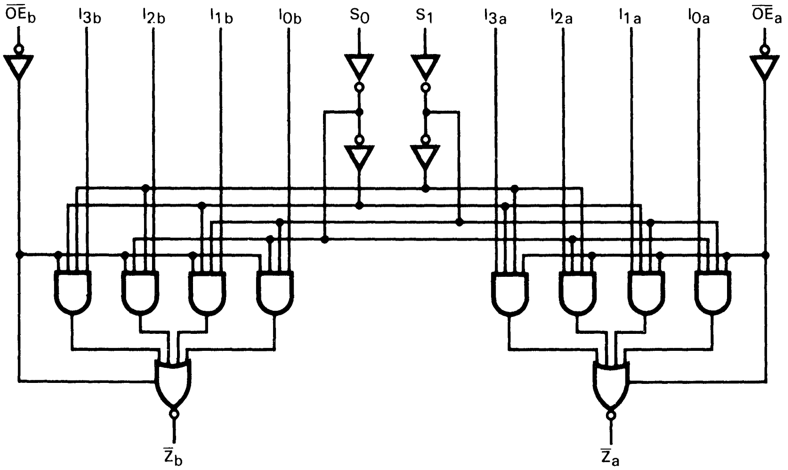
Address inputs S_0 and S_1 are common to both sections.

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

LOGIC DIAGRAM


$\overline{OE}_b$
I_{3b}
I_{2b}
I_{1b}
I_{0b}
S_0
S_1
I_{3a}
I_{2a}
I_{1a}
I_{0a}
$\overline{OE}_a$
$\overline{Z}_b$
$\overline{Z}_a$

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.5 3.0	11 8.5	3.0 2.5	14 11	3.0 2.5	12.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	2.5 1.0	7.0 3.5	2.0 1.0	9.0 5.0	2.0 1.0	8.0 4.0	ns
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.5	8.0 8.0	3.0 3.0	10.5 10.5	3.0 3.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	5.0 6.0	2.0 1.5	7.0 8.0	1.5 1.5	6.0 7.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100		$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCH}	Power Supply Current			9.3	14	mA	I_n, S_n, $\overline{OE}_n$ = Gnd	V_{CC} = MAX
I_{CCL}				13.3	20		I_n, S_n = Gnd	
I_{CCZ}				15	23		$\overline{OE}_n = 4.5$ V	

NOTES:

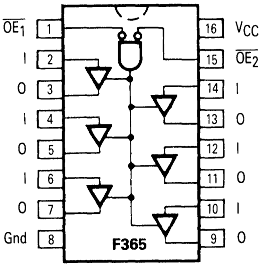
1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

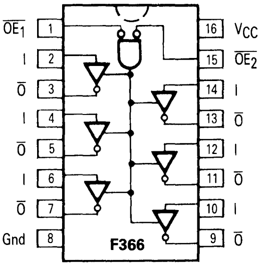
MOTOROLA

MC54F/74F365
MC54F/74F366

Advance Information

HEX BUFFER/DRIVER GATED ENABLE NON-INVERTING AND INVERTING, 3-STATE


$\overline{OE}_1$
1
I
2
O
3
I
4
O
5
I
6
O
7
Gnd
8
16
V_{CC}
15
$\overline{OE}_2$
14
I
13
O
12
I
11
O
10
I
9
O
F365


$\overline{OE}_1$
1
I
2
$\overline{O}$
3
I
4
$\overline{O}$
5
I
6
$\overline{O}$
7
Gnd
8
16
V_{CC}
15
$\overline{OE}_2$
14
I
13
$\overline{O}$
12
I
11
$\overline{O}$
10
I
9
$\overline{O}$
F366

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

F365
HEX BUFFER/DRIVER
GATED ENABLE
NON-INVERTING, 3-STATE

F366
HEX BUFFER/DRIVER
GATED ENABLE
INVERTING, 3-STATE

FAST™ SCHOTTKY TTL

FUNCTION TABLE

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	O	$\overline{O}$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			48 64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
		54	2.0			V	I_{OH} = −12 mA	V_{CC} = 4.5 V
		74	2.0			V	I_{OH} = −15 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	54		0.35	0.55	V	I_{OL} = 48 mA	V_{CC} = MAX
		74		0.4	0.55	V	I_{OL} = 64 mA	
I_{OZH}	Output Off Current HIGH				50	µA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current LOW				−50	µA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = 0 V
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−20	µA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Drive Current Note 2		−100		−225	mA	V_{OUT} = GND	V_{CC} = MAX
I_{CC}	F365	I_{CCH}			35	mA	V_{CC} = MAX	
		I_{CCL}			62			
		I_{CCZ}			48			
	F366	I_{CCH}			25			
		I_{CCL}			62			
		I_{CCZ}			48			

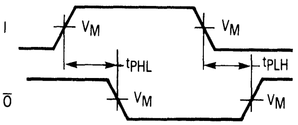
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

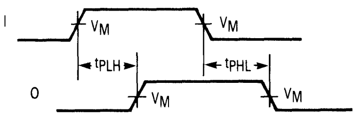
AC CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
				T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		T_A = 0°C to +70°C V_{CC} = +5.0 V ± 10% C_L = 50 pF		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay I_n to O_n	F365	Waveform 2	2.0	4.5	6.5	2.0	8.0	2.0	7.0	ns
t_{PHL}				3.0	5.5	7.0	3.0	8.5	3.0	7.5	
t_{PLH}	Propagation Delay I_n to $\overline{O}_n$	F366	Waveform 1	2.0	5.0	6.5	2.0	8.5	2.0	7.5	ns
t_{PHL}				1.0	3.0	5.0	1.0	6.5	1.0	5.5	
t_{PZH}	Output Enable Time to HIGH and LOW Level		Waveforms 3 & 4	3.0	6.5	9.5	3.0	11	3.0	10	ns
t_{PZL}				4.0	6.0	9.0	4.0	10.5	4.0	9.5	
t_{PHZ}	Output Disable Time from HIGH and LOW Level			2.5	4.5	6.5	2.5	8.0	2.5	7.0	ns
t_{PLZ}				1.5	4.0	6.0	1.5	7.5	1.5	6.5	

AC WAVEFORMS

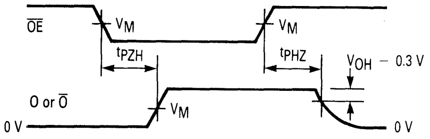

I
VM
VM
tPHL
tPLH
Ō
VM
VM

WAVEFORM 1 — FOR INVERTING OUTPUTS

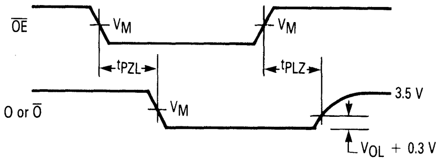

I
VM
VM
tPLH
tPHL
O
VM
VM

WAVEFORM 2 — FOR NON-INVERTING OUTPUTS

NOTE: For all waveforms, V_M = 1.5 V.

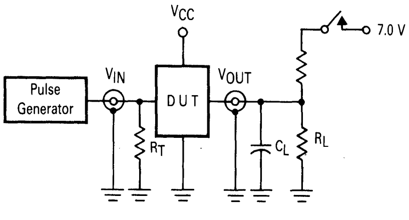

OE
VM
VM
tPZH
tPHZ
VOH − 0.3 V
O or Ō
0 V
VM
0 V

WAVEFORM 3 — 3-STATE OUTPUT ENABLE TIME TO HIGH LEVEL AND OUTPUT DISABLE TIME FROM HIGH LEVEL

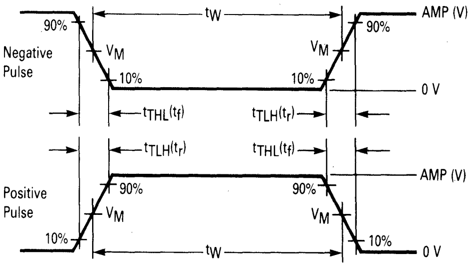

OE
VM
VM
tPZL
tPLZ
3.5 V
O or Ō
VM
VOL + 0.3 V

WAVEFORM 4 — 3-STATE OUTPUT ENABLE TIME TO LOW LEVEL AND OUTPUT DISABLE TIME FROM LOW LEVEL

TEST CIRCUIT AND WAVEFORMS


VCC
7.0 V
Pulse Generator
VIN
DUT
VOUT
RT
CL
RL

TEST CIRCUIT FOR 3-STATE OUTPUTS


tW
AMP (V)
90%
90%
Negative Pulse
VM
VM
10%
10%
0 V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
Positive Pulse
90%
90%
VM
VM
10%
10%
tW
0 V

V_M = 1.5 V

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

INPUT PULSE DEFINITION

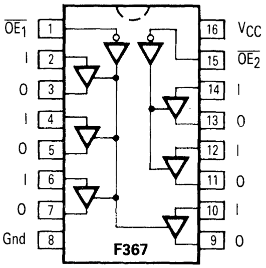
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

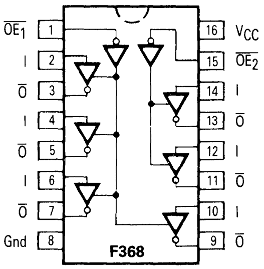
MOTOROLA

MC54F/74F367
MC54F/74F368

Advance Information

HEX BUFFER/DRIVER 4-BIT PLUS 2-BIT, NON-INVERTING AND INVERTING, 3-STATE


$\overline{OE}_1$
I
O
I
O
I
O
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{CC}
$\overline{OE}_2$
I
O
I
O
I
O
F367


$\overline{OE}_1$
I
$\overline{O}$
I
$\overline{O}$
I
$\overline{O}$
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{CC}
$\overline{OE}_2$
I
$\overline{O}$
I
$\overline{O}$
I
$\overline{O}$
F368

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

F367
HEX BUFFER/DRIVER, 4-BIT PLUS 2-BIT, NON-INVERTING 3-STATE

F368
HEX BUFFER/DRIVER, 4-BIT PLUS 2-BIT, INVERTING 3-STATE

FAST™ SCHOTTKY TTL

FUNCTION TABLE

Inputs		Outputs	
$\overline{OE}$	I	O	$\overline{O}$
L	L	L	H
L	H	H	L
H	X	Z	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			48 64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
		54	2.0			V	I_{OH} = −12 mA	V_{CC} = 4.5 V
		74	2.0			V	I_{OH} = −15 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	54		0.35	0.55	V	I_{OL} = 48 mA	V_{CC} = MAX
		74		0.4	0.55	V	I_{OL} = 64 mA	
I_{OZH}	Output Off Current HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = 0 V
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−20	μA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Drive Current Note 2		−100		−225	mA	V_{OUT} = GND	V_{CC} = MAX
I_{CC}	F367	I_{CCH}			35	mA	V_{CC} = MAX	
		I_{CCL}			62			
		I_{CCZ}			48			
	F368	I_{CCH}			25			
		I_{CCL}			62			
		I_{CCZ}			48			

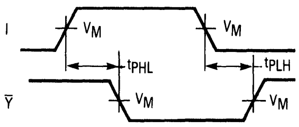
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

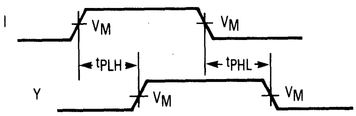
AC CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	54/74F			54F		74F		UNIT
				$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ± 10% $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V ± 10% $C_L = 50$ pF		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay I_n to O_n	F367	Waveform 2	2.0	4.5	6.5	2.0	8.0	2.0	7.0	ns
t_{PHL}				3.0	5.5	7.0	3.0	8.5	3.0	7.5	
t_{PLH}	Propagation Delay I_n to $\overline{O}_n$	F368	Waveform 1	2.0	5.0	6.5	2.0	8.5	2.0	7.5	ns
t_{PHL}				1.0	3.0	5.0	1.0	6.5	1.0	5.5	
t_{PZH}	Output Enable Time to HIGH and LOW Level		Waveforms 3 & 4	2.5	5.5	7.5	2.5	9.5	2.5	8.5	ns
t_{PZL}				3.0	6.5	8.5	3.0	10	3.0	9.0	
t_{PHZ}	Output Disable Time from HIGH and LOW Level			2.5	4.5	6.5	2.5	8.0	2.5	7.0	ns
t_{PLZ}				1.5	4.0	6.0	1.5	7.5	1.5	6.5	

AC WAVEFORMS

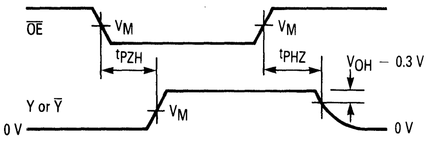

I
VM
VM
tPHL
tPLH
Ȳ
VM
VM

WAVEFORM 1 — FOR INVERTING OUTPUTS

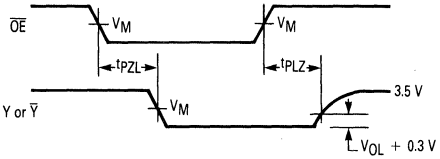

I
VM
VM
tPLH
tPHL
Y
VM
VM

WAVEFORM 2 — FOR NON-INVERTING OUTPUTS

NOTE: For all waveforms, $V_M = 1.5$ V.

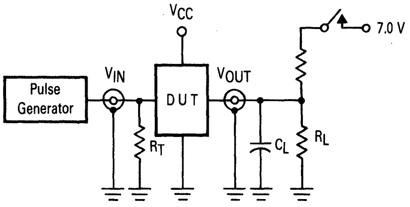

OE
VM
VM
tPZH
tPHZ
VOH − 0.3 V
Y or Ȳ
VM
0 V
0 V

WAVEFORM 3 — 3-STATE OUTPUT ENABLE TIME TO HIGH LEVEL AND OUTPUT DISABLE TIME FROM HIGH LEVEL

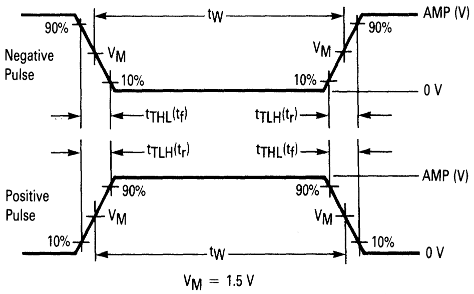

OE
VM
VM
tPZL
tPLZ
3.5 V
Y or Ȳ
VM
VOL + 0.3 V

WAVEFORM 4 — 3-STATE OUTPUT ENABLE TIME TO LOW LEVEL AND OUTPUT DISABLE TIME FROM LOW LEVEL

TEST CIRCUIT AND WAVEFORMS


VCC
7.0 V
Pulse Generator
VIN
DUT
VOUT
RT
CL
RL

TEST CIRCUIT FOR 3-STATE OUTPUTS


tW
AMP (V)
90%
90%
Negative Pulse
VM
VM
10%
10%
0 V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
Positive Pulse
90%
90%
VM
VM
10%
10%
tW
0 V

$V_M = 1.5$ V

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

INPUT PULSE DEFINITION

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

MOTOROLA

MC54F/74F373

OCTAL TRANSPARENT LATCH
(With 3-State Outputs)

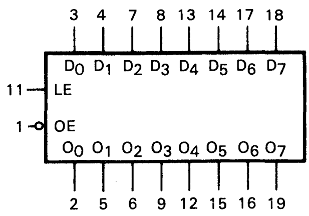
FAST™ SCHOTTKY TTL

OCTAL TRANSPARENT LATCH
(With 3-State Outputs)

DESCRIPTION — The MC54F/74F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

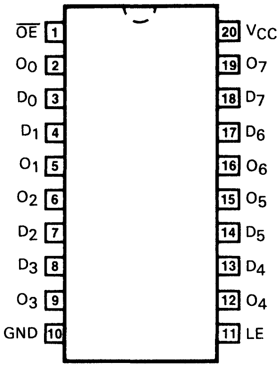
- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

LOGIC SYMBOL


3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 LE
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
2 5 6 9 12 15 16 19

V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM


OE 1
O0 2
D0 3
D1 4
O1 5
O2 6
D2 7
D3 8
O3 9
GND 10
20 VCC
19 O7
18 D7
17 D6
16 O6
15 O5
14 D5
13 D4
12 O4
11 LE

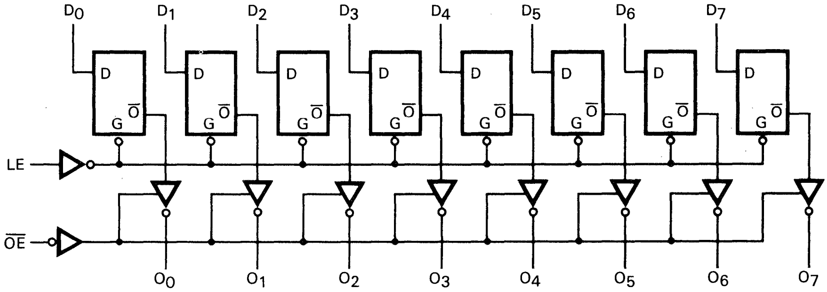
J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

FUNCTIONAL DESCRIPTION — The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100		$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCZ}	Power Supply Current (All Outputs OFF)			35	55	mA	$\overline{OE} = 4.5$ V	V_{CC} = MAX
							D_n, LE = Gnd	

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay D_n to O_n	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns
t_{PHL}		2.0	3.7	5.0	2.0	7.0	2.0	6.0	
t_{PLH}	Propagation Delay LE to O_n	5.0	9.0	11.5	5.0	15	5.0	13	ns
t_{PHL}		3.0	5.2	7.0	3.0	8.5	3.0	8.0	
t_{PZH}	Output Enable Time	2.0	5.0	11	2.0	13.5	2.0	12	ns
t_{PZL}		2.0	5.6	7.5	2.0	10	2.0	8.5	
t_{PHZ}	Output Disable Time	2.0	4.5	6.5	2.0	10	2.0	7.5	ns
t_{PLZ}		2.0	3.8	6.0	2.0	7.0	2.0	6.0	

AC OPERATING REQUIREMENTS:

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Setup Time, HIGH or LOW D_n to LE	2.0			2.0		2.0		ns
t_s (L)		2.0			2.0		2.0		
t_h (H)	Hold Time, High or LOW D_n to LE	3.0			3.0		3.0		
t_h (L)		3.0			3.0		3.0		
t_w (H)	LE Pulse Width HIGH	6.0			6.0		6.0		ns

MOTOROLA

MC54F/74F374

OCTAL D-TYPE FLIP-FLOP (With 3-State Outputs)

FAST™ SCHOTTKY TTL

OCTAL D-TYPE FLIP-FLOP
(With 3-State Outputs)

DESCRIPTION — The MC54F/74F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-triggered Clock**
- **3-State Outputs for Bus Oriented Applications**

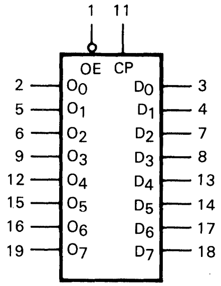
FUNCTIONAL DESCRIPTION — the 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	CP	$\overline{OE}$	O_n
H	↑	L	H
L	↑	L	L
X	X	H	Z

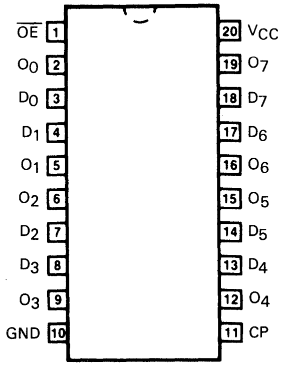
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC SYMBOL


1
11
OE
CP
2
5
6
9
12
15
16
19
O0
O1
O2
O3
O4
O5
O6
O7
D0
D1
D2
D3
D4
D5
D6
D7
3
4
7
8
13
14
17
18

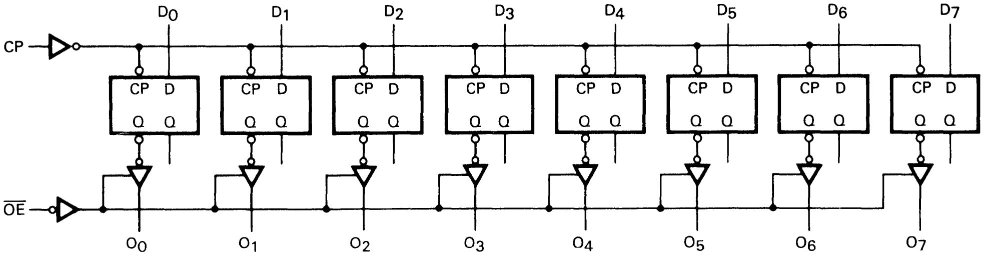
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM


OE 1
O0 2
D0 3
D1 4
O1 5
O2 6
D2 7
D3 8
O3 9
GND 10
20 VCC
19 O7
18 D7
17 D6
16 O6
15 O5
14 D5
13 D4
12 O4
11 CP

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100		$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCZ}	Power Supply Current (All Outputs OFF)			55	86	mA	D_n = Gnd $\overline{OE} = 4.5$ V	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100			60		70		MHz
t_{PLH}	Propagation Delay CP to O_n	4.0	6.5	8.5	4.0	10.5	4.0	10	ns
t_{PHL}		4.0	6.5	8.5	4.0	11	4.0	10	
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14	2.0	12.5	ns
t_{PZL}		2.0	5.8	7.5	2.0	10	2.0	8.5	
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	
t_{PLZ}		2.0	4.3	5.5	2.0	7.5	2.0	6.5	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V		T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Setup Time, HIGH or LOW D_n to CP	2.0		2.5		2.0		ns
t_s (L)		2.0		2.0		2.0		
t_h (H)	Hold Time, HIGH or LOW D_n to CP	2.0		2.0		2.0		
t_h (L)		2.0		2.5		2.0		
t_w (H)	CP Pulse Width, HIGH or LOW	7.0		7.0		7.0		ns
t_w (L)		6.0		6.0		6.0		

MOTOROLA

MC54F/74F378

PARALLEL D REGISTER WITH ENABLE

FAST™ SCHOTTKY TTL

PARALLEL D REGISTER WITH ENABLE

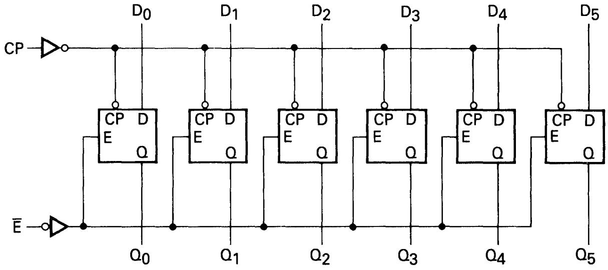
DESCRIPTION — The MC54F/74F378 is a 6-bit register with a buffered common enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input. This circuit is designed to prevent false clocking by transitions on the $\overline{E}$ input.

- **6-BIT HIGH-SPEED PARALLEL REGISTER**
- **POSITIVE EDGE-TRIGGERED D-TYPE INPUTS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULL TTL AND CMOS COMPATIBLE**

LOGIC DIAGRAM

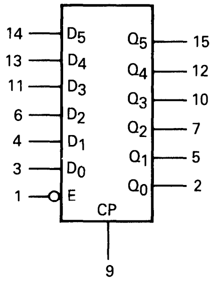

D0
D1
D2
D3
D4
D5
CP
CP D
E Q
E
Q0
Q1
Q2
Q3
Q4
Q5

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}$	CP	D_n	Q_n
H	↑	X	No change
L	↑	H	H
L	↑	L	L

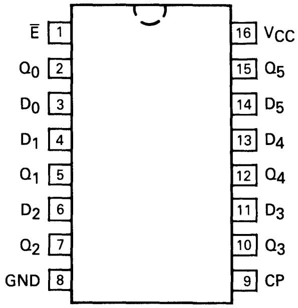
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC SYMBOL


14
13
11
6
4
3
1
D5
D4
D3
D2
D1
D0
E
CP
Q5
Q4
Q3
Q2
Q1
Q0
15
12
10
7
5
2
9

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM


E 1
Q0 2
D0 3
D1 4
Q1 5
D2 6
Q2 7
GND 8
16 VCC
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OL} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			30	45	mA	V_{CC} = MAX, V_{CP} = 0 V	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

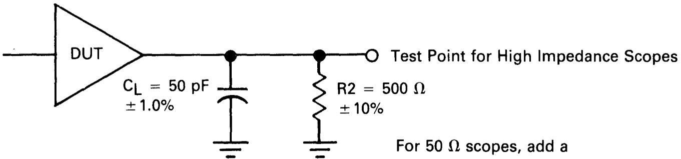
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC}=5.0V±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Input Frequency	80	140		80		80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	9.5 10.5	3.0 3.5	8.5 9.5	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$ $V_{CC} = +5.0$ V MIN	TYP	MAX	54F $T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V ±10% MIN	MAX	74F $T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V ±10% MIN	MAX	UNITS
t_s (H) t_s (L)	Set up Time, HIGH or LOW D_n to CP	4.0 4.0			4.0 4.0		4.0 4.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	0.0 0.0			0.0 0.0		0.0 0.0		
t_s (H) t_s (L)	Set up Time, HIGH or LOW E to CP	6.0 6.0			6.0 6.0		6.0 6.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW E to CP	2.0 2.0			2.0 2.0		2.0 2.0		
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.0 6.0			4.0 6.0		4.0 6.0		ns

AC TEST CIRCUIT


DUT
$C_L = 50$ pF
±1.0%
R2 = 500 Ω
±10%
Test Point for High Impedance Scopes

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MC54F/74F379

QUAD PARALLEL REGISTER WITH ENABLE

FAST™ SCHOTTKY TTL

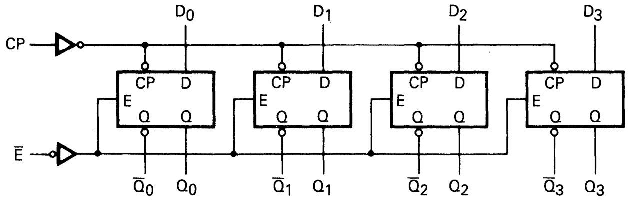
QUAD PARALLEL REGISTER

DESCRIPTION — The MC54F/74F379 is a 4-bit register with a buffered common enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

The 'F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed. This circuit is designed to prevent false clocking by transitions on the $\overline{E}$ input.

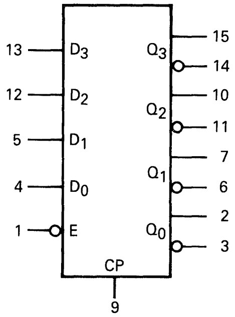
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **BUFFERED COMMON ENABLE INPUT**
- **TRUE AND COMPLEMENT OUTPUTS**

LOGIC DIAGRAM



CP
$\overline{E}$
D_0
D_1
D_2
D_3
CP D
E
Q Q
$\overline{Q}_0$ Q_0
$\overline{Q}_1$ Q_1
$\overline{Q}_2$ Q_2
$\overline{Q}_3$ Q_3

LOGIC SYMBOL



13 D_3
12 D_2
5 D_1
4 D_0
1 E
Q_3 15 14
Q_2 10 11
Q_1 7 6
Q_0 2 3
CP
9

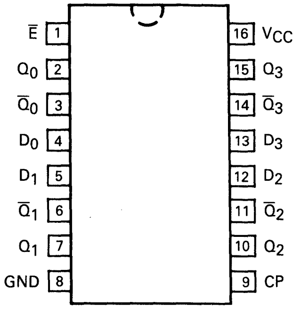
V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	H	H	L
L	↑	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
NC = No Change

CONNECTION DIAGRAM



$\overline{E}$ 1
Q_0 2
$\overline{Q}_0$ 3
D_0 4
D_1 5
$\overline{Q}_1$ 6
Q_1 7
GND 8
16 V_{CC}
15 Q_3
14 $\overline{Q}_3$
13 D_3
12 D_2
11 $\overline{Q}_2$
10 Q_2
9 CP

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OL} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			28	40	mA	V_{CC} = MAX, D = $\overline{E}$ = GND, CP = ⎍	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

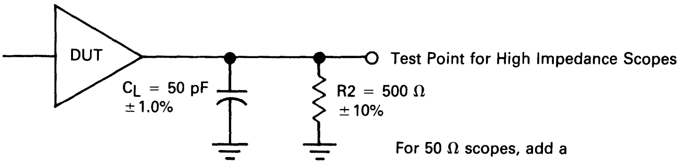
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0V ±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100	140		90		100		MHz
t_{PLH}	Propagation Delay	3.5*	5.0	6.5	3.5	8.5	3.5*	7.5	ns
t_{PHL}	CP to Q_n, $\overline{Q}_n$	5.0	6.5	8.5	5.0	10.5	5.0	9.5	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V		T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	3.0 3.0		3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	1.0 1.0		1.0 1.0		1.0 1.0		
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{E}$ to CP	6.0 6.0		6.0 6.0		6.0 6.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{E}$ to CP	2.0 2.0		2.0 2.0		2.0 2.0		
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.0 5.0		4.0 5.0		4.0 5.0		ns

AC TEST CIRCUIT


DUT
C_L = 50 pF ±1.0%
R2 = 500 Ω ±10%
Test Point for High Impedance Scopes

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

Fig. 1

MOTOROLA

MC54F/74F381

Advance Information

4-BIT ARITHMETIC LOGIC UNIT

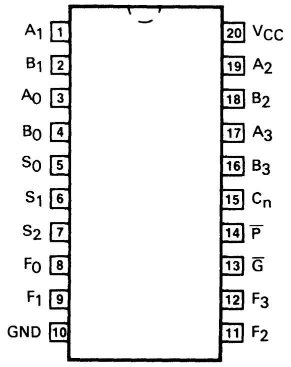
DESCRIPTION — The MC54F/74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. Carry Propagate and Generate outputs are provided for use with the F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the F382 ALU data sheet.

- **Low Input Loading Minimizes Drive Requirements**
- **Performs Six Arithmetic and Logic Functions**
- **Selectable Low (Clear) and High (Preset) Functions**
- **Carry Generate and Propagate Outputs for use with Carry Lookahead Generator**

4-BIT ARITHMETIC LOGIC UNIT

FAST™ SCHOTTKY TTL

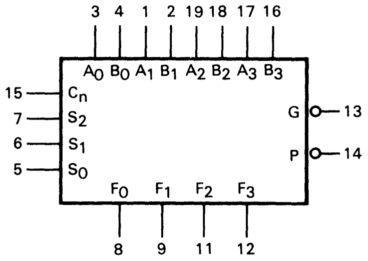
CONNECTION DIAGRAM



A_1 1
B_1 2
A_0 3
B_0 4
S_0 5
S_1 6
S_2 7
F_0 8
F_1 9
GND 10
20 V_{CC}
19 A_2
18 B_2
17 A_3
16 B_3
15 C_n
14 $\overline{P}$
13 $\overline{G}$
12 F_3
11 F_2

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

LOGIC SYMBOL



3 4 1 2 19 18 17 16
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
15 C_n
7 S_2
6 S_1
5 S_0
G 13
P 14
F_0 F_1 F_2 F_3
8 9 11 12

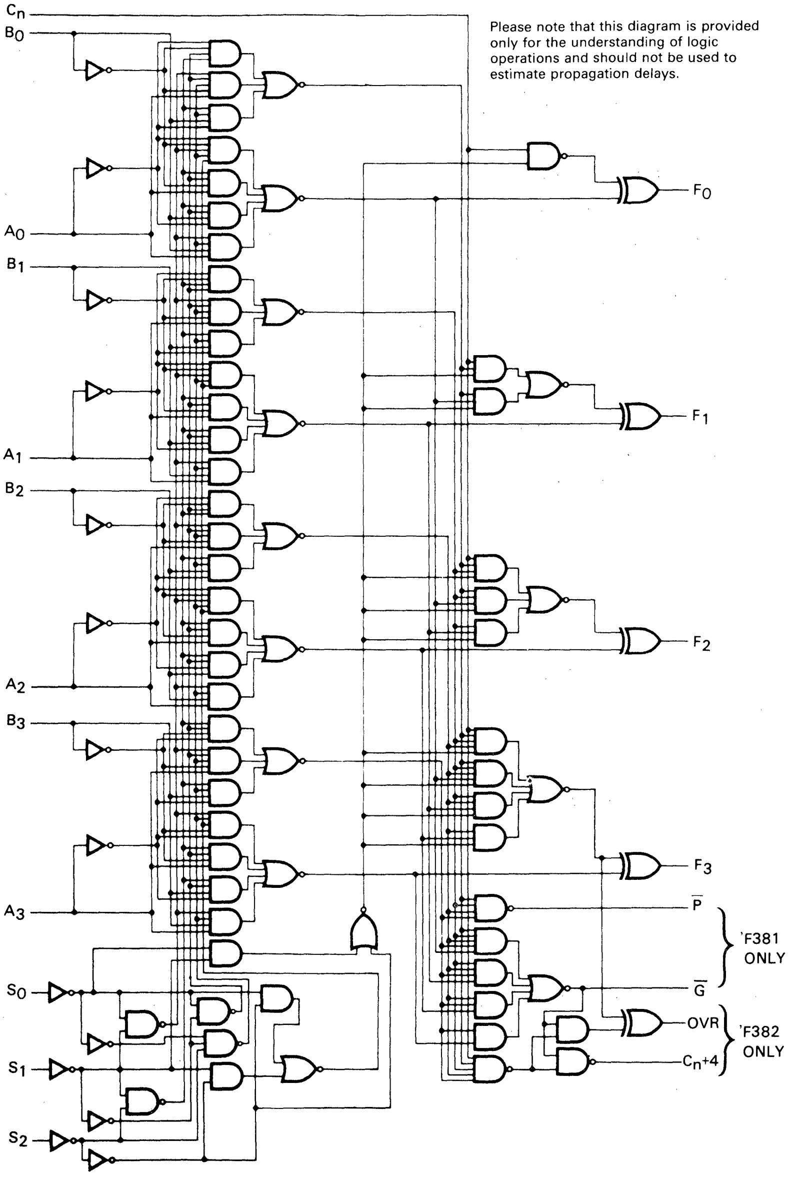
V_{CC} = Pin 20
GND = Pin 10

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM


Cn
B0
A0
B1
A1
B2
A2
B3
A3
S0
S1
S2
F0
F1
F2
F3
P
G
'F381 ONLY
OVR
Cn+4
'F382 ONLY

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current S_0–S_2 Inputs				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
	Other Inputs				−2.4	mA	$V_{IN} = 0.5$ V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			59	89	mA	S_0–S_2 = GND; Other Inputs HIGH	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — Signals applied to the Select inputs S_0–S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH operands, LOW for active-LOW operands) into the C_n input of the least significant package.

The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the F182 carry lookahead generator for expansion to longer word length, as shown in Figure 1. Note that an F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Figure 2.

FUNCTION SELECT TABLE

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A+B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level L = LOW Voltage Level

FIGURE 1 — 16-BIT LOOKAHEAD CARRY ALU EXPANSION

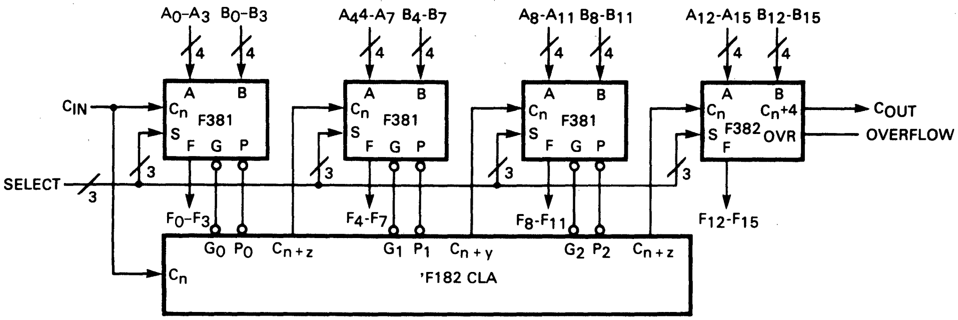

A0-A3 B0-B3
A4-A7 B4-B7
A8-A11 B8-B11
A12-A15 B12-B15
4
C_IN
SELECT
3
A
B
Cn
F381
S
F G P
F382
Cn+4
OVR
COUT
OVERFLOW
F0-F3
F4-F7
F8-F11
F12-F15
G0 P0
G1 P1
G2 P2
Cn+z
Cn+y
Cn
'F182 CLA

FIGURE 2 — 16-BIT DELAY TABULATION

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to $\overline{P}$	7.2 ns	7.2 ns
$\overline{P_i}$ to C_{n+j} ('F182)	6.2 ns	6.2 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	2.5 2.5	8.1 5.7	12 8.0	2.5 2.5	15 11	2.5 2.5	13 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	15 11	4.0 3.5	18 14	4.0 3.5	16 12	ns
t_{PLH} t_{PHL}	Propagation Delay S_i to F_i	4.5 4.0	8.3 8.2	20 13	4.5 4.0	23.5 16	4.5 4.0	21.5 14	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to $\overline{G}$	3.0 4.0	6.4 6.8	9.0 10	3.0 4.0	12 13	3.0 4.0	10 11	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to $\overline{P}$	2.5 3.5	7.2 6.5	10.5 9.5	2.5 3.5	13.5 12.5	2.5 3.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_i to $\overline{G}$ or $\overline{P}$	4.0 4.5	7.8 10.2	12 13.5	4.0 4.5	15 16.5	4.0 4.5	13 14.5	ns

TRUTH TABLE

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
$A \oplus B$	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
$A + B$	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = HIGH Voltage Level
0 = LOW Voltage Level
X = Immaterial

MOTOROLA

MC54F/74F382

4-BIT ARITHMETIC LOGIC UNIT

FAST™ SCHOTTKY TTL

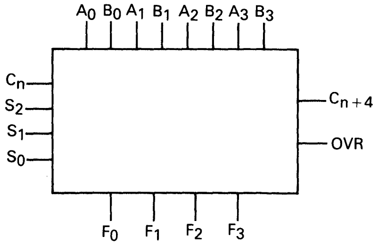
Advance Information

4-BIT ARITHMETIC LOGIC UNIT

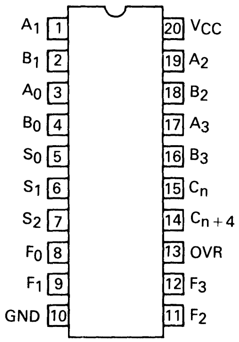
DESCRIPTION — The MC54/74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the F381 data sheet.

- Performs Six Arithmetic and Logic Functions
- Selectable Low (Clear) and High (Preset) Functions
- LOW Input Loading Minimizes Drive Requirements
- Carry Output for Ripple Expansion
- Overflow Output for Twos Complement Arithmetic

LOGIC SYMBOL



CONNECTION DIAGRAM



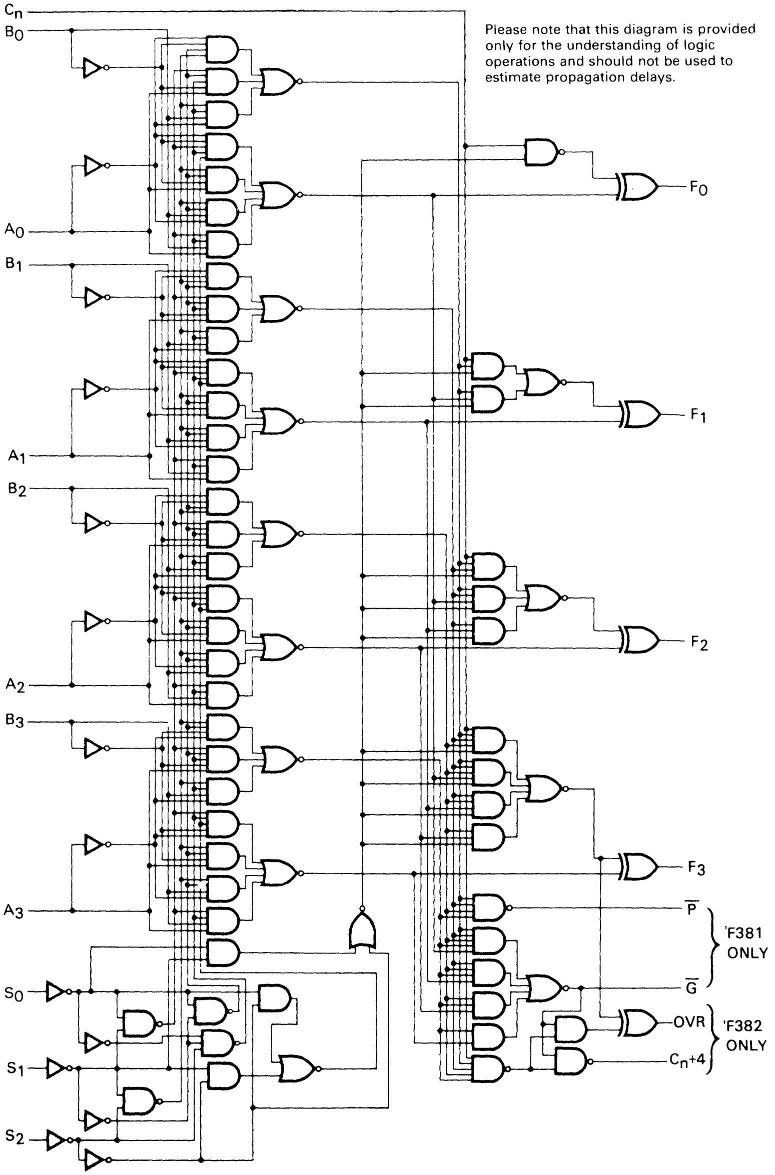
J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM


Cn
B0
A0
B1
A1
B2
A2
B3
A3
S0
S1
S2
F0
F1
F2
F3
P
'F381
ONLY
G
OVR
'F382
ONLY
Cn+4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current S_0–S_2 Inputs				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
	Other Inputs				−2.4	mA		
	C_n Input				−3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			54	81	mA	S_0, C_n = HIGH; Other Inputs GND	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — Signals applied to the Select inputs S_0–S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in twos complement operation. Typical delays for Figure 1 are given in Figure 2.

FUNCTION SELECT TABLE

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	A+B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level L = LOW Voltage Level

FIGURE 1 — 16-BIT RIPPLE CARRY ALU EXPANSION

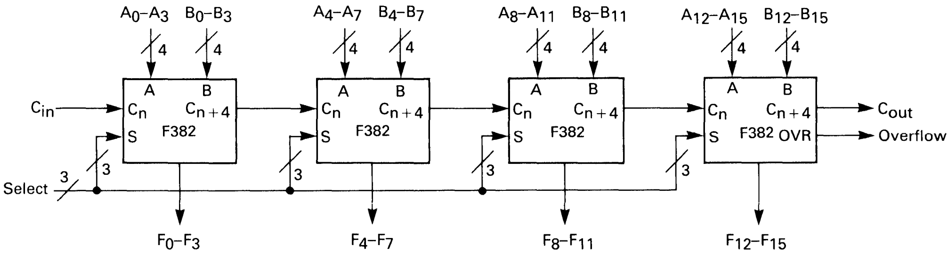

A_0–A_3
B_0–B_3
A_4–A_7
B_4–B_7
A_8–A_{11}
B_8–B_{11}
A_{12}–A_{15}
B_{12}–B_{15}
4
A
B
C_{in}
C_n
C_{n+4}
S
F382
OVR
C_{out}
Overflow
Select
3
F_0–F_3
F_4–F_7
F_8–F_{11}
F_{12}–F_{15}

FIGURE 2 — 16-BIT DELAY TABULATION

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

AC CHARACTERISTICS

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	3.0	8.1	12	3.0	15	3.0	13	ns
t_{PHL}	C_n to F_i	2.5	5.7	8.0	2.5	11	2.5	9.0	
t_{PLH}	Propagation Delay	4.0	10.4	15	4.0	18	4.0	16	ns
t_{PHL}	Any A or B to Any F	3.5	8.2	11	3.5	14	3.5	12	
t_{PLH}	Propagation Delay	6.0	11	15	6.0	21	6.0	16	ns
t_{PHL}	S_i to F_i	4.0	8.2	20.5	4.0	23.5	4.0	21.5	
t_{PLH}	Propagation Delay	3.5	6.0	8.5	3.5	11.5	3.5	9.5	ns
t_{PHL}	A_i or B_i to C_{n+4}	3.0	6.5	9.0	3.0	12.5	3.0	10.5	
t_{PLH}	Propagation Delay	7.0	12.5	16.5	7.0	19.5	7.0	17.5	ns
t_{PHL}	S_i to OVR or C_{n+4}	4.5	9.0	12	4.5	15	4.5	13	
t_{PLH}	Propagation Delay	2.5	5.6	8.0	2.5	11	2.5	9.0	ns
t_{PHL}	C_n to C_{n+4}	2.5	6.3	9.0	2.5	12	2.5	10	
t_{PLH}	Propagation Delay	3.5	8.0	11	3.5	14	3.5	12	ns
t_{PHL}	C_n to OVR	3.5	7.1	10	3.5	13	3.5	11	
t_{PLH}	Propagation Delay	6.5	11.5	15.5	6.5	18.5	6.5	16.5	ns
t_{PHL}	A_i or B_i to OVR	5.5	8.0	10.5	5.5	13.5	5.5	11.5	

TRUTH TABLE

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	1	1	1	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A⊕B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				X	1	1	0	0	0	0	1	1
				1	1	0	1	1	1	1	1	1
A+B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	X	0	0	0	0	0	0	1	1
				X	0	1	0	0	0	0	0	0
				X	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	X	0	0	1	1	1	1	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

1 = HIGH Voltage Level
0 = LOW Voltage Level
X = Immaterial

MOTOROLA

MC54F/74F398

QUAD 2-PORT REGISTER

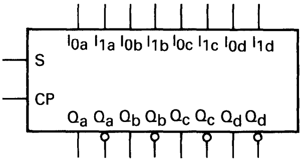
FAST™ SCHOTTKY TTL

QUAD 2-PORT REGISTER

DESCRIPTION — The MC54F/74F398 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock.

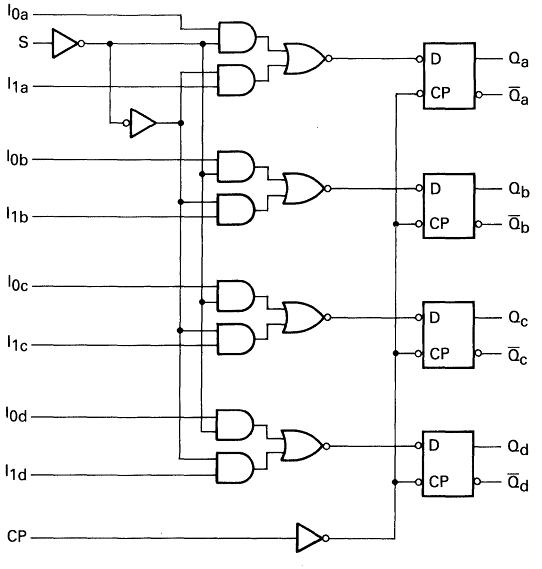
- **Select Inputs from Two Data Sources**
- **Fully Positive Edge-Triggered Operation**
- **Both True and Complement Outputs**

LOGIC SYMBOL



S
CP
I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d}
Q_a $\overline{Q}_a$ Q_b $\overline{Q}_b$ Q_c $\overline{Q}_c$ Q_d $\overline{Q}_d$

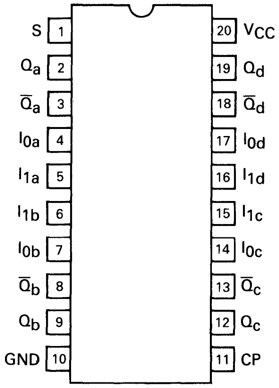
LOGIC DIAGRAM



I_{0a}
S
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
CP
D
CP
Q_a
$\overline{Q}_a$
Q_b
$\overline{Q}_b$
Q_c
$\overline{Q}_c$
Q_d
$\overline{Q}_d$

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAMS



S 1
Q_a 2
$\overline{Q}_a$ 3
I_{0a} 4
I_{1a} 5
I_{1b} 6
I_{0b} 7
$\overline{Q}_b$ 8
Q_b 9
GND 10
20 V_{CC}
19 Q_d
18 $\overline{Q}_d$
17 I_{0d}
16 I_{1d}
15 I_{1c}
14 I_{0c}
13 $\overline{Q}_c$
12 Q_c
11 CP

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

FUNCTIONAL DESCRIPTION

The MC54/74F398 is a high-speed quad 2-port register. It will select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The MC54/74F398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	µA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			25	38	mA	V_{CC} = MAX	V_{IN} = GND CP = _/‾

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

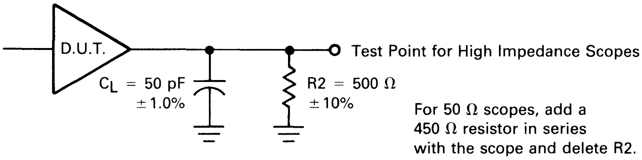
AC CHARACTERISTICS

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Input Clock Frequency	100	140		80		100		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$	3.0 3.0	5.7 6.8	7.5 9.5	3.0 3.0	9.5 11.5	3.0 3.0	8.5 10.0	ns

AC OPERATING REQUIREMENTS

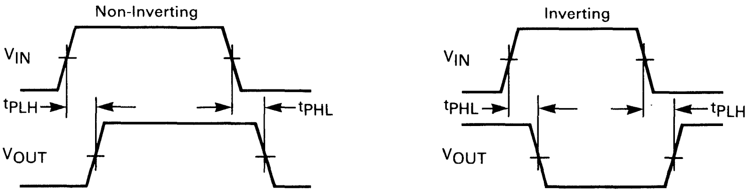
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I_n to CP	3.0 3.0			4.5 4.5		3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I_n to CP	1.0 1.0			1.5 1.5		1.0 1.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S to CP ('F398)	7.5 7.5			10.5 10.5		8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S to CP	0 0			0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 5.0			4.0 7.0		4.0 5.0		ns

AC TEST CIRCUIT


D.U.T.
C_L = 50 pF
±1.0%
R2 = 500 Ω
±10%
Test Point for High Impedance Scopes

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

PROPAGATION DELAY MEASUREMENTS


Non-Inverting
V_{IN}
t_{PLH}
t_{PHL}
V_{OUT}
Inverting
V_{IN}
t_{PHL}
t_{PLH}
V_{OUT}

MC54F/74F399

QUAD 2-PORT REGISTER

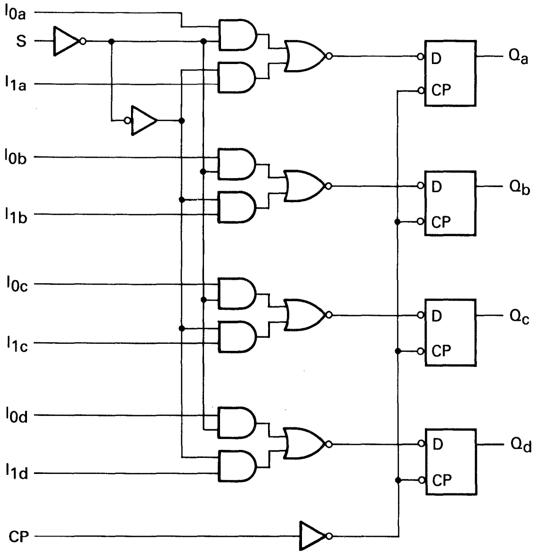
FAST™ SCHOTTKY TTL

QUAD 2-PORT REGISTER

DESCRIPTION — The MC54F/74F399 is a logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The MC54/74F399 is the 16-pin version of the MC54/74F398, with only the Q outputs of the flip-flops available.

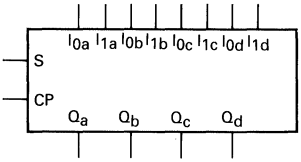
- **Select Inputs from Two Data Sources**
- **Fully Positive Edge-Triggered Operation**

LOGIC DIAGRAM

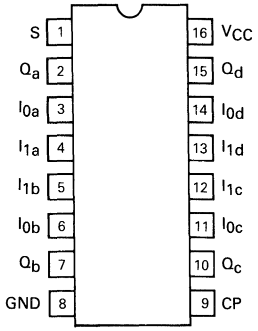

I_{0a}
S
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
CP
D
CP
Q_a
Q_b
Q_c
Q_d

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC SYMBOL


I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d}
S
CP
Q_a Q_b Q_c Q_d

CONNECTION DIAGRAM


S 1
Q_a 2
I_{0a} 3
I_{1a} 4
I_{1b} 5
I_{0b} 6
Q_b 7
GND 8
16 V_{CC}
15 Q_d
14 I_{0d}
13 I_{1d}
12 I_{1c}
11 I_{0c}
10 Q_c
9 CP

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

FUNCTIONAL DESCRIPTION

The MC54F/74F399 is a high-speed quad 2-port register. It will select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTION TABLE

INPUTS			OUTPUTS
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4		V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 20$ mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CC}	Power Supply Current			22	34	mA	V_{CC} = MAX	V_{IN} = GND CP = ↑

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

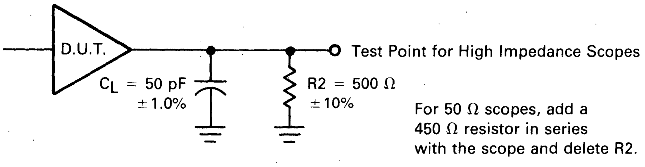
AC CHARACTERISTICS

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			$T_A, V_{CC} =$ MIL $C_L = 50\ pF$		$T_A, V_{CC} =$ COM $C_L = 50\ pF$		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Input Clock Frequency	100	140		80		100		MHz
t_{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	9.5	3.0	8.5	ns
t_{PHL}	CP to Q	3.0	6.8	9.5	3.0	11.5	3.0	10.0	

AC OPERATING REQUIREMENTS

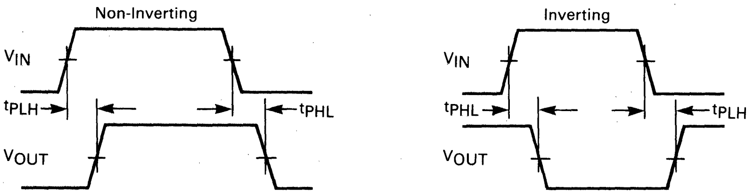
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			$T_A, V_{CC} =$ MIL		$T_A, V_{CC} =$ COM		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$	Setup Time, HIGH or LOW	3.0			4.5		3.0		ns
$t_s(L)$	I_n to CP	3.0			4.5		3.0		
$t_h(H)$	Hold Time, HIGH or LOW	1.0			1.5		1.0		
$t_h(L)$	I_n to CP	1.0			1.5		1.0		
$t_s(H)$	Setup Time, HIGH or LOW	7.5			9.5		8.5		ns
$t_s(L)$	S to CP	7.5			9.5		8.5		
$t_h(H)$	Hold Time, HIGH or LOW	0			0		0		
$t_h(L)$	S to CP	0			0		0		
$t_w(H)$	CP Pulse Width	4.0			4.0		4.0		ns
$t_w(L)$	HIGH or LOW	5.0			7.0		5.0		

AC TEST CIRCUIT


D.U.T.
Test Point for High Impedance Scopes
$C_L = 50\ pF$ ±1.0%
R2 = 500 Ω ±10%

For 50 Ω scopes, add a 450 Ω resistor in series with the scope and delete R2.

PROPAGATION DELAY MEASUREMENTS


Non-Inverting
V_{IN}
t_{PLH}
t_{PHL}
V_{OUT}
Inverting
V_{IN}
t_{PHL}
t_{PLH}
V_{OUT}

MOTOROLA

MC54F/74F521

8-BIT IDENTITY COMPARATOR

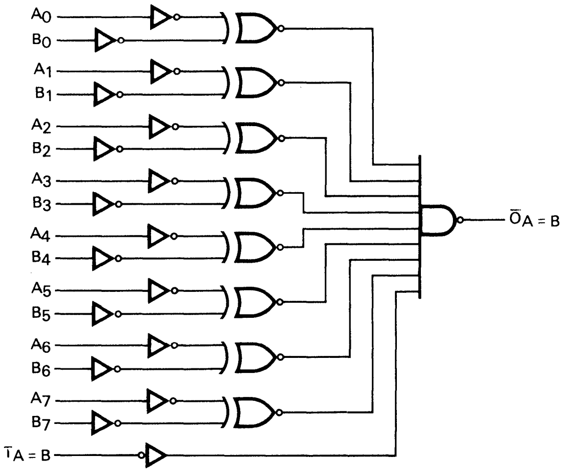
FAST™ SCHOTTKY TTL

8-BIT IDENTITY COMPARATOR

DESCRIPTION — The MC54F/74F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-LOW enable input.

- **Compares Two 8-Bit Words in 6.5 ns Typ**
- **Expandable to Any Word Length**
- **20-Pin Package**

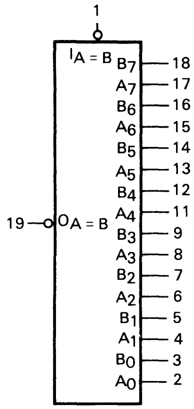
LOGIC DIAGRAM



A_0
B_0
A_1
B_1
A_2
B_2
A_3
B_3
A_4
B_4
A_5
B_5
A_6
B_6
A_7
B_7
$\overline{I}_{A=B}$
$\overline{O}_{A=B}$

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

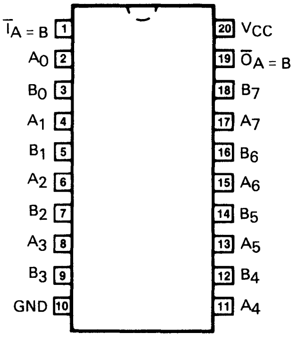
LOGIC SYMBOL



1
$I_{A=B}$
19
$O_{A=B}$
B_7 18
A_7 17
B_6 16
A_6 15
B_5 14
A_5 13
B_4 12
A_4 11
B_3 9
A_3 8
B_2 7
A_2 6
B_1 5
A_1 4
B_0 3
A_0 2

V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM



$\overline{I}_{A=B}$ 1
A_0 2
B_0 3
A_1 4
B_1 5
A_2 6
B_2 7
A_3 8
B_3 9
GND 10
20 V_{CC}
19 $\overline{O}_{A=B}$
18 B_7
17 A_7
16 B_6
15 A_6
14 B_5
13 A_5
12 B_4
11 A_4

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			21	32	mA	$\overline{I}_A$ = B = Gnd	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

TRUTH TABLE

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

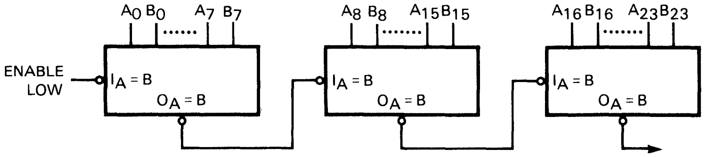
H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0$ V ±10% $C_L = 50$ pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay	2.5	6.5	10	2.5	15	2.5	11	ns
t_{PHL}	A_n or B_n to $\overline{O}_{A=B}$	3.0	6.5	10	3.0	12	3.0	11	
t_{PLH}	Propagation Delay	2.5	4.5	6.5	2.5	8.5	2.5	7.5	ns
t_{PHL}	$\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.5	5.0	9.0	3.5	10	3.5	10	

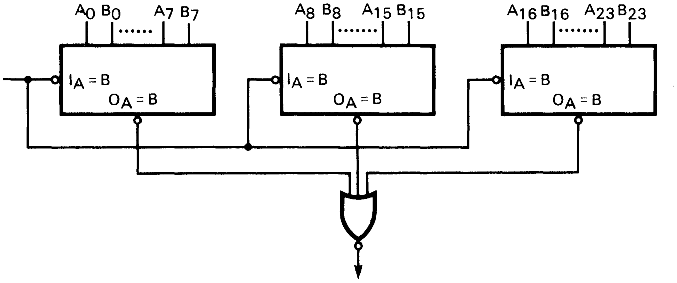
APPLICATIONS

Ripple Expansion



A_0 B_0 A_7 B_7
A_8 B_8 A_{15} B_{15}
A_{16} B_{16} A_{23} B_{23}
ENABLE LOW
$I_{A=B}$
$O_{A=B}$
$I_{A=B}$
$O_{A=B}$
$I_{A=B}$
$O_{A=B}$

Parallel Expansion



A_0 B_0 A_7 B_7
A_8 B_8 A_{15} B_{15}
A_{16} B_{16} A_{23} B_{23}
$I_{A=B}$
$O_{A=B}$
$I_{A=B}$
$O_{A=B}$
$I_{A=B}$
$O_{A=B}$

MC54F/74F533

OCTAL TRANSPARENT LATCH
(With 3-State Outputs)

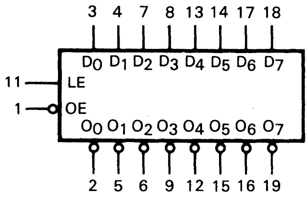
DESCRIPTION — The MC54F/74F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state. The F533 is the same as the F373, except that the outputs are inverted. For description and logic diagram please see the F373 data sheet.

- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

OCTAL TRANSPARENT LATCH
(With 3-State Outputs)

FAST™ SCHOTTKY TTL

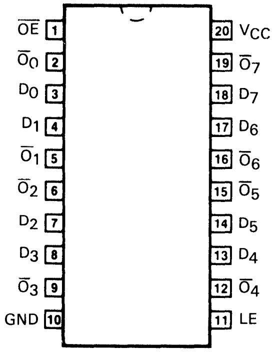
LOGIC SYMBOL



3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11
LE
1
OE
O0 O1 O2 O3 O4 O5 O6 O7
2 5 6 9 12 15 16 19

V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM



$\overline{OE}$ 1
$\overline{O}_0$ 2
D_0 3
D_1 4
$\overline{O}_1$ 5
$\overline{O}_2$ 6
D_2 7
D_3 8
$\overline{O}_3$ 9
GND 10
20 V_{CC}
19 $\overline{O}_7$
18 D_7
17 D_6
16 $\overline{O}_6$
15 $\overline{O}_5$
14 D_5
13 D_4
12 $\overline{O}_4$
11 LE

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.75
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCZ}	Power Supply Current			41	61	mA	$\overline{OE}$ = 4.5 V D_n, LE = Gnd	V_{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0 3.0	9.0 7.0	4.0 3.0	12 9.0	4.0 3.0	10 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0 3.0	11 7.0	5.0 3.0	14 9.0	5.0 3.0	13 8.0	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	10 6.5	2.0 2.0	12.5 9.0	2.0 2.0	11 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	6.0 5.5	2.0 2.0	8.5 7.5	2.0 2.0	7.0 6.5	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V		T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0		2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0		3.0 3.0		3.0 3.0		ns
t_w (H)	LE Pulse Width HIGH	6.0		6.0		6.0		ns

MC54F/74F534

OCTAL D-TYPE FLIP-FLOP
(With 3-State Outputs)

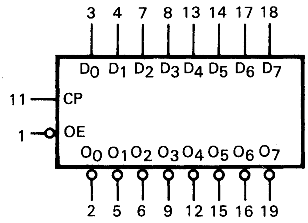
DESCRIPTION — The MC54F/74F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-triggered Clock**
- **3-State Outputs for Bus Oriented Applications**

OCTAL D-TYPE FLIP-FLOP
(With 3-State Outputs)

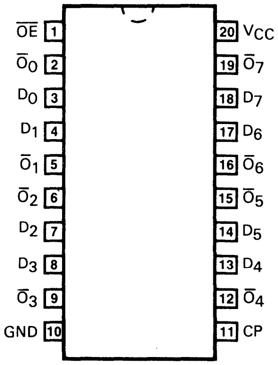
FAST™ SCHOTTKY TTL

LOGIC SYMBOL


3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11
CP
1
OE
O0 O1 O2 O3 O4 O5 O6 O7
2 5 6 9 12 15 16 19

V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM

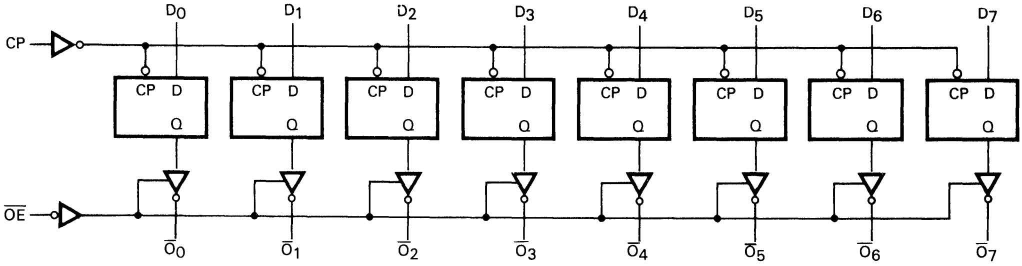

OE 1
Ō0 2
D0 3
D1 4
Ō1 5
Ō2 6
D2 7
D3 8
Ō3 9
GND 10
20 VCC
19 Ō7
18 D7
17 D6
16 Ō6
15 Ō5
14 D5
13 D4
12 Ō4
11 CP

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION — The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3		V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage			0.35	0.5	V	$I_{OL} = 24$ mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	$V_{OUT} = 2.7$ V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	$V_{OUT} = 0.5$ V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	$V_{IN} = 2.7$ V	V_{CC} = MAX
					100		$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.6	mA	$V_{IN} = 0.5$ V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	$V_{OUT} = 0$ V	V_{CC} = MAX
I_{CCZ}	Power Supply Current			55	86	mA	D_n = Gnd $\overline{OE} = 4.5$ V	V_{CC} = MAX

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50\ pF$		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$ $C_L = 50\ pF$		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100			60		70	MHz	
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	4.0	6.5	8.5	4.0	10.5	4.0	10	ns
t_{PHL}		4.0	6.5	8.5	4.0	11	4.0	10	
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14	2.0	12.5	
t_{PZL}		2.0	5.8	7.5	2.0	10	2.0	8.5	
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	ns
t_{PLZ}		2.0	4.3	5.5	2.0	7.5	2.0	6.5	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			$T_A = -55$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$		$T_A = 0$ to $+70°C$ $V_{CC} = 5.0\ V \pm 10\%$		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H)	Setup Time, HIGH or LOW D_n to CP	2.0			2.5		2.0		ns
t_s (L)		2.0			2.0		2.0		
t_h (H)	Hold Time, HIGH or LOW D_n to CP	2.0			2.0		2.0		
t_h (L)		2.0			2.5		2.0		
t_w (H)	CP Pulse Width HIGH or LOW	5.0			7.0		7.0		ns
t_w (L)		5.0			6.0		6.0		

MOTOROLA

MC54F/74F537

Product Preview

1-OF-10 DECODER
(With 3-State Outputs)

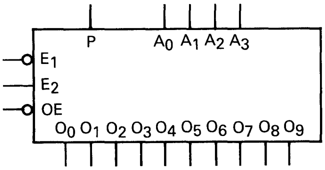
1-OF-10 DECODER
WITH 3-STATE OUTPUTS

FAST™ SCHOTTKY TTL

DESCRIPTION — The MC54/74F537 is one-of-ten decoder/demultiplexer with four active HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active LOW or active HIGH. The MC54/74F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input enables, active HIGH E_2 and active LOW $\overline{E}_1$, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

- **Demultiplexing Capability**
- **3-State Outputs**
- **Multiple Input Enable for Expansion**
- **Polarity Control Input**

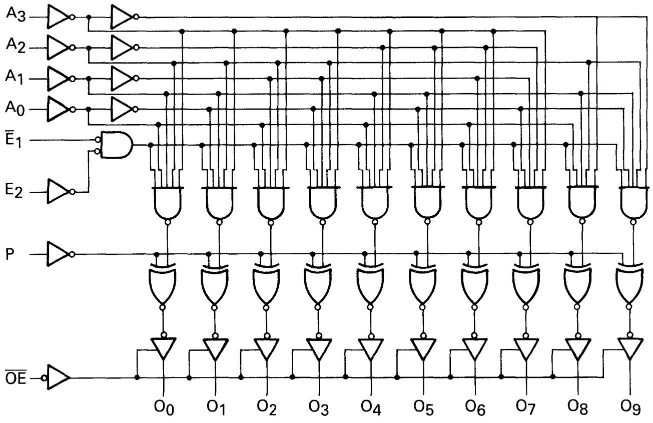
LOGIC SYMBOL



P
A_0 A_1 A_2 A_3
E_1
E_2
OE
O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7 O_8 O_9

V_{CC} = Pin 20
GND = Pin 10

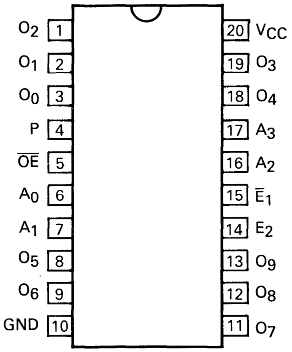
LOGIC DIAGRAM



A_3
A_2
A_1
A_0
$\overline{E}_1$
E_2
P
$\overline{OE}$
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
O_8
O_9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAM
DIP (TOP VIEW)



O_2 1
O_1 2
O_0 3
P 4
$\overline{OE}$ 5
A_0 6
A_1 7
O_5 8
O_6 9
GND 10
20 V_{CC}
19 O_3
18 O_4
17 A_3
16 A_2
15 $\overline{E}_1$
14 E_2
13 O_9
12 O_8
11 O_7

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7			V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CCZ}	Power Supply Current			44	66	mA	V_{CC} = MAX: A_0–A_3, $\overline{E}_1$ = GND $\overline{OE}$, E_2, P = HIGH	

AC CHARACTERISTICS

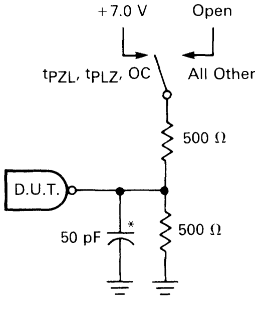
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	4.0 3.5	11 7.5	16 11			4.0 3.5	17 12	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to O_n	4.0 3.5	8.5 6.5	14.5 9.0			4.0 3.5	15.5 10	
t_{PLH} t_{PHL}	Propagation Delay E_2 to O_n	6.0 4.0	11 10	16 14			6.0 4.0	17 15	ns
t_{PLH} t_{PHL}	Propagation Delay P to O_n	5.0 4.0	11.5 11	18 16			5.0 4.0	20 17	
t_{PZH} t_{PLZ}	Output Enable Time $\overline{OE}$ to O_n	3.0 5.0	5.5 9.0	10.5 13			3.0 5.0	11.5 14	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0 1.5	4.0 5.0	6.0 7.0			2.0 1.5	7.0 8.0	

TRUTH TABLE

FUNCTION	INPUTS							OUTPUTS									
	$\overline{OE}$	$\overline{E}_1$	E_2	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
High Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	X	X	X	X	Outputs Equal P Input									
	L	X	L	X	X	X	X										
Active HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L
	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	H	X	X	L	L	L	L	L	L	L	L	L	L
Active LOW Output (P = H)	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
	L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H
	L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

AC TEST CIRCUIT



*Includes jig and probe capacitance

FIGURE 1 — TEST LOAD

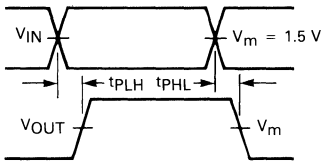


FIGURE 2 — WHETHER RESPONSE IS INVERTING OR NONINVERTING DEPENDS ON SPECIFIC TRUTH TABLE CONDITIONS

MOTOROLA

MC54F/74F538

1-OF-8 DECODER
WITH 3-STATE OUTPUTS

FAST™ SCHOTTKY TTL

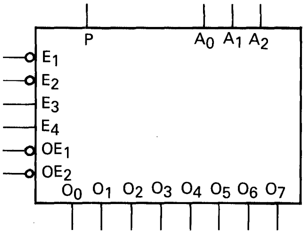
Product Preview

1-OF-8 DECODER
(With 3-State Outputs)

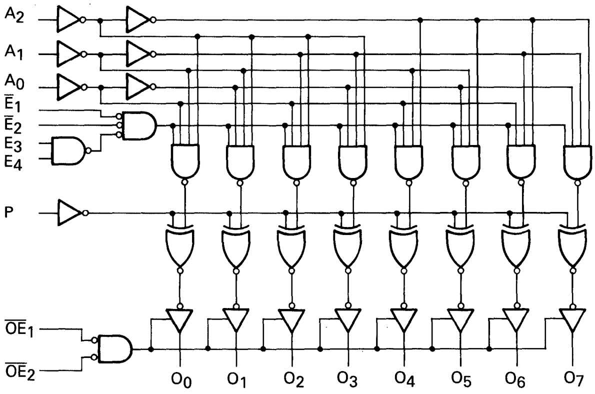
DESCRIPTION — The MC54/74F538 decoder/demultiplexer accepts three Address (A_0–A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH Signal on either of the active LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

- **Output Polarity Control**
- **Data Demultiplexing Capability**
- **Multiple Enables for Expansion**
- **3-State Outputs**

LOGIC SYMBOL

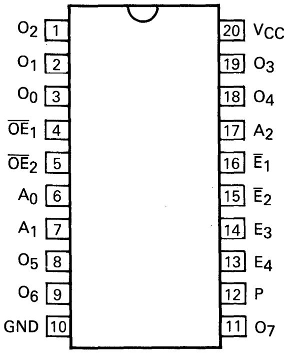

P
A0 A1 A2
E1
E2
E3
E4
OE1
OE2
O0 O1 O2 O3 O4 O5 O6 O7

V_{CC} = Pin 20
GND = Pin 10


A2
A1
A0
Ē1
Ē2
E3
E4
P
OE1
OE2
O0
O1
O2
O3
O4
O5
O6
O7

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAM
DIP (TOP VIEW)


O2 1
O1 2
O0 3
OE1 4
OE2 5
A0 6
A1 7
O5 8
O6 9
GND 10
20 VCC
19 O3
18 O4
17 A2
16 Ē1
15 Ē2
14 E3
13 E4
12 P
11 O7

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7			V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	µA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	µA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CCZ}	Power Supply Current			37	56	mA	V_{CC} = MAX A_0–A_2, $\overline{E}_1$, $\overline{E}_2$ = GND $\overline{OE}_1$, $\overline{OE}_2$, E_3, E_4, P = HIGH	

AC CHARACTERISTICS

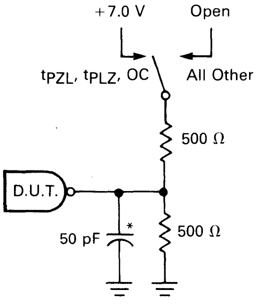
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	4.5 3.5	11 7.5	16 11			4.5 3.5	17 12	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to O_n	4.5 3.5	8.5 6.5	15 9.0			4.5 3.5	16 10	
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to O_n	5.5 4.0	11 10	16 14			5.5 4.0	17 15	ns
t_{PLH} t_{PHL}	Propagation Delay P to O_n	5.5 4.5	11.5 11	18 16			5.5 4.5	20 17	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	3.0 5.0	5.5 9.0	10 13			3.0 5.0	11 14	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	2.0 1.5	4.0 5.0	6.0 8.0			2.0 1.5	7.0 9.0	

TRUTH TABLE

FUNCTION	INPUTS									OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

AC TEST CIRCUIT



*Includes jig and probe capacitance

FIGURE 1 — TEST LOAD

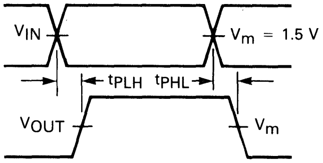


FIGURE 2 — WHETHER RESPONSE IS INVERTING OR NONINVERTING DEPENDS ON SPECIFIC TRUTH TABLE CONDITIONS

MOTOROLA

MC54F/74F539

DUAL 1-OF-4 DECODER WITH 3-STATE OUTPUTS

FAST™ SCHOTTKY TTL

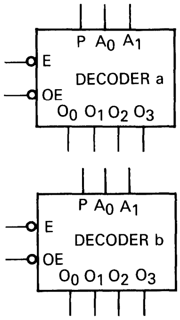
Product Preview

DUAL 1-OF-4 DECODER
(With 3-State Outputs)

DESCRIPTION — The MC54/74F539 contains two independent decoders. Each accepts two Address (A_0–A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH (P = L) or active LOW (P = H). An active LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH Signal on the active LOW Output Enable ($\overline{OE}$) input forces the 3-state outputs to the high impedance state.

- **Demultiplexing Capability**
- **3-State Outputs**
- **Two Completely Independent 1-of-4 Decoders**
- **Input Clamp Diodes Limit High Speed Termination Effects**

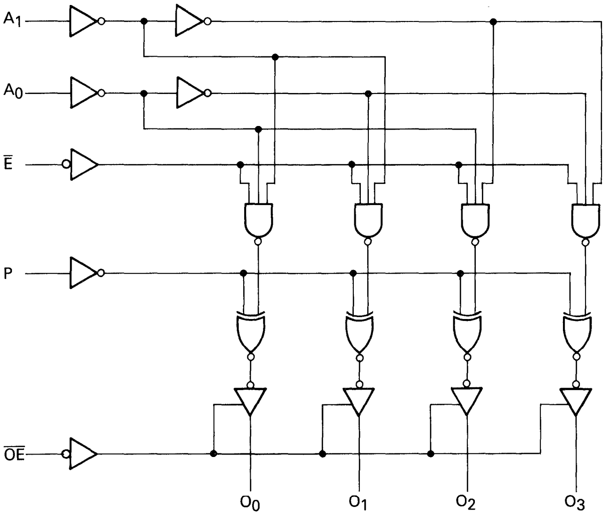
LOGIC SYMBOL



P A_0 A_1
E
DECODER a
OE
O_0 O_1 O_2 O_3
P A_0 A_1
E
DECODER b
OE
O_0 O_1 O_2 O_3

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM (1/2 SHOWN)

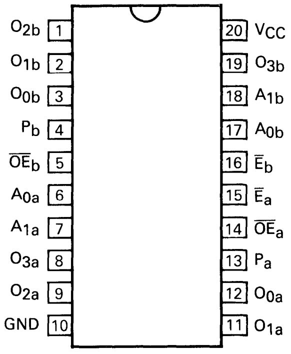


A_1
A_0
$\overline{E}$
P
$\overline{OE}$
O_0
O_1
O_2
O_3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

CONNECTION DIAGRAM
DIP (TOP VIEW)



O_{2b} 1
O_{1b} 2
O_{0b} 3
P_b 4
$\overline{OE}_b$ 5
A_{0a} 6
A_{1a} 7
O_{3a} 8
O_{2a} 9
GND 10
20 V_{CC}
19 O_{3b}
18 A_{1b}
17 A_{0b}
16 $\overline{E}_b$
15 $\overline{E}_a$
14 $\overline{OE}_a$
13 P_a
12 O_{0a}
11 O_{1a}

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7			V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CCZ}	Power Supply Current			40	60	mA	V_{CC} = MAX, A_0, A_1, $\overline{E}$ = GND $\overline{OE}$, P = HIGH	

AC CHARACTERISTICS

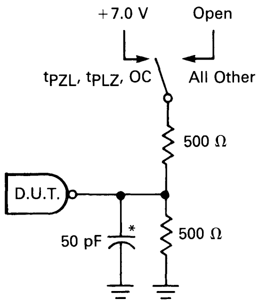
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	4.0 3.5	14.5 9.5	18.5 12			4.0 3.5	19.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to O_n	3.5 3.0	12 7.5	16 9.5			3.5 3.0	17 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay P to O_n	6.0 4.0	14.5 11	21.5 16.5			6.0 4.0	22.5 17.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	4.0 5.5	8.0 10	10.5 13			4.0 5.5	11.5 14	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0 2.5	4.5 6.5	6.0 8.5			2.0 2.5	7.0 9.5	

TRUTH TABLE (each half)

FUNCTION	INPUTS				OUTPUTS			
	$\overline{OE}$	$\overline{E}$	A_1	A_0	O_0	O_1	O_2	O_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	O_n = P			
Active HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

AC TEST CIRCUIT


+7.0 V
Open
t_{PZL}, t_{PLZ}, OC
All Other
500 Ω
D.U.T.
50 pF
*
500 Ω

*Includes jig and probe capacitance

FIGURE 1 — TEST LOAD

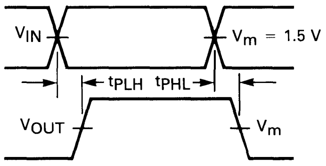

V_{IN}
V_m = 1.5 V
t_{PLH}
t_{PHL}
V_{OUT}
V_m

FIGURE 2 — WHETHER RESPONSE IS INVERTING OR NONINVERTING DEPENDS ON SPECIFIC TRUTH TABLE CONDITIONS

MOTOROLA

Advance Information

MC54F/74F568
MC54F/74F569

4-BIT
BIDIRECTIONAL
COUNTERS
(With 3-State Outputs)

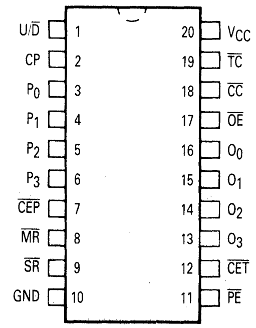
FAST™ SCHOTTKY TTL

4-BIT BIDIRECTIONAL COUNTERS (With 3-State Outputs)

DESCRIPTION — The MC54/74F568 and MC54/74F569 are fully synchronous, reversible counters with 3-state outputs. The F568 is a BCD decade counter; the F569 is a binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

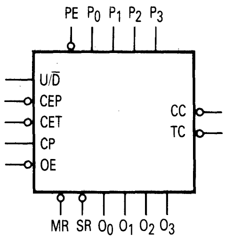
- **Synchronous Counting and Loading**
- **Lookahead Carry Capability for Easy Cascading**
- **Preset Capability for Programmable Operation**
- **3-State Outputs for Bus Organized Systems**

CONNECTION DIAGRAM


U/$\overline{D}$ 1
CP 2
P_0 3
P_1 4
P_2 5
P_3 6
$\overline{CEP}$ 7
$\overline{MR}$ 8
$\overline{SR}$ 9
GND 10
20 V_{CC}
19 $\overline{TC}$
18 $\overline{CC}$
17 $\overline{OE}$
16 O_0
15 O_1
14 O_2
13 O_3
12 $\overline{CET}$
11 $\overline{PE}$

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
DW Suffix — Case 751D-03 (SOIC)

LOGIC SYMBOL


PE P_0 P_1 P_2 P_3
U/$\overline{D}$
CEP
CET
CP
OE
CC
TC
MR SR O_0 O_1 O_2 O_3

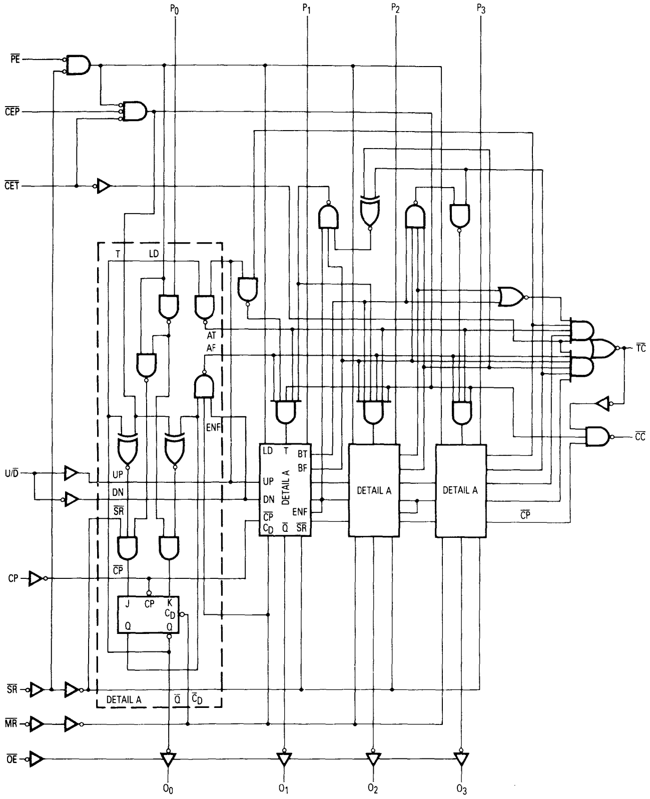
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

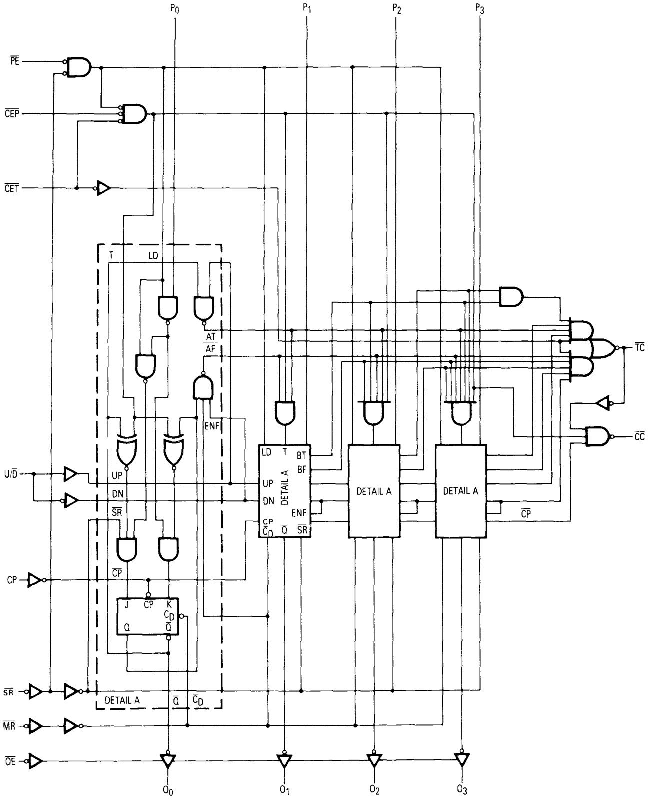
This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAMS

MC54F/74F568


P0
P1
P2
P3
PE
CEP
CET
T
LD
AT
AF
ENF
U/D
UP
DN
SR
CP
J
K
Q
CD
DETAIL A
BT
BF
TC
CC
O0
O1
O2
O3
MR
OE

MC54F/74F569


P0
P1
P2
P3
PE
CEP
CET
T
LD
AT
AF
ENF
U/D
UP
DN
SR
CP
J
K
Q
CD
DETAIL A
BT
BF
TC
CC
O0
O1
O2
O3
MR
OE

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset ($\overline{\text{MR}}$), Synchronous Reset ($\overline{\text{SR}}$), Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel ($\overline{\text{CEP}}$) and Count Enable Trickle $\overline{\text{CET}}$) — plus the Up/Down (U/$\overline{\text{D}}$) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{\text{MR}}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{\text{SR}}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{\text{PE}}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{\text{MR}}$, $\overline{\text{SR}}$ and $\overline{\text{PE}}$ HIGH, $\overline{\text{CEP}}$ and $\overline{\text{CET}}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ inhibits counting.

The F568 and F569 use edge-triggered flip-flops and changing the $\overline{\text{SR}}$, $\overline{\text{PE}}$, $\overline{\text{CEP}}$, $\overline{\text{CET}}$ or U/$\overline{\text{D}}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{\text{TC}}$) output is normally HIGH and goes LOW providing $\overline{\text{CET}}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the F568, 15 for the F569) in the Up mode. $\overline{\text{TC}}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{\text{D}}$ or $\overline{\text{CET}}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{\text{TC}}$ output and the $\overline{\text{CEP}}$ and $\overline{\text{CET}}$ inputs can provide either slow or fast carry propagation. Figure A shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{\text{TC}}$ delay of the first stage, plus the cumulative $\overline{\text{CET}}$ to $\overline{\text{TC}}$ delays of the intermediate stages, plus the $\overline{\text{CET}}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure B are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 (F568) or 16 (F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{\text{TC}}$ delay of the first stage plus the $\overline{\text{CEP}}$ to CP setup time of the last stage. The $\overline{\text{TC}}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{\text{CC}}$) output is provided. The $\overline{\text{CC}}$ output is normally HIGH. When $\overline{\text{CEP}}$, $\overline{\text{CET}}$, and $\overline{\text{TC}}$ are LOW, the $\overline{\text{CC}}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{\text{CC}}$ Truth Table. When the Output Enable ($\overline{\text{OE}}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{\text{OE}}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:

Count Enable = $\overline{\text{CEP}} \bullet \overline{\text{CET}} \bullet \text{PE}$

Up ('F568): $\overline{\text{TC}} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (\text{Up}) \bullet \overline{\text{CET}}$

('F569): $\overline{\text{TC}} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (\text{Up}) \bullet \overline{\text{CET}}$

Down (Both): $\overline{\text{TC}} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (\text{Down}) \bullet \overline{\text{CET}}$

$\overline{\text{CC}}$ TRUTH TABLE

Inputs						Output
$\overline{\text{SR}}$	$\overline{\text{PE}}$	$\overline{\text{CEP}}$	$\overline{\text{CET}}$	$\overline{\text{TC}}$*	CP	$\overline{\text{CC}}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	‾⊔‾	‾⊔‾

* = $\overline{\text{TC}}$ is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECT TABLE

Inputs						Operating Mode
$\overline{\text{MR}}$	$\overline{\text{SR}}$	$\overline{\text{PE}}$	$\overline{\text{CEP}}$	$\overline{\text{CET}}$	U/$\overline{\text{D}}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FIGURE A — MULTISTAGE COUNTER WITH RIPPLE CARRY

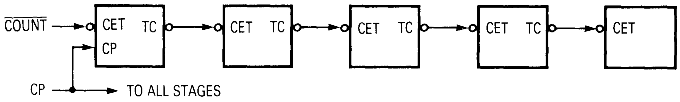
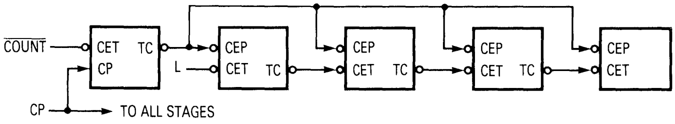

$\overline{\text{COUNT}}$
CET TC
CP
CET TC
CET TC
CET TC
CET
CP
TO ALL STAGES

FIGURE B — MULTISTAGE COUNTER WITH LOOKAHEAD CARRY


$\overline{\text{COUNT}}$
CET TC
CP
L
CEP
CET TC
CEP
CET TC
CEP
CET TC
CEP
CET
CP
TO ALL STAGES

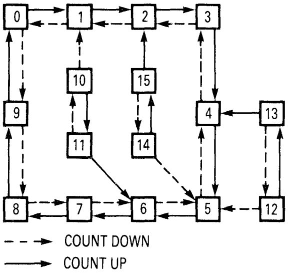
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.3		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.3	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{PE}$, $\overline{CET}$ Others				 −1.2 −0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current (ALL Outputs OFF)				67	mA	V_{CC} = MAX	

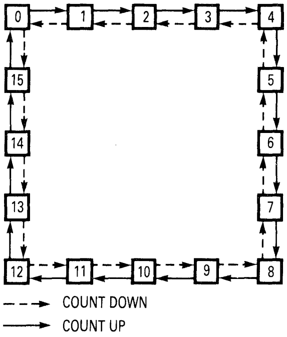
NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

STATE DIAGRAMS

MC54F/74F568



MC54F/74F569

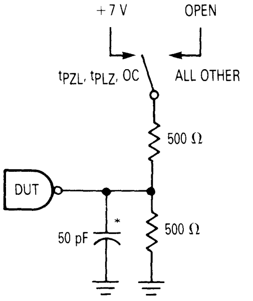


AC CHARACTERISTICS

SYMBOL	PARAMETER	54F/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	100		60		85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.0 4.0	8.5 11.5	3.0 4.0	10.5 14	3.0 4.0	9.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.5 4.0	15.5 11	5.5 4.0	18.5 13.5	5.5 4.0	17.5 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	6.0 8.0	2.5 2.5	8.0 10	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('F568)	3.5 4.0	11 16	3.5 4.0	13.5 19	3.5 4.0	12.5 18	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('F569)	3.5 4.0	11 10.5	3.5 4.0	13.5 13	3.5 4.0	12.5 12	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{CC}$	2.5 2.0	7.0 6.0	2.5 2.0	9.0 8.0	2.5 2.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$	2.5 4.0	6.5 11	2.5 4.0	8.5 13.5	2.5 4.0	7.5 12.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	5.0	13	5.0	15.5	5.0	14.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.5 3.0	7.0 8.0	2.5 3.0	9.0 10	2.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	1.5 2.0	6.5 6.0	1.5 2.0	8.5 8.0	1.5 2.0	7.5 7.0	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54F/74F		54F		74F		UNITS
		T_A = +25°C V_{CC} = +5.0 V		T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10%		T_A = 0°C to +70°C V_{CC} = 5.0 V ± 10%		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$	Setup Time, HIGH or LOW P_n to CP	4.0		5.5		4.5		ns
$t_s(L)$		4.0		5.5		4.5		
$t_h(H)$	Hold Time, HIGH or LOW P_n to CP	3.0		3.5		3.5		
$t_h(L)$		3.0		3.5		3.5		
$t_s(H)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	5.0		7.0		6.0		ns
$t_s(L)$		5.0		7.0		6.0		
$t_h(H)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0		0		0		
$t_h(L)$		0		0		0		
$t_s(H)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0		10		9.0		ns
$t_s(L)$		8.0		10		9.0		
$t_h(H)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0		0		0		
$t_h(L)$		0		0		0		
$t_s(H)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F568)	11		13.5		12.5		ns
$t_s(L)$		16.5		18.5		17.5		
$t_s(H)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F569)	11		13.5		12.5		ns
$t_s(L)$		7.0		9.0		8.0		
$t_h(H)$	Hold time, HIGH or LOW U/$\overline{D}$ to CP	0		0		0		ns
$t_h(L)$		0		0		0		
$t_s(H)$	Setup Time, HIGH or LOW $\overline{SR}$ to CP	10		12		11		ns
$t_s(L)$		8.5		10.5		9.5		
$t_h(H)$	Hold Time, HIGH or LOW $\overline{SR}$ to CP	0		0		0		
$t_h(L)$		0		0		0		
$t_w(H)$	CP Pulse Width HIGH or LOW	4.0		6.0		4.5		ns
$t_w(L)$		6.0		8.0		6.5		
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	4.5		6.0		5.0		ns
t_{rec}	$\overline{MR}$ Recovery Time	6.0		8.0		7.0		ns



*INCLUDES JIG AND PROBE CAPACITANCE

FIGURE 1 — TEST LOAD

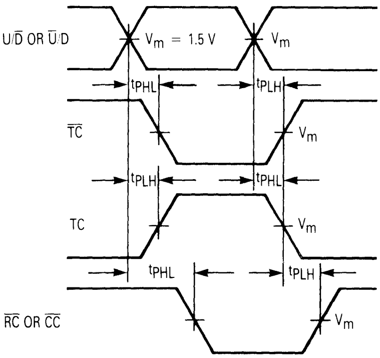


FIGURE 2 — PROPAGATION DELAYS FROM UP/DOWN CONTROL

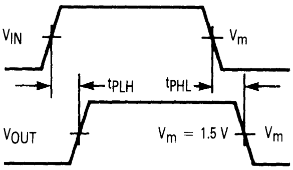

VIN
Vm
tPLH
tPHL
VOUT
Vm = 1.5 V
Vm

FIGURE 3 — WAVEFORM FOR NON-INVERTING FUNCTIONS

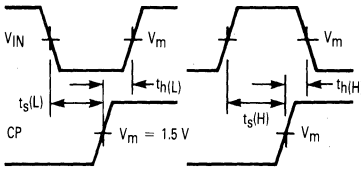

VIN
Vm
Vm
Vm
th(L)
th(H)
ts(L)
ts(H)
CP
Vm = 1.5 V
Vm

FIGURE 4 — SETUP AND HOLD TIMES, RISING-EDGE CLOCK

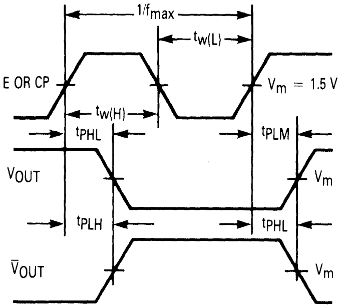

1/fmax
tw(L)
E OR CP
Vm = 1.5 V
tw(H)
tPHL
tPLM
VOUT
Vm
tPLH
tPHL
V̄OUT
Vm

FIGURE 5 — PROPAGATION DELAYS FROM RISING-EDGE CLOCK OR ENABLE

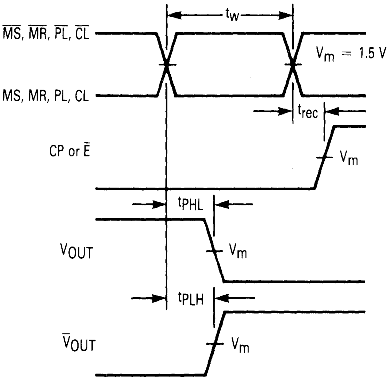

tw
M̄S̄, M̄R̄, P̄L̄, C̄L̄
Vm = 1.5 V
MS, MR, PL, CL
trec
CP or Ē
Vm
tPHL
VOUT
Vm
tPLH
V̄OUT
Vm

FIGURE 6 — ASYNCHRONOUS SET, RESET, PARALLEL LOAD OR CLEAR, ACTIVE RISING-EDGE CLOCK OR ACTIVE-LOW ENABLE

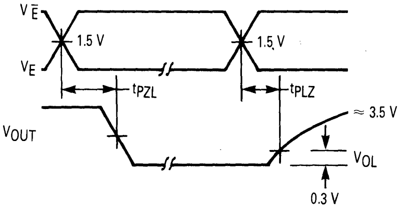

VĒ
1.5 V
1.5 V
VE
tPZL
tPLZ
≈ 3.5 V
VOUT
VOL
0.3 V

FIGURE 7 — 3-STATE OUTPUT LOW ENABLE AND DISABLE TIMES

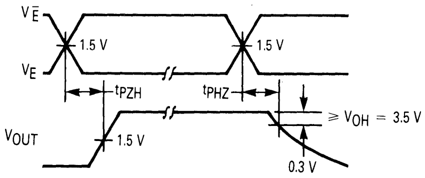

VĒ
1.5 V
1.5 V
VE
tPZH
tPHZ
≥ VOH = 3.5 V
VOUT
1.5 V
0.3 V

FIGURE 8 — 3-STATE OUTPUT HIGH ENABLE AND DISABLE TIMES

MOTOROLA

MC74F803

Advance Information

CLOCK DRIVER
QUAD D-TYPE FLIP-FLOP
With Matched Propagation Delays

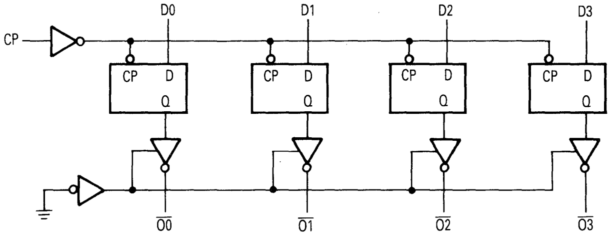
DESCRIPTION — The MC74F803 is a high-speed, low-power, quad D-type flip-flop featuring separate D-type inputs, and inverting outputs with closely matched propagation delays. With a buffered clock (CP) input that is common to all flip-flops, the 'F803 is useful in high-frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 1.0 to 1.5 nanoseconds.

- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Matched Outputs for Synchronous Clock Driver Applications**
- **Outputs Guaranteed for Simultaneous Switching**

GUARANTEED OPERATION RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High	—	—	−20	mA
I_{OL}	Output Current — Low	—	—	24	mA

LOGIC DIAGRAM



CP
D0
D1
D2
D3
CP D Q
$\overline{O0}$
$\overline{O1}$
$\overline{O2}$
$\overline{O3}$

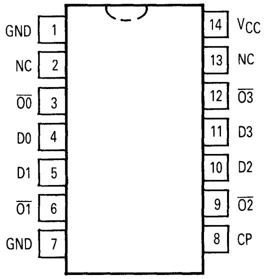
NOTE: Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CLOCK DRIVER
QUAD D-TYPE FLIP-FLOP
With Matched Propagation Delays

FAST™ SCHOTTKY TTL

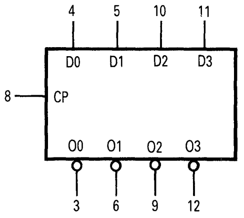
CONNECTION DIAGRAM



GND 1
NC 2
$\overline{O0}$ 3
D0 4
D1 5
$\overline{O1}$ 6
GND 7
14 V_{CC}
13 NC
12 $\overline{O3}$
11 D3
10 D2
9 $\overline{O2}$
8 CP

N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

LOGIC SYMBOL



4
5
10
11
D0 D1 D2 D3
8
CP
O0 O1 O2 O3
3
6
9
12

V_{CC} = PIN 14
GND = PINS 1 AND 7
NC = PINS 2 AND 13

FUNCTIONAL DESCRIPTION

The 'F803 consists of four positive edge-triggered flip-flops with individual D-type inputs and inverting outputs. The buffered clock is common to all flip-flops and the following specifications allow for outputs switching simultaneously. The four flip-flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz, and the LOW-to-HIGH and HIGH-to-LOW propagation delays of the $\overline{O}_1$ output vary by, at most, 1 nanosecond. Therefore, the device is ideal for use as a divide-by-two driver for high-frequency clock signals that require symmetrical duty cycles. The difference between the LOW-to-HIGH and HIGH-to-LOW propagation delays for the $\overline{O}_0$, $\overline{O}_2$, and $\overline{O}_3$ outputs vary by at most 1.5 nanoseconds. These outputs are very useful as clock drivers for circuits with less stringent requirements. In addition, the output-to-output skew is a maximum of 1.5 nanoseconds. Finally, the I_{OH} specification at 2.5 volts is guaranteed to be at least −20 milliamps. If their inputs are identical, multiple outputs can be tied together and the I_{OH} is commensurately increased.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS*	
		MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage	—	—	−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	2.5	—	—	V	I_{OH} = −20 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	—	0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current	—	—	20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
		—	—	100		V_{IN} = 7.0 V	V_{CC} = MAX
I_{IL}	Input LOW Current	—	—	−0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)	−60	—	−150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current	—	—	70	mA	V_{CC} = MAX	

*Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the '74F803 can be tied together and the I_{OH} doubles.

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%, see Note 1)

SYMBOL	PARAMETER	C_L = 50 pF		C_L = 100 pF		UNITS
		MIN	MAX	MIN	MAX	
f_{max}	Maximum Clock Frequency	70	—	50	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{On}$	3.0	7.5	3.0	10	ns
t_{PV}	Propagation Delay CP to $\overline{On}$ Variation (see Note 3)	—	3.0	—	4.0	ns
t_{ps} $\overline{O}_1$	Propagation Delay Skew $\lvert t_{PLH}$ Actual — t_{PHL} Actual$\rvert$ for $\overline{O}_1$ Only	—	1.0	—	2.0	ns
t_{ps} $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$	Propagation Delay Skew $\lvert t_{PLH}$ Actual — t_{PHL} Actual$\rvert$ for $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$	—	1.5	—	2.0	ns
t_{os}	Output to Output Skew (see Note 2) $\lvert t_p\ \overline{On} — t_p\ \overline{Om}\rvert$	—	1.5	—	2.5	ns
t_{rise}, t_{fall} $\overline{O}_1$	Rise/Fall Time for $\overline{O}_1$ (0.8 to 2.0 V)	—	3.0	—	4.0	ns
t_{rise}, t_{fall} $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$	Rise/Fall Time for $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$ (0.8 to 2.0 V)	—	3.5	—	4.5	ns

NOTES:

1. The test conditions used are all four outputs switching simultaneously. The AC characteristics described above (except for $\overline{O}_1$) are also guaranteed when two outputs are tied together.
2. Where t_p $\overline{On}$ and t_p $\overline{Om}$ are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
3. For a given set of conditions (i.e., capacitive load, temperature, V_{CC}, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

AC OPERATING REQUIREMENTS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%)

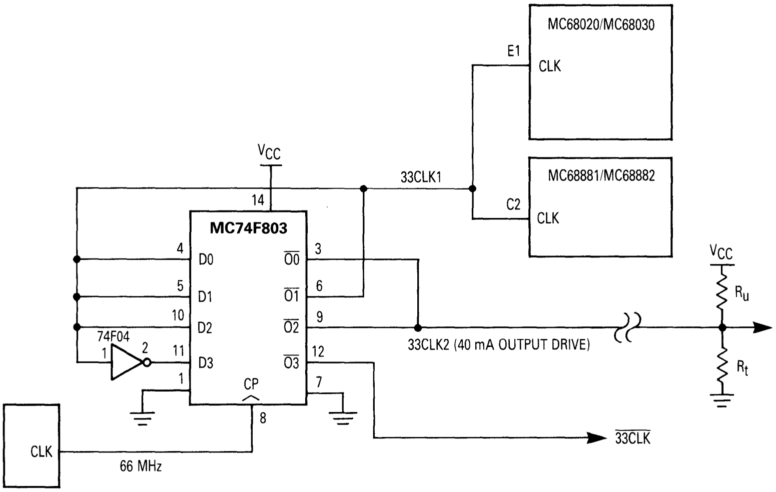
SYMBOL	PARAMETER	C_L = 50 pF		C_L = 100 pF		UNITS
		MIN	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to CP	3.0 3.0	— —	4.0 4.0	— —	ns
t_f	$t_p + t_s$ (see Note)	—	9.0	—	12	ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0	— —	2.0 2.0	— —	ns
t_w(H) t_w(L)	CP Pulse Width HIGH or LOW	7.0 6.0	— —	8.0 8.0	— —	ns

NOTE:
The combination of the setup time (t_s) requirement and maximum propagation delay (t_p) are guaranteed to be within this limit for all conditions.

APPLICATION NOTE

The closely matched outputs of the MC74F803 provide an ideal interface for the clock input of Motorola's high-frequency microprocessors.

74F803 INTERFACE AS CLOCK TO MC68020 SYSTEM


MC68020/MC68030
E1
CLK
MC68881/MC68882
C2
CLK
V_{CC}
33CLK1
14
MC74F803
4
D0
5
D1
10
D2
74F04
1
2
11
D3
1
CP
8
$\overline{O0}$
3
$\overline{O1}$
6
$\overline{O2}$
9
$\overline{O3}$
12
7
33CLK2 (40 mA OUTPUT DRIVE)
V_{CC}
R_u
R_t
$\overline{33CLK}$
CLK
66 MHz

MOTOROLA

MC54F/74F827
MC54F/74F828

Advance Information

10-BIT BUFFERS/LINE DRIVERS
(With 3-State Outputs)

DESCRIPTION — The MC54/74F827 and MC54/74F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

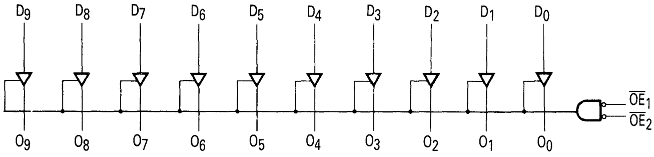
The F827 and F828 are functionally and pin compatible to AMD's 29827 and 29828. The F828 is an inverting version of the F827.

- **3-State Outputs Drive Memory Address, Bus and Clock Lines**
- **Outputs Sink 64 mA**
- **15 mA Source Current**

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54			−12	mA
		74			−15	
I_{OL}	Output Current — Low	54			48	mA
		74			64	

LOGIC DIAGRAM



D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
OE1
OE2
O9
O8
O7
O6
O5
O4
O3
O2
O1
O0

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTION TABLE

Inputs		Outputs		Function
		O_n		
$\overline{OE}$	D_n	F827	F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

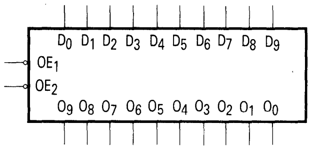
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

10-BIT BUFFERS/LINE DRIVERS
(With 3-State Outputs)

FAST™ SCHOTTKY TTL

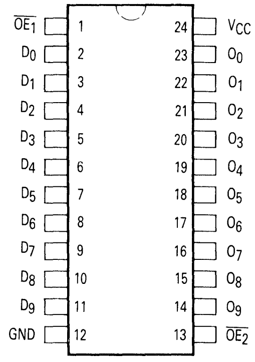
LOGIC SYMBOL



D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
OE1
OE2
O9 O8 O7 O6 O5 O4 O3 O2 O1 O0

CONNECTION DIAGRAMS

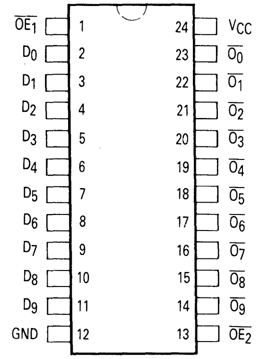
F827



OE1 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D9 11
GND 12
24 VCC
23 O0
22 O1
21 O2
20 O3
19 O4
18 O5
17 O6
16 O7
15 O8
14 O9
13 OE2

TOP VIEW

F828



OE1 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D8 10
D9 11
GND 12
24 VCC
23 O0
22 O1
21 O2
20 O3
19 O4
18 O5
17 O6
16 O7
15 O8
14 O9
13 OE2

TOP VIEW

J SUFFIX — CASE 758-01 (CERAMIC DIP)
N SUFFIX — CASE 724-02 (PLASTIC DIP)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	$I_{IN} = -18$ mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54	2.0			V	$I_{OH} = -12$ mA	V_{CC} = MIN
		74	2.0			V	$I_{OH} = -15$ mA	
		54, 74	2.4			V	$I_{OH} = -3.0$ mA	
		74	2.7			V	$I_{OH} = -3.0$ mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage	54			0.55	V	I_{OL} = 48 mA	V_{CC} = MIN
		74			0.55	V	I_{OL} = 64 mA	
I_{OZH}	Output Off Current HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current LOW				−50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = 0 V
					100	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−20	μA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		−100		−225	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current HIGH	F827			70	mA	Outputs HIGH	V_{CC} = MAX
		F828			45	mA		
I_{CCL}	Power Supply Current LOW	F827			100	mA	Outputs LOW	V_{CC} = MAX
		F828			85	mA		
I_{CCZ}	Power Supply Current OFF	F827			90	mA	Outputs OFF	V_{CC} = MAX
		F828			70	mA		

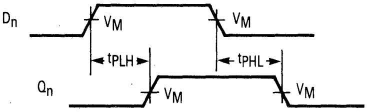
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

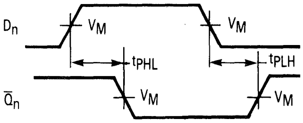
SYMBOL	PARAMETER		54F/74F		54F		74F		UNITS
			$T_A = +25°C$ $V_{CC} = +5.0$ V C_L = 50 pF		$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0$ V ± 10% C_L = 50 pF		T_A = 0°C to 70°C $V_{CC} = 5.0$ V ± 10% C_L = 50 pF		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delay, Data to Output	F827	2.0	8.5	2.0	10	2.0	9.0	ns
t_{PHL}			2.0	8.5	2.0	10	2.0	9.0	ns
t_{PZH}	Output Enable Time		3.5	9.5	3.5	11	3.5	10	ns
t_{PZL}			4.0	9.0	4.0	10.5	4.0	9.5	ns
t_{PHZ}	Output Disable Time		2.0	8.0	2.0	9.5	2.0	8.5	ns
t_{PLZ}			1.5	8.0	1.5	9.5	1.5	8.5	ns
t_{PLH}	Propagation Delay, Data to Output	F828	2.0	9.0	2.0	11	2.0	10	ns
t_{PHL}			1.0	8.0	1.0	10	1.0	9.0	ns
t_{PZH}	Output Enable Time		3.5	9.5	3.5	11	3.5	10	ns
t_{PZL}			4.0	9.0	4.0	10.5	4.0	9.5	ns
t_{PHZ}	Output Disable Time		2.0	8.5	2.0	10	2.0	9.0	ns
t_{PLZ}			1.5	7.0	1.5	9.0	1.5	8.0	ns

AC WAVEFORMS

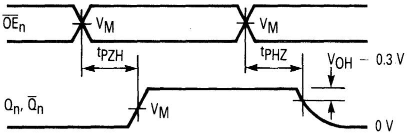
$V_M = 1.5\ V$


Dn
VM
VM
tPLH
tPHL
Qn
VM
VM

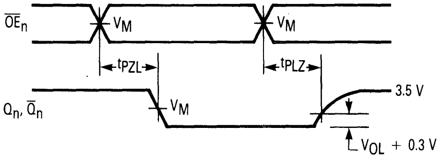
WAVEFORM 1 — PROPAGATION DELAY FOR NON-INVERTING OUTPUTS


Dn
VM
VM
tPHL
tPLH
Q̄n
VM
VM

WAVEFORM 2 — PROPAGATION DELAY FOR INVERTING OUTPUTS

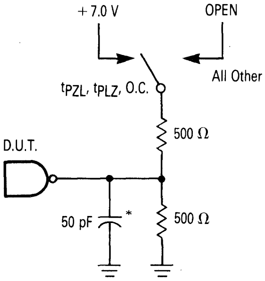

ŌEn
VM
VM
tPZH
tPHZ
VOH − 0.3 V
Qn, Q̄n
VM
0 V

WAVEFORM 3 — 3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL


ŌEn
VM
VM
tPZL
tPLZ
3.5 V
Qn, Q̄n
VM
VOL + 0.3 V

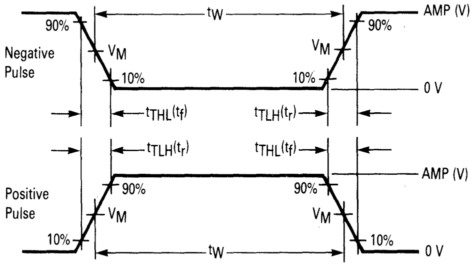
WAVEFORM 4. 3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

AC TEST CONDITIONS


+7.0 V
OPEN
All Other
tPZL, tPLZ, O.C.
500 Ω
D.U.T.
50 pF
*
500 Ω

*Includes jig and probe capacitance

FIGURE 1 — TEST LOAD


90%
tW
AMP (V)
90%
Negative Pulse
VM
VM
10%
10%
0 V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
Positive Pulse
90%
90%
VM
VM
10%
10%
tW
0 V

$V_M = 1.5\ V$

INPUT PULSE DEFINITION

INPUT PULSE REQUIREMENTS				
Amplitude	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

MOTOROLA

MC74F2960/
Am2960
MC74F2960A

ERROR DETECTION AND CORRECTION CIRCUIT

ADVANCED LOW POWER SCHOTTKY

Advance Information

ERROR DETECTION AND CORRECTION CIRCUIT

The MC74F2960 will be dual marked with the AMD part number Am2960 to indicate plug-in compatibility. However, the device will be referred to as the MC74F2960 in the remainder of this specification. The MC74F2960A is a high speed version of MC74F2960 and is a plug-in replacement for MC74F2960 where higher performance is required.

DESCRIPTION — The MC74F2960 and MC74F2960A Error Detection and Correction Units (EDAC) contain the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the MC74F2960 and MC74F2960A will correct any single bit error* and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The MC74F2960 and MC74F2960A are expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

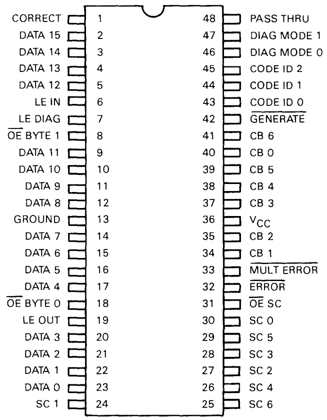
The MC74F2960 and MC74F2960A also feature two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product will be supplied in a 48-lead DIP package.

*Double bit errors can also be corrected if at least one of the two errors is a hard error. This requires extra processor cycles.

- **PIN AND FUNCTIONALLY COMPATIBLE WITH THE Am2960**
- **BOOSTS MEMORY RELIABILITY**
- **EXPANDABLE TO 64-BIT DATA WORDS**
- **BUILT-IN DIAGNOSTICS PERMITS SOFTWARE SYSTEM CHECK**
- **SEPARATE BYTE CONTROLS FACILITATE BYTE OPERATIONS**
- **COMPATIBLE WITH MC68000 AND OTHER PROCESSORS**

16-Bit Timing (Worst Case)	74F2960	74F2960A	Units
Check Bit Generation	32	20	ns
Single Error Detection	32	19	ns
Single Error Correction	65	42	ns

CONNECTION DIAGRAM
Top View



CORRECT 1
DATA 15 2
DATA 14 3
DATA 13 4
DATA 12 5
LE IN 6
LE DIAG 7
$\overline{\text{OE}}$ BYTE 1 8
DATA 11 9
DATA 10 10
DATA 9 11
DATA 8 12
GROUND 13
DATA 7 14
DATA 6 15
DATA 5 16
DATA 4 17
$\overline{\text{OE}}$ BYTE 0 18
LE OUT 19
DATA 3 20
DATA 2 21
DATA 1 22
DATA 0 23
SC 1 24
48 PASS THRU
47 DIAG MODE 1
46 DIAG MODE 0
45 CODE ID 2
44 CODE ID 1
43 CODE ID 0
42 $\overline{\text{GENERATE}}$
41 CB 6
40 CB 0
39 CB 5
38 CB 4
37 CB 3
36 V_{CC}
35 CB 2
34 CB 1
33 $\overline{\text{MULT ERROR}}$
32 $\overline{\text{ERROR}}$
31 $\overline{\text{OE}}$ SC
30 SC 0
29 SC 5
28 SC 3
27 SC 2
26 SC 4
25 SC 6

J Suffix — Case 740-03 (Ceramic)
N Suffix — Case 767-02 (Plastic)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM

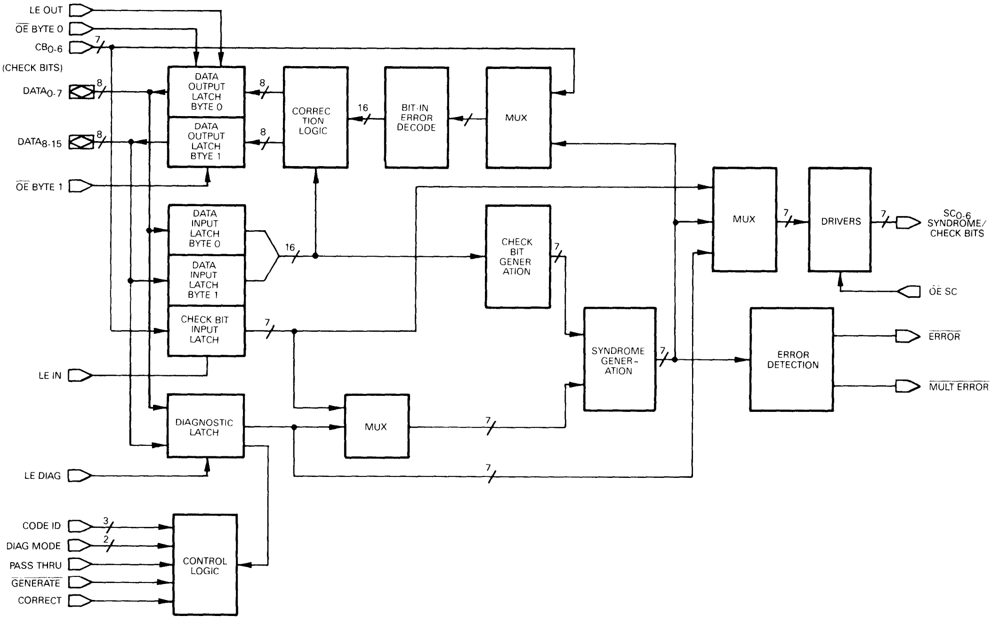

LE OUT
OE BYTE 0
CB0-6
(CHECK BITS)
DATA0-7
DATA8-15
OE BYTE 1
LE IN
LE DIAG
CODE ID
DIAG MODE
PASS THRU
GENERATE
CORRECT
DATA OUTPUT LATCH BYTE 0
DATA OUTPUT LATCH BTYE 1
CORRECTION LOGIC
BIT-IN ERROR DECODE
MUX
DATA INPUT LATCH BYTE 0
DATA INPUT LATCH BYTE 1
CHECK BIT INPUT LATCH
CHECK BIT GENERATION
SYNDROME GENERATION
DIAGNOSTIC LATCH
MUX
MUX
DRIVERS
ERROR DETECTION
CONTROL LOGIC
SC0-6 SYNDROME/ CHECK BITS
OE SC
ERROR
MULT ERROR
7
8
8
16
8
16
7
7
7
7
7
7
7
3
2

TABLE 1. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (Except $DATA_{0-15}$)	V_{in}	−0.5 to +7.0	V
Input Voltage ($DATA_{0-15}$)	V_{in}	−0.5 to +5.5	V
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

TABLE 2. GUARANTEED OPERATING RANGES (θ_{JC} = 6°C/Watt)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			−0.8	mA
I_{OL}	Output Current — Low			8.0	mA

Operating ranges define those limits over which the functionality of the device is guaranteed.

TABLE 3. DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage (1)		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage (1)				0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage				-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage		2.7			V	V_{CC} = MIN, I_{OH} = -0.8 mA
V_{OL}	Output LOW Voltage				0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{OZH}	Output Off Current-HIGH	$DATA_{0-15}$			70	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
		SC_{0-6}			50	μA	
I_{OZL}	Output Off Current-LOW	$DATA_{0-15}$			-410	μA	V_{CC} = MAX, V_{OUT} = 0.5 V
		SC_{0-6}			-50	μA	
I_{IH}	Input High Current	$DATA_{0-15}$			70	μA	V_{CC} = MAX, V_{IN} = 2.7 V
		OTHERS			50	μA	
		ALL			1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input Low Current	$DATA_{0-15}$			-410	μA	V_{CC} = MAX, V_{IN} = 0.5 V
		OTHERS			-360	μA	
I_{OS}	Short Circuit Current (2)		-25		-85	mA	V_{CC} = MAX, V_O = 0 V
I_{CC}	Power Supply Current				300	mA	V_{CC} = MAX

(1) These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
(2) Not more than one output should be shorted at a time.

FIGURE 2 — AC TEST FIXTURE

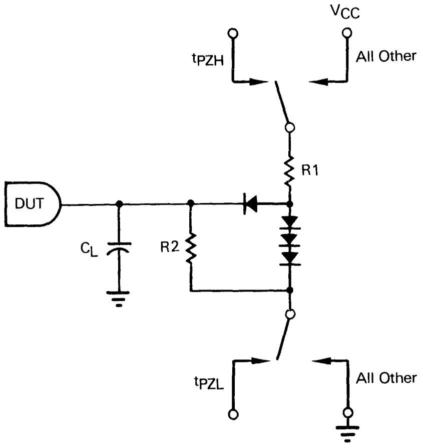


TABLE 4. TEST OUTPUT LOADS

Pin	Pin Label	R_1	R_2
-	D_0-D_{15}	430 Ω	1 kΩ
24-30	SC_0-SC_6	430 Ω	1 kΩ
32	$\overline{ERROR}$	470 Ω	3 kΩ
33	$\overline{MULT\ ERROR}$	470 Ω	3 kΩ

TABLE 5. AC CHARACTERISTICS (MAXIMUM LIMITS)

SYMBOL	PARAMETER		V_{CC} = 5.0 V ± 5%; T_A = 0 to +70°C; C_L = 50 pF; UNITS = ns***							
	From Input / To Output		SC_{0-6}		$DATA_{0-15}$		$\overline{\text{ERROR}}$		$\overline{\text{MULT ERROR}}$	
t_{PLH}, t_{PHL}	Propagation Delay		MC74F 2960	MC74F 2960A	MC74F 2960	MC74F 2960A	MC74F 2960	MC74F 2960A	MC74F 2960	MC74F 2960A
	$DATA_{0-15}$		32	20	65*	42*	32	19	50	26
	CB_{0-6} (CODE ID_{2-0} 000, 011)		28	18	56	34	29	16	47	24
	CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)		28	19	45	30	29	18	34	22
	$\overline{\text{GENERATE}}$		35	19	63	35	36	18	55	22
	CORRECT (Not Internal Control Mode)		—	—	45	32	—	—	—	—
	DIAG $MODE_{0-1}$ (Not Internal Control Mode)		50	35	78	55	59	42	75	53
	PASS THRU (Not Internal Control Mode)		36	18	44	30	29	18	46	22
	CODE ID_{0-2}		61	40	90	52	60	40	80	44
	LE IN (From latched to transparent)		39	24	72*	40*	39	22	59	26
	LE OUT (From latched to transparent)		—	—	31	22	—	—	—	—
	LE DIAG (From latched to transparent; Not Internal Control Mode)		45	32	78	55	45	32	65	46
	Internal Control Mode: LE DIAG (From latched to transparent)		67	47	96	67	66	46	86	60
	Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)		67	47	96	67	66	46	86	60
t_{PZH}, t_{PZL}**	Output Enable Time	$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1	—	—	30	30	—	—	—	—
		$\overline{\text{OE}}$ SC	30	30	—	—	—	—	—	—
t_{PHZ}, t_{PLZ}**	Output Disable Time	$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1	—	—	30	30	—	—	—	—
		$\overline{\text{OE}}$ SC	30	30	—	—	—	—	—	—

*Data In or LE In to Correct Data Out measurement requires timing as shown in Figure 3.

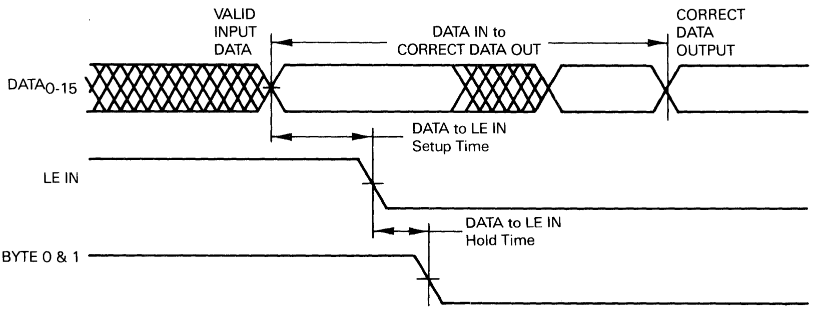
**C_L for t_{PZH}, t_{PZL}, t_{PHZ} and t_{PLZ} = 5.0 pF

***Inputs switching between 0V and 3V at 1V/ns, measurements made at 1.5V. All outputs have maximum DC load.

TABLE 6. AC OPERATING REQUIREMENTS (MINIMUM LIMITS)

SYMBOL	PARAMETER		T_A = 0 to +70°C V_{CC} = 5.0 V ±10%		UNITS
			MC74F2960	MC74F2960A	
t_{su} t_h	Setup Time Hold Time	DATA$_{0-15}$ to LE IN	6 7	4 6	ns
t_{su} t_h	Setup Time Hold Time	CB$_{0-6}$ to LE IN	5 6	3 5	ns
t_{su} t_h	Setup Time Hold Time	DATA$_{0-15}$ to LE OUT	44 5	18 3	ns
t_{su} t_h	Setup Time Hold Time	CB$_{0-6}$ to LE OUT (Code ID 000, 011)	35 0	17 0	ns
t_{su} t_h	Setup Time Hold Time	CB$_{0-6}$ to LE OUT (Code ID 010, 100, 101, 110, 111)	27 0	27 0	ns
t_{su} t_h	Setup Time Hold Time	$\overline{\text{GENERATE}}$ to LE OUT	42 0	27 0	ns
t_{su} t_h	Setup Time Hold Time	CORRECT to LE OUT	26 1	19 0	ns
t_{su} t_h	Setup Time Hold Time	DIAG MODE$_{0-1}$, to LE OUT	69 0	69 0	ns
t_{su} t_h	Setup Time Hold Time	PASS THRU to LE OUT	26 0	20 0	ns
t_{su} t_h	Setup Time Hold Time	CODE ID$_{0-2}$, to LE OUT	81 0	24 0	ns
t_{su} t_h	Setup Time Hold Time	LE IN to LE OUT	51 5	30 5	ns
t_{su} t_h	Setup Time Hold Time	DATA$_{0-15}$ to LE DIAG	6 8	6 8	ns
t_w	Minimum Pulse Width, High or Low	LE IN, LE OUT, or LE DIAG	15	15	ns

FIGURE 3 — TIMING REQUIRED for DATA IN (or LE IN) to CORRECTED DATA OUT


VALID INPUT DATA
DATA IN to CORRECT DATA OUT
CORRECT DATA OUTPUT
DATA$_{0-15}$
DATA to LE IN Setup Time
LE IN
DATA to LE IN Hold Time
$\overline{\text{OE}}$ BYTE 0 & 1

PIN DEFINITIONS

DATA$_{0-15}$

16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch, DATA$_0$ is the least significant bit; DATA$_{15}$ the most significant.

CB$_{0-6}$

Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. They are also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN

Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

$\overline{\text{GENERATE}}$

Generate Check Bits input. When this input is LOW the EDAC is in the Check Bit Generate Mode. When HIGH the EDAC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDAC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected — corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC$_{0-6}$

Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDAC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

$\overline{\text{OE}}$ SC

Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC$_{0-6}$ are enabled. When HIGH, the SC outputs are in the high impedance state.

$\overline{\text{ERROR}}$

Error Detected output. When the EDAC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

$\overline{\text{MULT ERROR}}$

Multiple Errors Detected output. When the EDAC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)

CORRECT

Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDAC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

LE OUT

Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDAC is in Generate Mode.

$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1

Output Enable — Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU

Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC$_{0-6}$) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

DIAG MODE$_{0-1}$

Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDAC.

CODE ID$_{0-2}$

Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDAC is processing. The three allowable data word sizes are 16, 32 and 64-bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID$_2$, ID$_1$, ID$_0$) is also used to instruct the EDAC that the signals CODE ID$_{0-2}$, DIAG MODE$_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG

Latch Enable — Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID$_{0-2}$, DIAG MODE$_{0-1}$, CORRECT and PASS THRU.

FUNCTIONAL DESCRIPTION

The MC74F2960 and MC74F2960A contain the necessary logic to generate check bits on a 16-bit data field according to a modified Hamming code. This code allows the EDAC to 1) be cascaded, 2) detect all double bit errors, 3) detect RAM failure (all 1 or 0 data).

The EDAC may be configured to work on data words from 8- to 64-bits in length. When cascaded for word lengths in excess of 16 bits, each EDAC must know which bits it is processing. This is done with Code ID inputs as shown in Table 7. The Internal Control Mode is described later.

MODE SELECTION

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG MODE$_{0\text{-}1}$ and CODE ID$_{0\text{-}2}$. Table 8 lists the MC74F2960 and MC74F2960A modes of operation. The data flow for each of these modes is shown in Figures 3 through 6.

PASS THRU MODE

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on the SC outputs. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

GENERATE MODE

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the SC outputs.

DETECT MODE

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULT ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on the SC outputs are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

CORRECT MODE

In this mode, the EDAC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified.

If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in GENERATE MODE to produce a correct check bit sequence for the data in the Data Input Latch.

DIAGNOSTIC GENERATE
DIAGNOSTIC DETECT
DIAGNOSTIC CORRECT

These are special diagnostic modes where check bits loaded into the Diagnostic Latch are substituted for either normal check bit inputs or outputs.

INITIALIZE

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in the initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDAC may be placed in initialize mode and its' outputs written into all memory locations by the processor.

INTERNAL CONTROL MODE

When in the internal control mode, the EDAC takes the CODE ID$_{0\text{-}2}$, DIAG MODE$_{0\text{-}1}$, CORRECT and PASS THRU control signals from the Internal Diagnostic Latch rather than from the external input lines or Memory Controller.

TABLE 7. HAMMING CODE AND SLICE IDENTIFICATION

CODE ID$_2$	CODE ID$_1$	CODE ID$_0$	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE 8. F2960/F2960A MODES OF OPERATION

	CONTROL INPUTS*				
OPERATING MODE*	**DIAG MODE 1**	**DIAG MODE 0**	**PASS THRU**	**$\overline{\text{GENERATE}}$**	**CORRECT**
PASS THRU	X	X	1	X	X
GENERATE	X	0	0	0	X
DETECT	0	X	0	1	0
CORRECT	0	X	0	1	1
DIAGNOSTIC GENERATE	0	1	0	0	X
DIAGNOSTIC DETECT	1	0	0	1	0
DIAGNOSTIC CORRECT	1	0	0	1	1
INITIALIZE	1	1	0	X	X

*The internal control mode overrides control inputs (See Text).

FIGURE 4 — CHECK BIT GENERATION

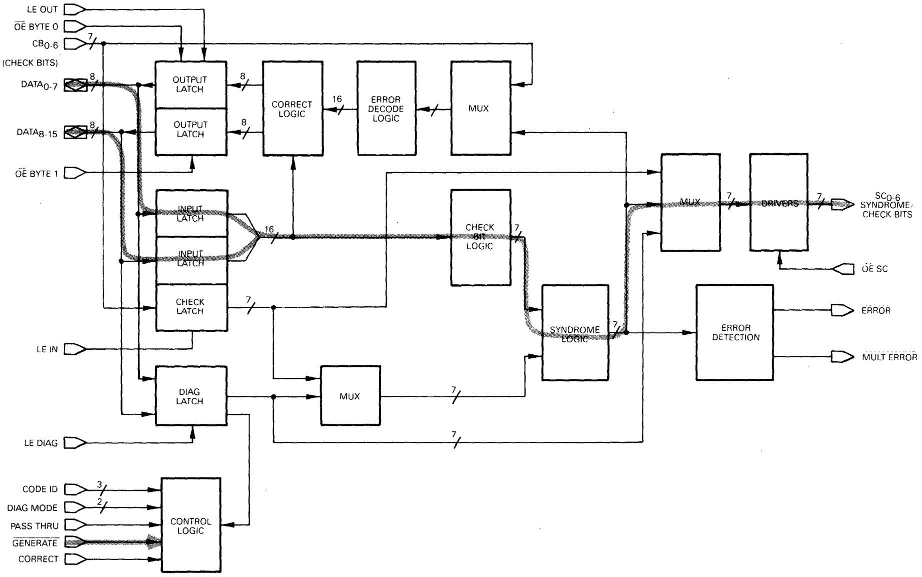

LE OUT
OE BYTE 0
CB0-6
(CHECK BITS)
DATA0-7
DATA8-15
OE BYTE 1
LE IN
LE DIAG
CODE ID
DIAG MODE
PASS THRU
GENERATE
CORRECT
OUTPUT LATCH
OUTPUT LATCH
INPUT LATCH
INPUT LATCH
CHECK LATCH
DIAG LATCH
CONTROL LOGIC
CORRECT LOGIC
ERROR DECODE LOGIC
MUX
CHECK BIT LOGIC
SYNDROME LOGIC
MUX
MUX
DRIVERS
ERROR DETECTION
SC0-6 SYNDROME/CHECK BITS
OE SC
ERROR
MULT ERROR
7
8
8
8
8
16
16
7
7
7
7
7
7
3
2

FIGURE 5 — ERROR DETECTION AND CORRECTION

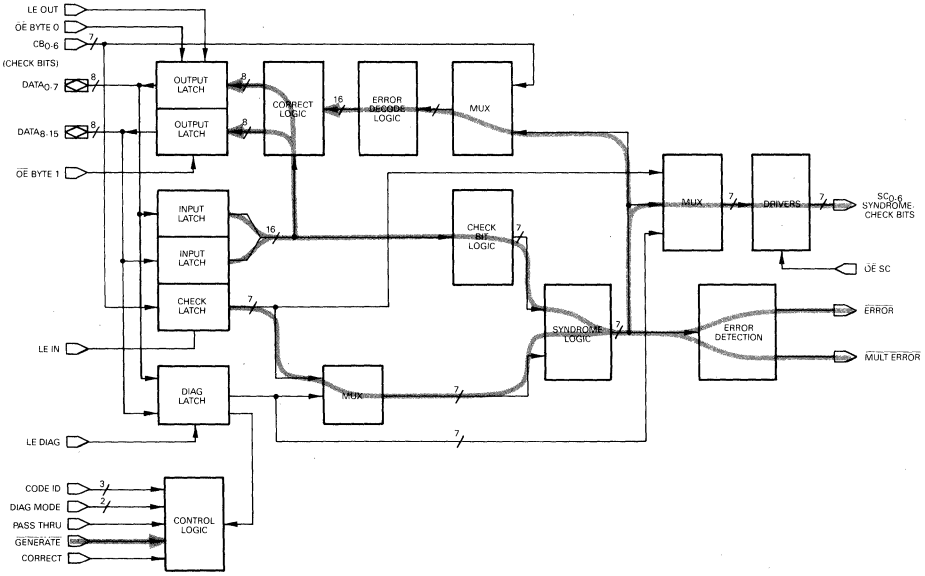

LE OUT
OE BYTE 0
CB0-6
(CHECK BITS)
DATA0-7
DATA8-15
OE BYTE 1
LE IN
LE DIAG
CODE ID
DIAG MODE
PASS THRU
GENERATE
CORRECT
OUTPUT LATCH
OUTPUT LATCH
INPUT LATCH
INPUT LATCH
CHECK LATCH
DIAG LATCH
CONTROL LOGIC
CORRECT LOGIC
ERROR DECODE LOGIC
MUX
CHECK BIT LOGIC
SYNDROME LOGIC
MUX
MUX
DRIVERS
ERROR DETECTION
SC0-6 SYNDROME/CHECK BITS
OE SC
ERROR
MULT ERROR
7
8
8
8
8
16
16
7
7
7
7
7
7
3
2

FIGURE 6 — DIAGNOSTIC CHECK BIT GENERATION

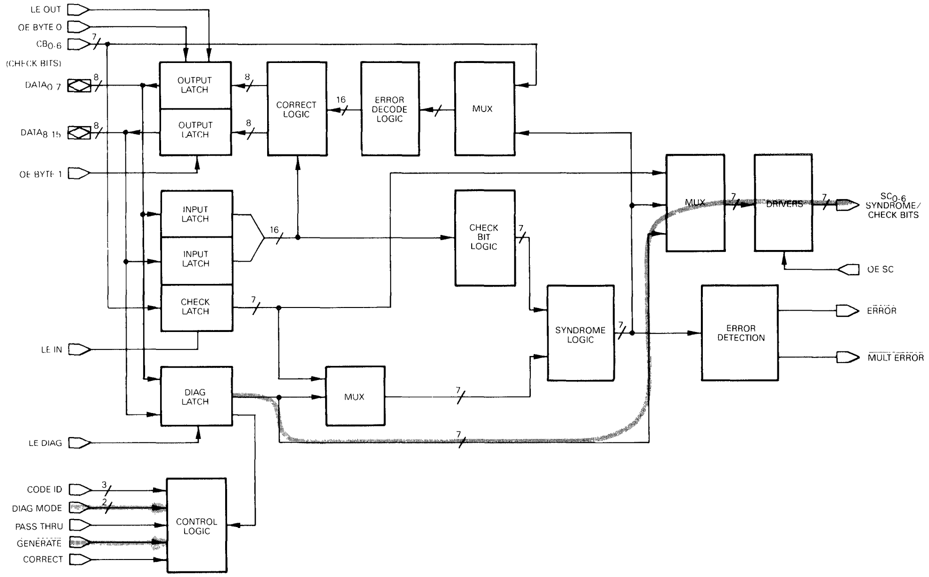
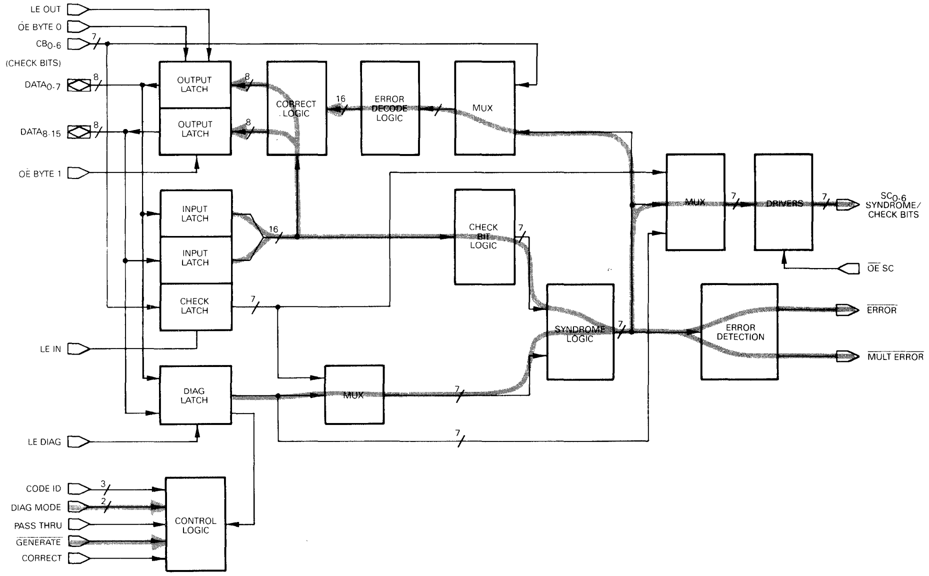

LE OUT
OE BYTE 0
CB0-6
(CHECK BITS)
DATA0-7
DATA8-15
OE BYTE 1
LE IN
LE DIAG
CODE ID
DIAG MODE
PASS THRU
GENERATE
CORRECT
OUTPUT LATCH
OUTPUT LATCH
INPUT LATCH
INPUT LATCH
CHECK LATCH
DIAG LATCH
CONTROL LOGIC
CORRECT LOGIC
ERROR DECODE LOGIC
MUX
MUX
MUX
DRIVERS
CHECK BIT LOGIC
SYNDROME LOGIC
ERROR DETECTION
SC0-6 SYNDROME/ CHECK BITS
OE SC
ERROR
MULT ERROR
7
8
8
16
16
7
7
7
7
7
7
3
2

FIGURE 7 — DIAGNOSTIC DETECT AND CORRECT


LE OUT
OE BYTE 0
CB0-6
(CHECK BITS)
DATA0-7
DATA8-15
OE BYTE 1
LE IN
LE DIAG
CODE ID
DIAG MODE
PASS THRU
GENERATE
CORRECT
OUTPUT LATCH
OUTPUT LATCH
INPUT LATCH
INPUT LATCH
CHECK LATCH
DIAG LATCH
CONTROL LOGIC
CORRECT LOGIC
ERROR DECODE LOGIC
MUX
MUX
MUX
DRIVERS
CHECK BIT LOGIC
SYNDROME LOGIC
ERROR DETECTION
SC0-6 SYNDROME/ CHECK BITS
OE SC
ERROR
MULT ERROR
7
8
8
16
16
7
7
7
7
7
7
3
2

CASCADING THE MC74F2960/MC74F2960A

The system configuration, as well as the specific function of various EDAC inputs and outputs, varies slightly depending upon the width of the data word.

The system configuration for 16-bit, 32-bit and 64-bit data words is shown in Figures 7, 8 and 9. In addition, accompanying figures and tables indicate the memory word format, diagnostic latch format, check bit encode, syndrome decode and ac calculations for each configuration.

When cascading to 32- or 64-bit configurations, syndrome bits must be fed back to the check bit inputs to correct an erroneous data word. Figure 9 and Table 18 illustrate the use of a 3-state buffer to control the multiplexing of check bits and syndrome bits into the EDAC(s).

Cascading to a 64-bit configuration requires additional MSI logic to generate a portion of the Syndrome and also the $\overline{\text{ERROR}}$ flag. The implementation shown in Figure 10 results in a different meaning for the $\overline{\text{MULT ERROR}}$ flag than in other configurations. $\overline{\text{MULT ERROR}}$ is HIGH if no errors or a 1-bit error is detected, but it is also HIGH for some 2-bit errors. In order to determine if an error is correctable, a DOUBLE ERROR output indicates that 2 errors have been detected when HIGH. Otherwise DOUBLE ERROR is Low.

16-BIT DATA WORD WIDTH

TABLE 9. 16-BIT DATA FORMAT

DATA		CHECK BITS					
BYTE 1	BYTE 0	CX	C0	C1	C2	C4	C8
15 8	7 0						

Uses Modified Hamming Code 16/22
- — 16 data bits
- — 6 check bits
- — 22 bits in total

FIGURE 8 — 16-BIT CONFIGURATION

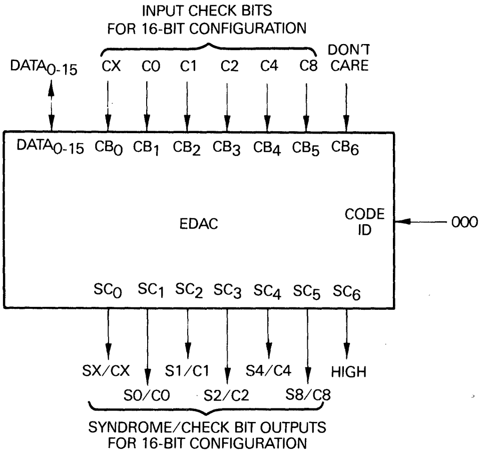

INPUT CHECK BITS
FOR 16-BIT CONFIGURATION
DON'T CARE
DATA0-15
CX
C0
C1
C2
C4
C8
DATA0-15
CB0
CB1
CB2
CB3
CB4
CB5
CB6
EDAC
CODE ID
000
SC0
SC1
SC2
SC3
SC4
SC5
SC6
SX/CX
S0/C0
S1/C1
S2/C2
S4/C4
S8/C8
HIGH
SYNDROME/CHECK BIT OUTPUTS
FOR 16-BIT CONFIGURATION

TABLE 10. 16-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

16-BIT DATA WORD WIDTH (continued)

TABLE 11. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

* — no errors detected
Number — the location of the single bit-in-error
T — two errors detected
M — three or more errors detected

TABLE 12. DIAGNOSTIC LATCH LOADING — 16-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

32-BIT DATA WORD WIDTH

TABLE 13. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* — no errors detected
Number — the location of the single bit-in-error
T — two errors detected
M — three or more errors detected

TABLE 14. DIAGNOSTIC LATCH LOADING — 32-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 — CODE ID 0
9	Slice 0/1 — CODE ID 1
10	Slice 0/1 — CODE ID 2
11	Slice 0/1 — DIAG MODE 0
12	Slice 0/1 — DIAG MODE 1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID 0
25	Slice 2/3 — CODE ID 1
26	Slice 2/3 — CODE ID 2
27	Slice 2/3 — DIAG MODE 0
28	Slice 2/3 — DIAG MODE 1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASS THRU
31	Don't Care

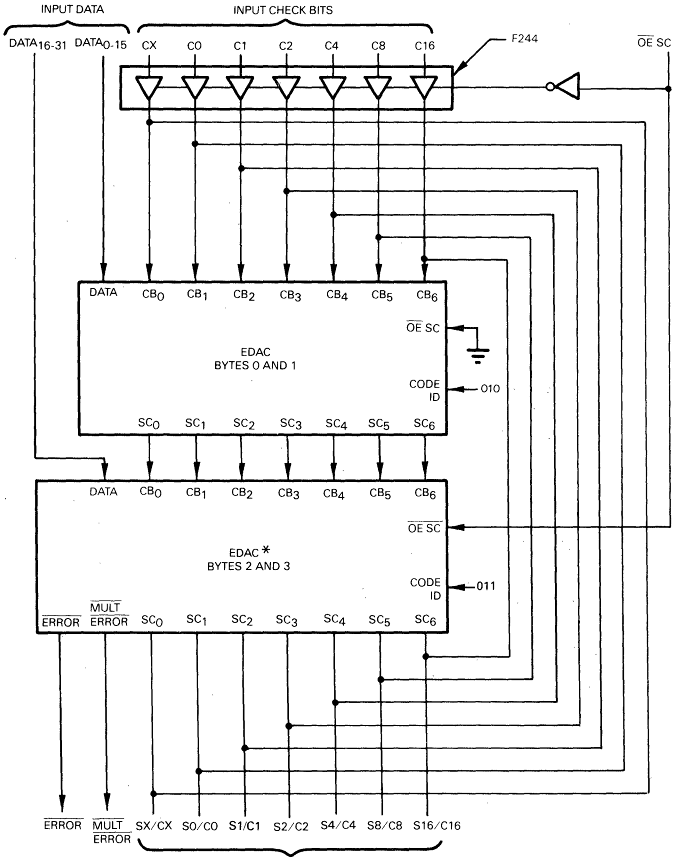
32-BIT DATA WORD WIDTH (continued)

TABLE 15. 32-BIT DATA FORMAT

DATA				CHECK BITS						
BYTE 3	BYTE 2	BYTE 1	BYTE 0	CX	C0	C1	C2	C4	C8	C16
31 24	23 16	15 8	7 0							

Uses Modified Hamming Code 32/39
- — 32 data bits
- — 7 check bits
- — 39 bits in total

FIGURE 9 — 32-BIT CONFIGURATION


INPUT DATA
INPUT CHECK BITS
DATA16-31
DATA0-15
CX
C0
C1
C2
C4
C8
C16
F244
OE SC
DATA
CB0
CB1
CB2
CB3
CB4
CB5
CB6
OE SC
EDAC
BYTES 0 AND 1
CODE ID
010
SC0
SC1
SC2
SC3
SC4
SC5
SC6
DATA
CB0
CB1
CB2
CB3
CB4
CB5
CB6
OE SC
EDAC *
BYTES 2 AND 3
CODE ID
011
ERROR
MULT ERROR
SC0
SC1
SC2
SC3
SC4
SC5
SC6
ERROR
MULT ERROR
SX/CX
S0/C0
S1/C1
S2/C2
S4/C4
S8/C8
S16/C16
OUTPUT SYNDROME/CHECK BITS

*Check Bit Latch is Forced Transparent in this Code ID Combination for this Slice.

32-BIT DATA WORD WIDTH (continued)

TABLE 16. 32-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

TABLE 17. KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-Bit Propagation Delay		Delay Calculation
From	To	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA IN	Corrected DATA OUT	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

64-BIT DATA WORD WIDTH

TABLE 18. 64-BIT DATA FORMAT

DATA								CHECK BITS							
BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0	CX	C0	C1	C2	C4	C8	C16	C32
63	48	47	32	31	16	15	0								

Uses Modified Hamming Code 64/72
- — 64 data bits
- — 8 check bits
- — 72 bits in total

64-BIT DATA WORD WIDTH (continued)

TABLE 19. 64-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

64-BIT DATA WORD WIDTH (continued)

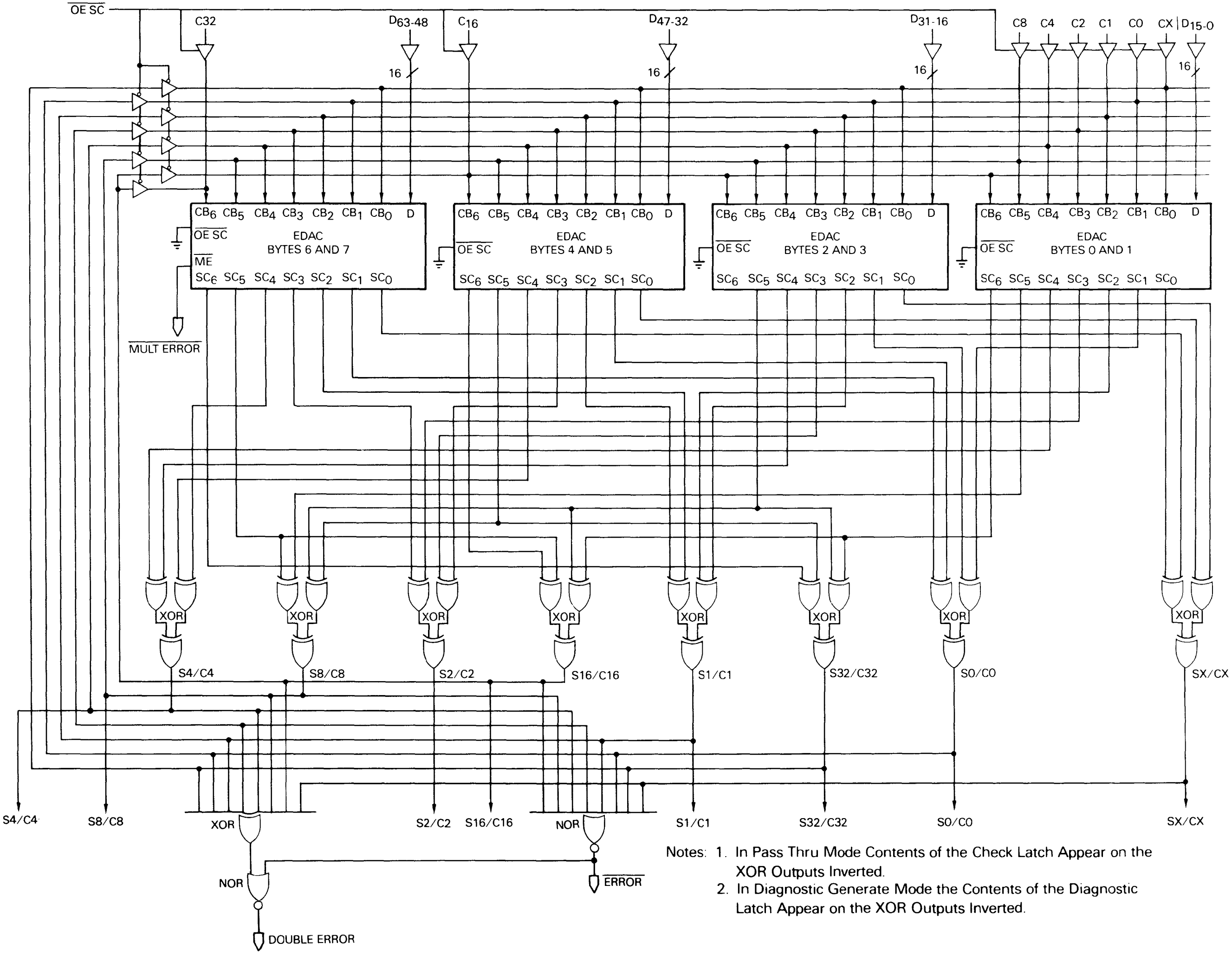

OE SC
C32
D63-48
C16
D47-32
D31-16
C8 C4 C2 C1 C0 CX
D15-0
16
CB6 CB5 CB4 CB3 CB2 CB1 CB0 D
EDAC
BYTES 6 AND 7
BYTES 4 AND 5
BYTES 2 AND 3
BYTES 0 AND 1
ME
SC6 SC5 SC4 SC3 SC2 SC1 SC0
MULT ERROR
XOR
S4/C4
S8/C8
S2/C2
S16/C16
S1/C1
S32/C32
S0/C0
SX/CX
NOR
ERROR
DOUBLE ERROR

FIGURE 10 — 64-BIT DATA CONFIGURATION

Notes: 1. In Pass Thru Mode Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch Appear on the XOR Outputs Inverted.

64-BIT DATA WORD WIDTH (continued)

TABLE 20. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* — no errors detected

Number — the location of the single bit-in-error

T — two errors detected

M — three or more errors detected

TABLE 21. DIAGNOSTIC LATCH LOADING — 64-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 — CODE ID 0
9	Slice 0/1 — CODE ID 1
10	Slice 0/1 — CODE ID 2
11	Slice 0/1 — DIAG MODE 0
12	Slice 0/1 — DIAG MODE 1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID 0
25	Slice 2/3 — CODE ID 1
26	Slice 2/3 — CODE ID 2
27	Slice 2/3 — DIAG MODE 0
28	Slice 2/3 — DIAG MODE 1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASS THRU

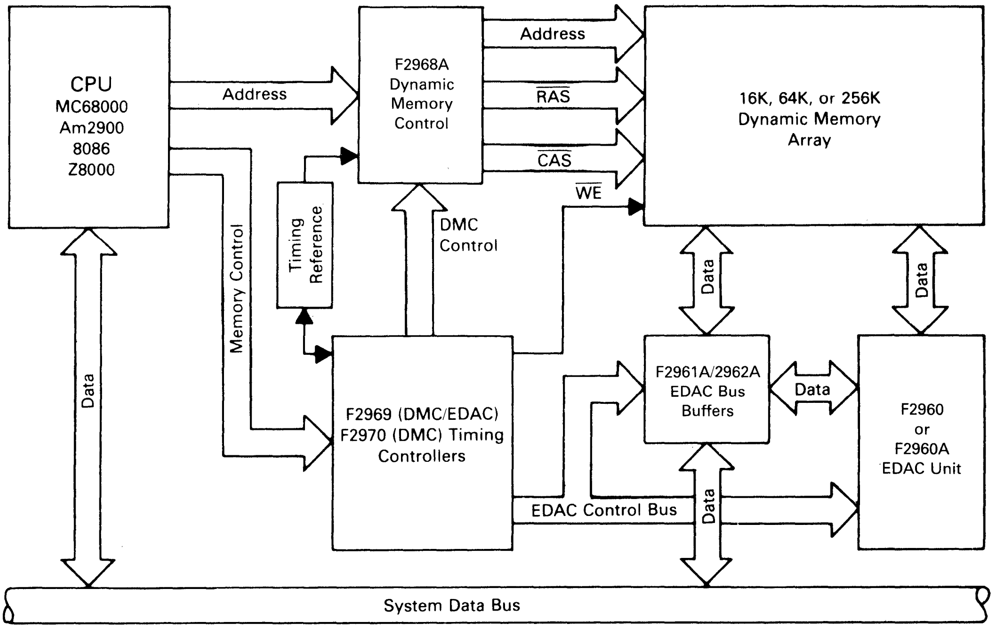
Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 — CODE ID 0
41	Slice 4/5 — CODE ID 1
42	Slice 4/5 — CODE ID 2
43	Slice 4/5 — DIAG MODE 0
44	Slice 4/5 — DIAG MODE 1
45	Slice 4/5 — CORRECT
46	Slice 4/5 — PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 — CODE ID 0
57	Slice 6/7 — CODE ID 1
58	Slice 6/7 — CODE ID 2
59	Slice 6/7 — DIAG MODE 0
60	Slice 6/7 — DIAG MODE 1
61	Slice 6/7 — CORRECT
62	Slice 6/7 — PASS THRU
63	Don't Care

64-BIT DATA WORD WIDTH (continued)

TABLE 22. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-Bit Propagation Delay		Delay Calculation
From	**To**	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA IN	Corrected DATA OUT	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

FIGURE 11 — HIGH PERFORMANCE COMPUTER MEMORY


CPU
MC68000
Am2900
8086
Z8000
Address
F2968A
Dynamic
Memory
Control
Address
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{WE}}$
16K, 64K, or 256K
Dynamic Memory
Array
Memory Control
Timing Reference
DMC
Control
Data
Data
Data
F2961A/2962A
EDAC Bus
Buffers
Data
F2960
or
F2960A
EDAC Unit
F2969 (DMC/EDAC)
F2970 (DMC) Timing
Controllers
EDAC Control Bus
Data
System Data Bus

MOTOROLA

MC74F2961A
MC74F2962A

4-BIT ERROR CORRECTION MULTIPLE BUS BUFFERS

Advance Information

4-BIT CORRECTION MULTIPLE BUS BUFFERS

DESCRIPTION — The MC74F2961A and MC74F2962A are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the MC74F2960/A Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The MC74F2961A provides an inverting data path beween the data bus (B_i) and the MC74F2960/A error correction data input (Y_i) and the MC74F2962A provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the MC74F2960/A and memory data bus, thereby optimizing internal data path speeds.

The MC74F2961A and MC74F2962A are 4-bit devices. Four devices are used to interface each 16-bit MC74F2960/A Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

- Provides complete data path interface between the MC74F2960/A Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- 3-State 24 mA Output to Data Bus
- 3-State Data Output to Memory
- Inverting Data Bus for MC74F2961A and Noninverting for MC74F2962A
- Data Bus Latches Allow Operation with Multiplexed Buses
- Space Saving 24-Pin 0.3″ Package

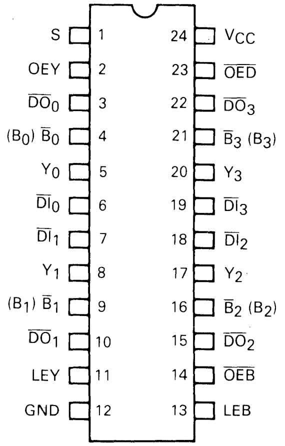
System Performance Improvement
Motorola 'A' System versus AMD Standard System

Mode	Device	Path	Am2960 Am2961	MC74F2960A/ 2961A	% Improvement with 'A'-System
Generate	2961/A	B to Y	25	12	52%
	2960/A	Data to S/C	32	20	38%
		Total Delay	**57**	**32**	**44%**
Detect	2961/A	D to Y	15	10	33%
	2960/A	Data to Error	32	19	41%
		Total Delay	**47**	**29**	**38%**
Correct	2961/A	D to Y	15	10	33%
	2960/A	Data to Data	65	42	35%
	2961/A	Y to B	20	13	35%
		Total Delay	**100**	**65**	**35%**

All delays are in nanoseconds and are manufacturer's published specifications.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

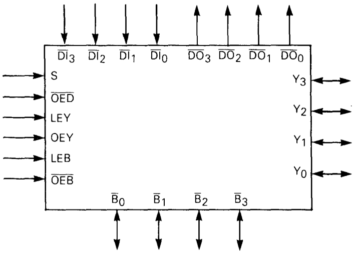
CONNECTION DIAGRAM
Top View


S 1
OEY 2
$\overline{DO}_0$ 3
(B_0) $\overline{B}_0$ 4
Y_0 5
$\overline{DI}_0$ 6
$\overline{DI}_1$ 7
Y_1 8
(B_1) $\overline{B}_1$ 9
$\overline{DO}_1$ 10
LEY 11
GND 12
24 V_{CC}
23 $\overline{OED}$
22 $\overline{DO}_3$
21 $\overline{B}_3$ (B_3)
20 Y_3
19 $\overline{DI}_3$
18 $\overline{DI}_2$
17 Y_2
16 $\overline{B}_2$ (B_2)
15 $\overline{DO}_2$
14 $\overline{OEB}$
13 LEB

Note: Pin 1 is marked for orientation

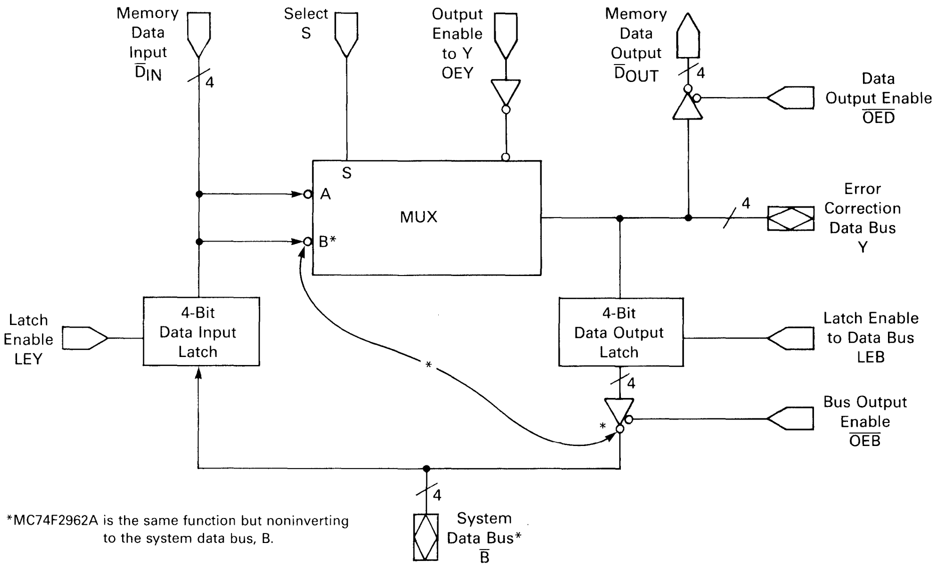
N Suffix — Case 724-02 (Plastic)
J Suffix — Case 758-01 (Ceramic)

LOGIC SYMBOL


$\overline{DI}_3$
$\overline{DI}_2$
$\overline{DI}_1$
$\overline{DI}_0$
$\overline{DO}_3$
$\overline{DO}_2$
$\overline{DO}_1$
$\overline{DO}_0$
S
$\overline{OED}$
LEY
OEY
LEB
$\overline{OEB}$
Y_3
Y_2
Y_1
Y_0
$\overline{B}_0$
$\overline{B}_1$
$\overline{B}_2$
$\overline{B}_3$

B-Bus is noninverting for MC74F2962A

BLOCK DIAGRAM


Memory
Data
Input
$\overline{D}_{IN}$
4
Select
S
Output
Enable
to Y
OEY
Memory
Data
Output
$\overline{D}_{OUT}$
4
Data
Output Enable
$\overline{OED}$
S
A
MUX
B*
Error
Correction
Data Bus
Y
4
Latch
Enable
LEY
4-Bit
Data Input
Latch
4-Bit
Data Output
Latch
Latch Enable
to Data Bus
LEB
*
4
Bus Output
Enable
$\overline{OEB}$
*
4
System
Data Bus*
$\overline{B}$

*MC74F2962A is the same function but noninverting to the system data bus, B.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 9, 16, 21	B_0, B_1, B_2, B_3	I/O	The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the MC74F2961A ($\overline{B}_i$) and noninverting for the MC74F2962A (B_i).
14	$\overline{OEB}$	I	The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW, data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH, the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.
13	LEB	I	Latch Enable for the Data Output Latch. When LEB is HIGH, the latch is transparent and Y-Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.
5, 8, 17, 20	Y_0, Y_1, Y_2, Y_3	I/O	The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.
11	LEY	I	The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.
2	OEY	I	Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH, data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW, the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.
1	S	I	The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).
3, 10, 15, 22	$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$	O	The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.
23	$\overline{OED}$	I	Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.
6, 7, 18, 19	$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$	I	The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{\text{DI}}_i$	$\overline{\text{B}}_i$* MC74F2961A	B_i* MC74F2962A	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{\text{OEB}}$ = HIGH for B data input

B-BUS OUTPUT

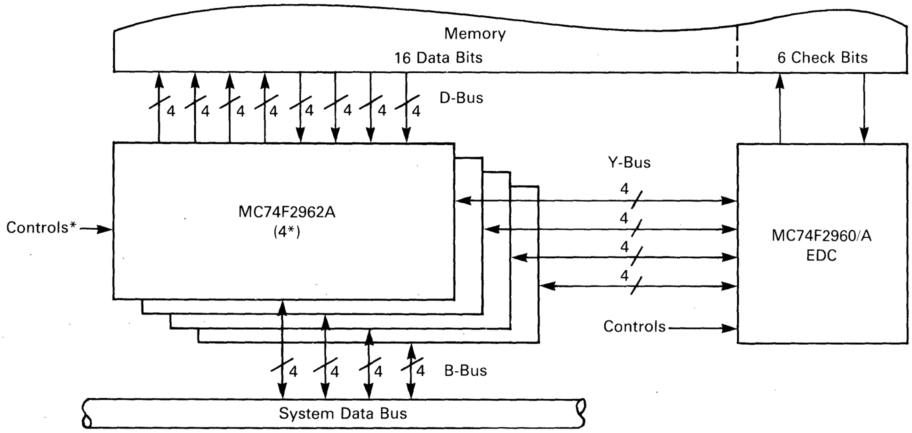
Y* Input	LEB	$\overline{\text{OEB}}$	$\overline{\text{B}}$ MC74F2961A	B MC74F2962A
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{\text{DO}}$ PORT OUTPUT

Y	$\overline{\text{OED}}$	$\overline{\text{DO}}$
X	H	Z
L	L	H
H	L	L

APPLICATION



*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs For High Output State	−0.5 V to V_{CC} Max
DC Input Voltage	5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Stress above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0°C to +70°C
Supply Voltage	+4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
Y BUS							
V_{OH}	Output HIGH Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3.0$ mA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16$ mA		0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, $I_{IN} = -18$ mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, $V_{IN} = 0.4$ V	OEY = LOW			−1.2	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 2.7$ V	OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 5.5$ V	OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	$V_O = 0.4$ V			−1.2	mA
			$V_O = 2.4$ V			+100	μA
B BUS							
V_{OH}	Output HIGH Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15$ mA	2.0			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24$ mA		0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, $I_{IN} = -18$ mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, $V_{IN} = 0.4$ V	$\overline{OEB}$ = HIGH			−0.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 2.7$ V	$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 5.5$ V	$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	$V_O = 0.4$ V			−0.6	μA
			$V_O = 2.4$ V			+100	
DO OUTPUTS							
V_{OH}	Output HIGH Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100$ μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 1.0$ mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	$V_O = 0.4$ V			−50	μA
			$V_O = 2.4$ V			+50	
DI INPUTS AND CONTROLS							
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_C	Input Clamp Voltage	V_{CC} = MIN, $I_{IN} = -18$ mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, $V_{IN} = 0.4$ V	DI Inputs			−0.6	mA
			Controls			−0.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 2.7$ V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 7.0$ V				100	μA
POWER SUPPLY							
I_{CC}	Power Supply Current	V_{CC} = MAX			60	75	mA

NOTES: 1. For conditions as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING TEST CIRCUIT

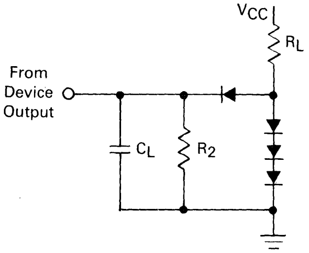


FIGURE 1.

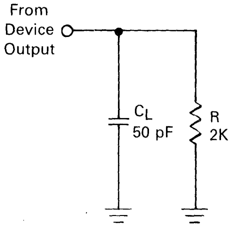


FIGURE 2.

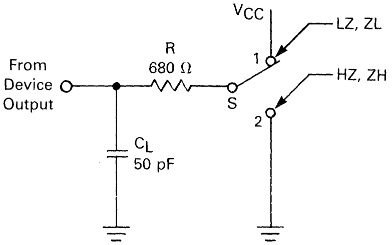


FIGURE 3.

MC74F261A SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions	COMMERCIAL		Units
			Min	Max	
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)	Figure 1 C_L = 5.0 pF R_L = 390 Ω R_2 = 1.0 kΩ		12	ns
t_{PHL}				12	ns
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)			10	ns
t_{PHL}				10	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)			13	ns
t_{PHL}				13	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)			16	ns
t_{PHL}				16	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y			14	ns
t_{PZL}				14	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y			14	ns
t_{PLZ}				14	ns
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)	Figure 1 C_L = 50 pF R_L = 270 Ω R_2 = 1.0 kΩ		16	ns
t_{PHL}				16	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)			13	ns
t_{PHL}				13	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)	Figure 1 C_L = 300 pF R_L = 270 Ω R_2 = 1.0 kΩ		23	ns
t_{PHL}				23	ns
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$	Figure 1 C_L = 50 pF R_L = 270 Ω R_2 = 1.0 kΩ		14	ns
t_{PZL}				14	ns
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$			14	ns
t_{PHZ}				14	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)	Figure 2 C_L = 50 pF R = 2.0 kΩ		11	ns
t_{PHL}				11	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	S = 2 Figure 3 C_L = 50 pF R = 680 Ω		14	ns
t_{PZL}		S = 1		14	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$	S = 2		14	ns
t_{PLZ}		S = 1		14	ns
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1 C_L = 50 pF R_L = 390 Ω R_2 = 1.0 kΩ	4		ns
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)		6		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1 C_L = 50 pF R_L = 270 Ω R_2 = 1.0 kΩ	4		ns
t_H	Y to LEB Hold Time (OEY = LOW)		6		ns

MC74F262A SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions	COMMERCIAL		Units
			Min	Max	
t_{PLH}	Propagation Delay B to Y (Latch Transparent, OEY = LEY = HIGH)	Figure 1 C_L = 5.0 pF R_L = 390 Ω R_2 = 1.0 kΩ		13	ns
t_{PHL}				13	ns
t_{PLH}	Propagation Delay $\overline{\text{DI}}$ to Y (OEY = HIGH, S = LOW)			10	ns
t_{PHL}				10	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)			14	ns
t_{PHL}				14	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)			16	ns
t_{PHL}				16	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y			14	ns
t_{PZL}				14	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y			14	ns
t_{PLZ}				14	ns
t_{PLH}	Propagation Delay LEB to B ($\overline{\text{OEB}}$ = LOW)	Figure 1 C_L = 50 pF R_L = 270 Ω R_2 = 1.0 kΩ		16	ns
t_{PHL}				16	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{\text{OEB}}$ = LOW, OEY = LOW)			14	ns
t_{PHL}				14	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{\text{OEB}}$ = LOW, OEY = LOW)	Figure 1 C_L = 300 pF R_L = 270 Ω R_2 = 1.0 kΩ		24	ns
t_{PHL}				24	ns
t_{PZH}	B Bus Output Enable Time $\overline{\text{OEB}}$ to B	Figure 1 C_L = 50 pF R_L = 270 Ω R_2 = 1.0 kΩ		14	ns
t_{PZL}				14	ns
t_{PLZ}	B Bus Output Disable Time $\overline{\text{OEB}}$ to B			14	ns
t_{PHZ}				14	ns
t_{PLH}	Propagation Delay Y to $\overline{\text{DO}}$ ($\overline{\text{OED}}$ = OEY = LOW)	Figure 2 C_L = 50 pF R = 2.0 kΩ		11	ns
t_{PHL}				11	ns
t_{PZH}	$\overline{\text{DO}}$ Output Enable Time $\overline{\text{OED}}$ to $\overline{\text{DO}}$	S = 2 Figure 3 C_L = 50 pF R = 680 Ω		14	ns
t_{PZL}		S = 1		14	ns
t_{PHZ}	$\overline{\text{DO}}$ Output Disable Time $\overline{\text{OED}}$ to $\overline{\text{DO}}$	S = 2		14	ns
t_{PLZ}		S = 1		14	ns
t_S	B to LEY Set-up Time ($\overline{\text{OEB}}$ = HIGH)	Figure 1 C_L = 50 pF R_L = 390 Ω R_2 = 1.0 kΩ	4		ns
t_H	B to LEY Hold Time ($\overline{\text{OEB}}$ = HIGH)		6		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1 C_L = 50 pF R_L = 270 Ω R_2 = 1.0 kΩ	4		ns
t_H	Y to LEB Hold Time (OEY = LOW)		6		ns

MOTOROLA

Advance Information

Dynamic Memory Controller (DMC) for 256K DRAMs

MC74F2968A

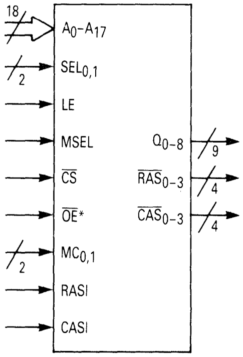
The MC74F2968A will be dual marked with the AMD part number Am2968A to indicate that it is a direct replacement for the Am2968A.

The MC74F2968A Dynamic Memory Controller (DMC) is designed to be an integral part of today's high performance memory systems. The DMC functions as the address controller between any processor and Dynamic memory array. Using its two 9-bit address latches, the DMC holds the Row and Column addresses for any DRAM up to 256K. These latches and the two 9-bit Row/Column Refresh address counters feed into a 9-bit, 4-input MUX, for output to the Dynamic RAM address lines. Each of the four $\overline{RAS}_N$ and $\overline{CAS}_N$ outputs is selected by the outputs of the Bank Select latch, which is driven by the two high-order address bits.

The MC74F2968A has two basic modes of operation, read/write and refresh. In the refresh mode, the Row and Column counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the Row counter is used, generating up to 512 addresses to refresh a 512-cycle-refresh 256K DRAM. When memory scrubbing is being performed, both the Row and Column counters are utilized to perform read-modify-write cycles. In this mode, all $\overline{RAS}_N$ outputs will be active, while only $\overline{CAS}_N$ output is active at a time.

- Provides Control for 16K, 64K, and 256K Dynamic RAMs
- Outputs Directly Drive up to 88 DRAMs, with a Guaranteed, Worst-Case Limit on the Undershoot
- Highest-Order Two Address Bits Select One of Four Banks of RAMs
- Separate Output Enable for Multi-Channel Access to Memory on Surface-Mount Packages
- Supports Scrubbing Operations and Other Specially Access Modes
- Upgrade Path to 74F29368 1M-Bit DMC

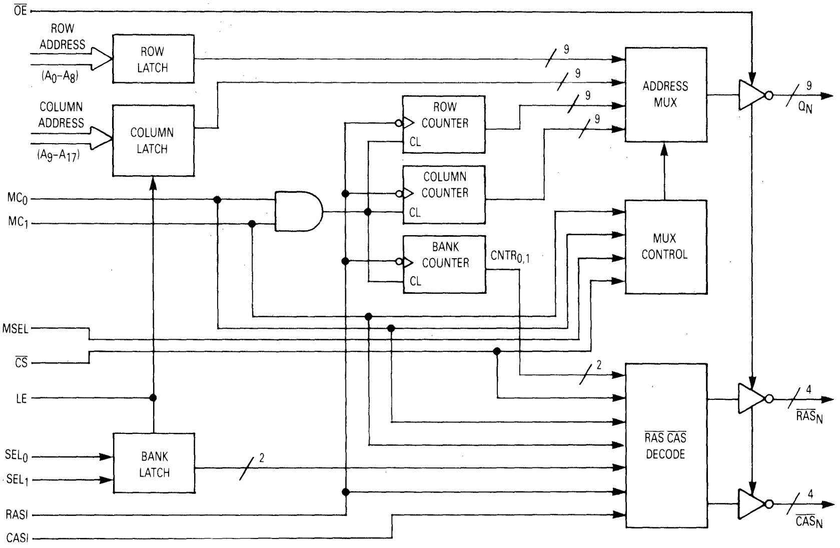
LOGIC DIAGRAM


18
A0-A17
SEL0,1
2
LE
MSEL
CS
OE*
MC0,1
2
RASI
CASI
Q0-8
9
RAS0-3
4
CAS0-3
4

Parameter	CERDIP	PDIP	LCC	PLCC	Units
θ_{JA}	37	55	31	35	°C/Watt
θ_{JC}	10	N/A	6	N/A	

*Available only on surface mount packages.

BLOCK DIAGRAM

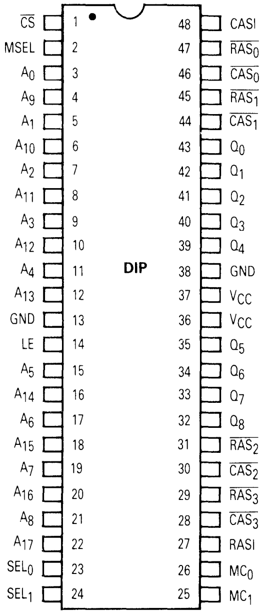

OE
ROW ADDRESS
(A0-A8)
ROW LATCH
COLUMN ADDRESS
(A9-A17)
COLUMN LATCH
MC0
MC1
ROW COUNTER
CL
COLUMN COUNTER
CL
BANK COUNTER
CL
CNTR0,1
9
9
9
9
ADDRESS MUX
9
QN
MUX CONTROL
MSEL
CS
LE
SEL0
SEL1
BANK LATCH
2
2
RASI
CASI
RAS CAS DECODE
4
RASN
4
CASN

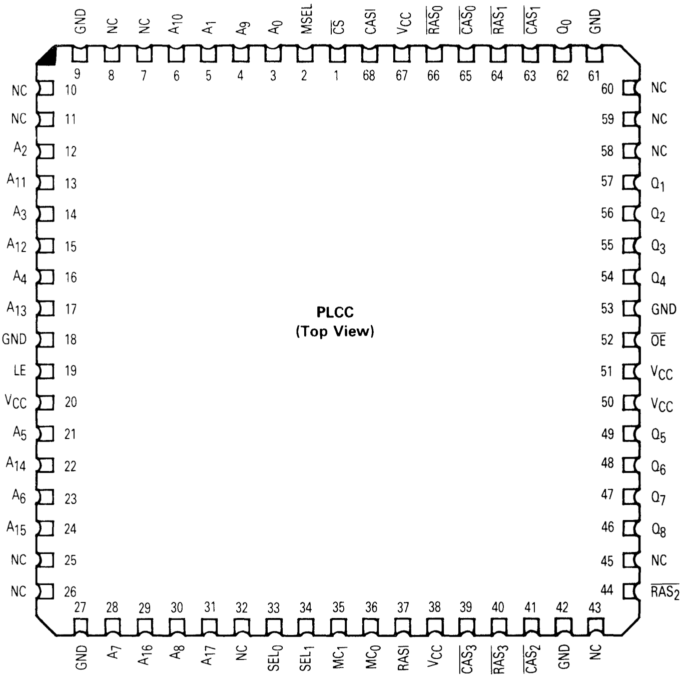
This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION

The MC74F2968A provides all the required data and refresh addresses needed by the dynamic RAM memory. In normal operation, the Row and Column addresses are multiplexed to the dynamic RAM by using MSEL, with the corresponding $\overline{RAS}_i$ and $\overline{CAS}_i$ signals activated to strobe the addresses into the RAM. High capacitance drivers on the outputs allow the DMC to drive four banks of 16-bit words, including a 6-bit checkword, for a total of 88 DRAMs.

CONNECTIONS DIAGRAMS


DIP
1 $\overline{CS}$
2 MSEL
3 A_0
4 A_9
5 A_1
6 A_{10}
7 A_2
8 A_{11}
9 A_3
10 A_{12}
11 A_4
12 A_{13}
13 GND
14 LE
15 A_5
16 A_{14}
17 A_6
18 A_{15}
19 A_7
20 A_{16}
21 A_8
22 A_{17}
23 SEL_0
24 SEL_1
48 CASI
47 $\overline{RAS_0}$
46 $\overline{CAS_0}$
45 $\overline{RAS_1}$
44 $\overline{CAS_1}$
43 Q_0
42 Q_1
41 Q_2
40 Q_3
39 Q_4
38 GND
37 V_{CC}
36 V_{CC}
35 Q_5
34 Q_6
33 Q_7
32 Q_8
31 $\overline{RAS_2}$
30 $\overline{CAS_2}$
29 $\overline{RAS_3}$
28 $\overline{CAS_3}$
27 RASI
26 MC_0
25 MC_1


PLCC
(Top View)
9 GND
8 NC
7 NC
6 A_{10}
5 A_1
4 A_9
3 A_0
2 MSEL
1 $\overline{CS}$
68 CASI
67 V_{CC}
66 $\overline{RAS_0}$
65 $\overline{CAS_0}$
64 $\overline{RAS_1}$
63 $\overline{CAS_1}$
62 Q_0
61 GND
10 NC
11 NC
12 A_2
13 A_{11}
14 A_3
15 A_{12}
16 A_4
17 A_{13}
18 GND
19 LE
20 V_{CC}
21 A_5
22 A_{14}
23 A_6
24 A_{15}
25 NC
26 NC
27 GND
28 A_7
29 A_{16}
30 A_8
31 A_{17}
32 NC
33 SEL_0
34 SEL_1
35 MC_1
36 MC_0
37 RASI
38 V_{CC}
39 $\overline{CAS_3}$
40 $\overline{RAS_3}$
41 $\overline{CAS_2}$
42 GND
43 NC
60 NC
59 NC
58 NC
57 Q_1
56 Q_2
55 Q_3
54 Q_4
53 GND
52 $\overline{OE}$
51 V_{CC}
50 V_{CC}
49 Q_5
48 Q_6
47 Q_7
46 Q_8
45 NC
44 $\overline{RAS_2}$

PIN DESCRIPTION

A_0–A_{17} Address Inputs (Input (18))

A_0–A_8 are latched in as the nine-bit Row Address for the RAM. These inputs drive Q_0–Q_8 when the F2968A is in the Read/Write mode and MSEL is LOW. A_9–A_{17} are latched in as the Column Address, and will drive Q_0–Q_8 when MSEL is HIGH and the DMC is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.

SEL_{0-1} Bank Select (Input (2))

These two inputs are normally the two higher-order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the $\overline{RAS}_i$ and $\overline{CAS}_i$ signals after RASI and CASI go HIGH.

LE Latch Enable (Input (1))

This active-HIGH input causes the Row, Column, and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.

MSEL Multiplexer Select (Input (1))

This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on $MC_{0,1}$.

$\overline{CS}$ $\overline{\text{Chip Select}}$ (Input (1))

This active-LOW input is used to select the DMC. When $\overline{CS}$ is active, the F2968A operates normally in all four modes. When $\overline{CS}$ goes HIGH, the device will not enter the Read/Write mode. This allows more than one F2968A DMC to control the same memory, thus providing an easy method for expanding the memory size.

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input (1))

This active-LOW input enables/disables the output signals. When $\overline{OE}$ is HIGH, the outputs of the DMC enter the high-impedance state. $\overline{OE}$ is only available on the surface-mount packages.

MC_{0-1} Mode Control (Input (2))

These inputs are used to specify which of the four operating modes the DMC should be using. The description of the four operating modes is given in Table 1.

Q_{0-8} Address Outputs (Outputs (9))

These address outputs will feed the DRAM address inputs, and provide drive for memory systems up to 500 picofarads in capacitance.

RASI Row Address Strobe (Input (1))

During normal memory cycles, the decoded $\overline{RAS_i}$ output ($\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, or $\overline{RAS_3}$) is forced LOW after receipt of RASI. In either Refresh mode, all four $\overline{RAS_i}$ outputs will go LOW following RASI going HIGH.

$\overline{RAS_{0-3}}$ $\overline{\text{Row Address Strobe}}$ (Output (4))

Each one of the Row Address Strobe outputs provides a $\overline{RAS_i}$ signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL_0 and SEL_1 and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.

CASI Column Address Strobe (Input (1))

This input going active will cause the selected $\overline{CAS_i}$ output to be forced LOW.

$\overline{CAS_{0-3}}$ $\overline{\text{Column Address Strobe}}$ (Output (4))

During normal Read/Write cycles the two select bits (SEL_0, SEL_1) determine which $\overline{CAS_i}$ output will go active following CASI going HIGH. When memory scrubbing is performed, only the $\overline{CAS_i}$ signal selected by $CNTR_0$ and $CNTR_1$ will be active (see $\overline{CAS}$ Output Function Table). For non-scrubbing cycles, all four $\overline{CAS_i}$ outputs remain HIGH.

MODE CONTROL FUNCTION TABLE

MC_1	MC_0	Operating Mode
0	0	Refresh without Scrubbing. Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $\overline{RAS_i}$ outputs are active while the four $\overline{CAS_i}$ signals are kept HIGH.
0	1	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $\overline{RAS_i}$ go active in response to RASI, while only one $\overline{CAS_i}$ output goes LOW in response to CASI. The Bank Counter keeps track of which $\overline{CAS_i}$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	Read/Write. This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL. SEL_0 and SEL_1 are decoded to determine which $\overline{RAS_i}$ and $\overline{CAS_i}$ will be active.
1	1	Clear Refresh Counter. This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{RAS_i}$ are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed.

ADDRESS OUTPUT FUNCTION TABLE

$\overline{CS}$	MC_1	MC_0	MSEL	Mode	MUX Output
0	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	1	Read/Write	Column Address Latch
			0		Row Address Latch
	1	1	X	Clear Refresh Counter	Zero
1	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	X	Read/Write	Zero
	1	1	X	Clear Refresh Counter	Zero

$\overline{RAS}$ OUTPUT FUNCTION TABLE

RASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	Mode	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
0	X	X	X	X	X	X	1	1	1	1
1	0	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1	X	X	Refresh with Scrubbing	0	0	0	0
		1	0	0	0	Read/Write	0	1	1	1
				0	1		1	0	1	1
				1	0		1	1	0	1
				1	1		1	1	1	0
		1	1	X	X	Clear Refresh Counter	0	0	0	0
	1	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1			Refresh with Scrubbing	0	0	0	0
		1	0			Read/Write	1	1	1	1
		1	1			Clear Refresh Counter	0	0	0	0

$\overline{CAS}$ OUTPUT FUNCTION TABLE

Inputs						Internal		Outputs			
CASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	$CNTR_1$	$CNTR_0$	$\overline{CAS}_0$	$\overline{CAS}_1$	$\overline{CAS}_2$	$\overline{CAS}_3$
1	0	0	0	X	X	X	X	1	1	1	1
		0	1	X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	0	0	X	X	0	1	1	1
				0	1			1	0	1	1
				1	0			1	1	0	1
				1	1			1	1	1	0
		1	1	X	X	X	X	1	1	1	1
	1	0	0	X	X	X	X	1	1	1	1
		0	1	X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	X	X	X	X	1	1	1	1
		1	1								
0	X	X	X	X	X	X	X	1	1	1	1

Input Latches

For those systems where addresses and data are multiplexed onto a single bus, the DMC has latches to hold the address information. The twenty input latches (Row, Column, and Bank Select) are transparent when Latch Enable (LE) is HIGH and will latch the input data meeting setup and hold time requirements when LE goes LOW. For systems where the processor has separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counters

The two 9-bit refresh counters make it possible to support 128, 256, and 512 line refresh. External control over which type of refresh is to be performed allows the user maximum flexibility when choosing the refreshing scheme. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counters are advanced at the HIGH-to-LOW transition of RASI. This assures a stable counter output for the next refresh cycle.

Refresh with Error Correction

The F2968A makes it possible to correct single-bit errors in parallel with performing dynamic RAM refresh cycles. This "scrubbing" of memory can be done periodically as a background routine when the memory is not being used by the processor. In a memory scrubbing cycle ($MC_{1,0}$ = 01), the Row Address is strobed into all four banks with all four $\overline{RAS_i}$ outputs going LOW.

The Column Address is strobed into a single bank with the activated $\overline{CAS_i}$ output being selected by the Bank Counter. This type of cycle is used to simultaneously refresh the addressed row in all banks and read and correct (if necessary) one word in memory; thereby reducing the overhead associated with Error Detection and Correction. When doing refresh with memory scrubbing, both the Row and Column counters are multiplexed to the dynamic RAM address lines by using MSEL. Using the Refresh with Memory Scrubbing mode implies the presence of an error correcting facility such as the Am2960A EDC unit. When doing refresh without scrubbing, all four $\overline{RAS_i}$ still go LOW but the $\overline{CAS_i}$ outputs are all driven HIGH so as not to activate the output lines of the memory.

Decoupling

Due to the high switching speeds and high drive capability of the F2968A, it is necessary to decouple the device for proper operation. 1 μF multilayer ceramic capacitors are recommended for decoupling (see Figure 1a). It is important to mount the capacitors as close as possible to the power pins (V_{CC}, GND) to minimize lead inductance and noise. A ground plane is recommended.

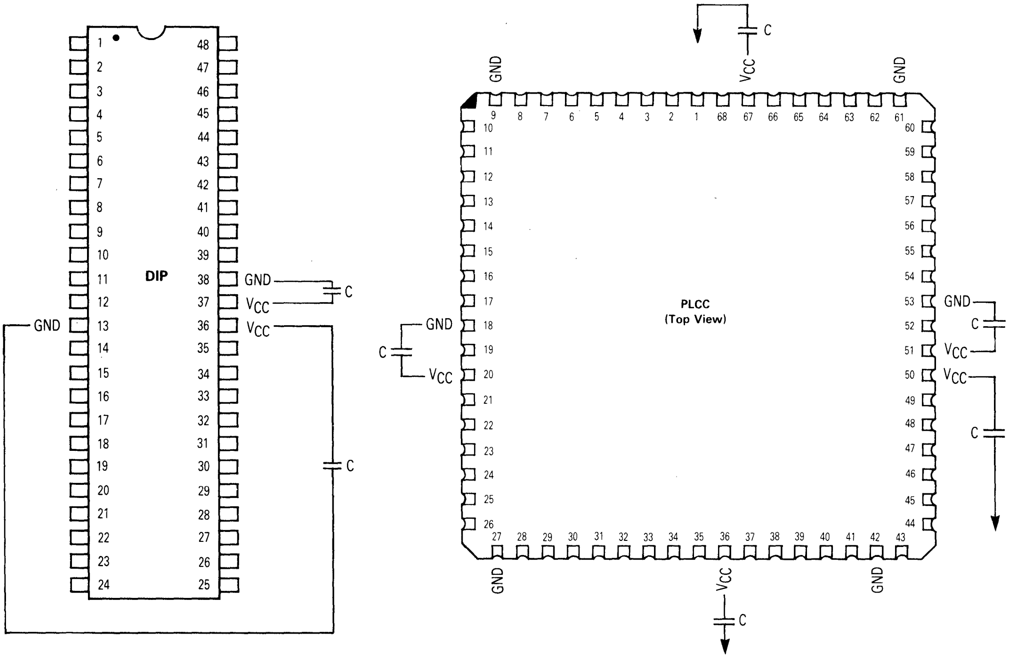


Figure 1a. Decoupling Connection Diagrams

V_{ONP}

The guaranteed maximum undershoot voltage of the F2968A is -0.5 volts. V_{ONP} is measured with respect to ground (Figure 1b). Note that the ground of the capacitive load must be the same as for the V_{CC} pin(s).

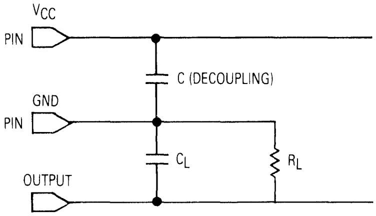
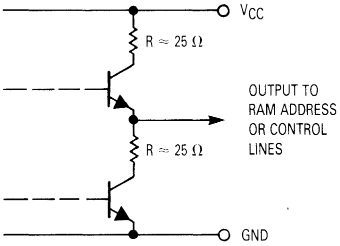


Figure 1b.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25 Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels. External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.



Typical Output Driver

APPLICATIONS

Timing Control

To obtain optimum performance and maximum design flexibility, the timing and control logic for the memory system has been kept a separate function. For systems implementing Error Detection and Correction, the F2969 Memory Timing Controller (MTC) provides all the necessary control signals for the F2968A, F2961A/62A EDC Bus Buffers, and the F2960A EDC unit (See Figure 2a). Systems not using EDC, can use the F2970 MTC to provide the control for the F2968A (See Figure 2b). Both the F2969 and F2970 Memory Timing Controllers use a delay line to provide the most accurate timing reference from which the control signals are derived.

Memory Expansion

With a 9-bit address path, the F2968A can control up to one megaword memory when using 256K dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to double the memory size by using two F2968As. Memory can be increased in one megaword increments by adding another DMC unit. A four-megaword memory system implementing EDC is shown in Figure 3.

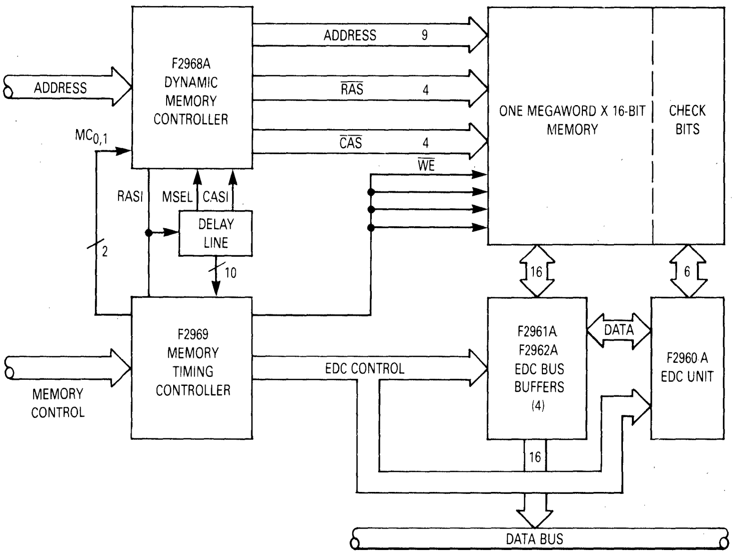

F2968A
DYNAMIC
MEMORY
CONTROLLER
ADDRESS
$MC_{0,1}$
ADDRESS 9
$\overline{RAS}$ 4
$\overline{CAS}$ 4
$\overline{WE}$
ONE MEGAWORD X 16-BIT
MEMORY
CHECK
BITS
RASI
MSEL
CASI
DELAY
LINE
2
10
16
6
F2969
MEMORY
TIMING
CONTROLLER
MEMORY
CONTROL
EDC CONTROL
F2961A
F2962A
EDC BUS
BUFFERS
(4)
DATA
F2960A
EDC UNIT
16
DATA BUS

Figure 2a. One Megaword Dynamic Memory with Error Detection and Correction

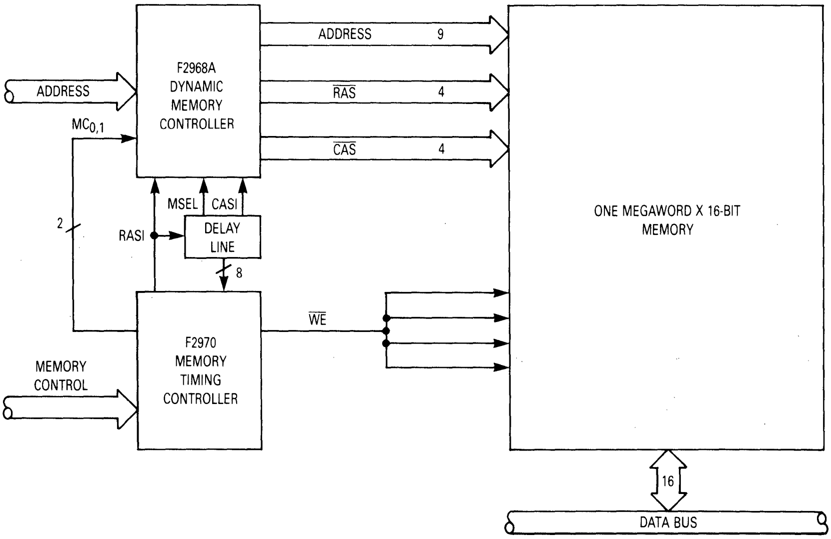

F2968A
DYNAMIC
MEMORY
CONTROLLER
ADDRESS
$MC_{0,1}$
ADDRESS 9
$\overline{RAS}$ 4
$\overline{CAS}$ 4
ONE MEGAWORD X 16-BIT
MEMORY
MSEL
CASI
2
RASI
DELAY
LINE
8
$\overline{WE}$
F2970
MEMORY
TIMING
CONTROLLER
MEMORY
CONTROL
16
DATA BUS

Figure 2b. One Megaword Dynamic Memory

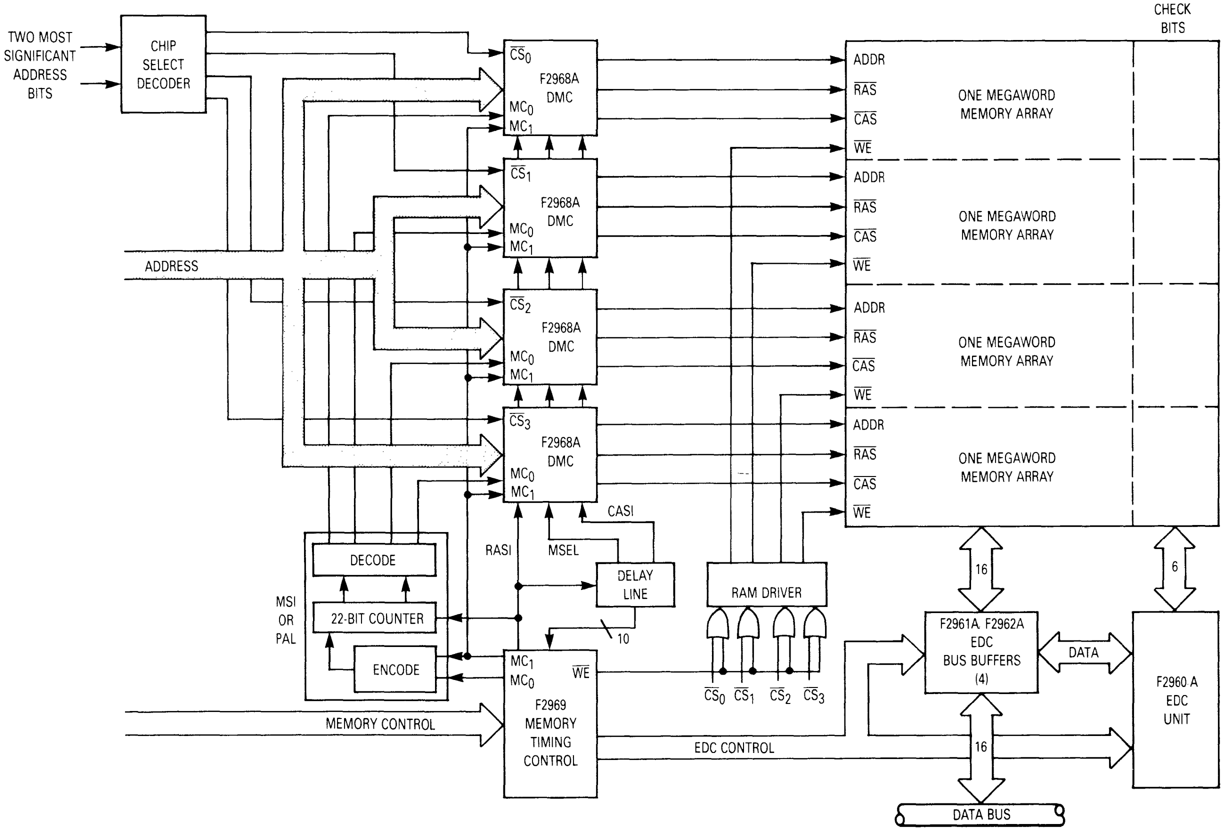

TWO MOST
SIGNIFICANT
ADDRESS
BITS
CHIP
SELECT
DECODER
ADDRESS
$\overline{CS}_0$
F2968A
DMC
MC_0
MC_1
$\overline{CS}_1$
$\overline{CS}_2$
$\overline{CS}_3$
CHECK
BITS
ADDR
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
ONE MEGAWORD
MEMORY ARRAY
RASI
MSEL
CASI
DELAY
LINE
10
MSI
OR
PAL
DECODE
22-BIT COUNTER
ENCODE
MEMORY CONTROL
F2969
MEMORY
TIMING
CONTROL
$\overline{WE}$
RAM DRIVER
$\overline{CS}_0$ $\overline{CS}_1$ $\overline{CS}_2$ $\overline{CS}_3$
EDC CONTROL
16
6
F2961A, F2962A
EDC
BUS BUFFERS
(4)
DATA
F2960 A
EDC
UNIT
DATA BUS

Figure 3. Four Megaword Error Correcting Memory

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . −55°C to +150°C
Supply Voltage to Ground
Potential Continuous . . . . −0.5 V to +7 V
DC Voltage Applied to Outputs for
High Output State . . . . −0.5 V to $+V_{CC}$ Max
DC Input Voltage . . . . −0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

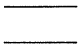
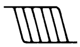
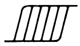
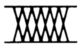
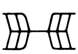
Commercial
T_A (Ambient) . . . . 0 to +70°C
V_{CC} . . . . 5 V to ±10%
Min . . . . 4.5 V
Max . . . . 5.5 V

DC CHARACTERISTICS (over operating ranges unless otherwise specified)

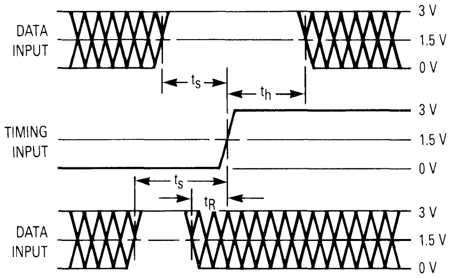
Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL} I_{OH} = −1 mA	COMM	2.7			Volts
			MIL	2.5			
V_{OL}	Output LOW Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 1 mA			0.5	Volts
			I_{OL} = 12 mA			0.8	
V_{IH}	Input HIGH Level	Guaranteed input logical-HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical-LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4 V				−400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 2.4 V				20	μA
I_I	Input HIGH Current	V_{CC} = Max, V_{IN} = 5.5 V				100	μA
I_{OZH}	Off-State Current	V_O = 2.4 V				50	μA
I_{OZL}	Off-State Current	V_O = 0.4 V				−50	μA
I_{OL}	Output Sink Current	V_{OL} = 2 V		45			mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max (Note 2)		−60	−95	−275	mA
I_{CC}	Power Supply Current	V_{CC} = Max	25°C, 5 V		230		mA
			0°C to +70°C			280	

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under Operating Range for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

KEY TO SWITCHING WAVEFORMS

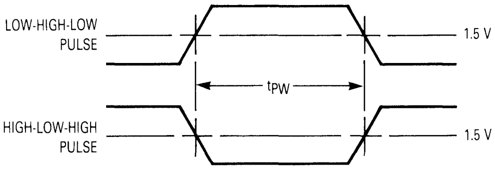
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

SWITCHING TEST WAVEFORMS



Setup, Hold, and Release Times

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched are "don't care" condition.



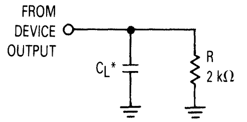
Pulse Width

GENERAL TEST NOTES

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Automatic tester hardware and handler add additional round trip A.C. delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

SWITCHING TEST CIRCUITS


FROM
DEVICE
OUTPUT
C_L*
R
2 kΩ

*t_{pd} specified at C_L = 50, 150 and 500 pF

Figure 4. Capacitive Load Switching

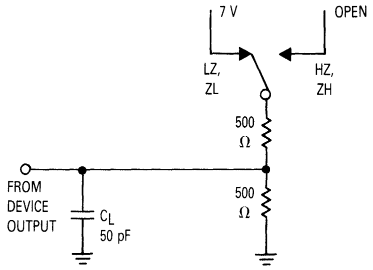

7 V
OPEN
LZ,
ZL
HZ,
ZH
500
Ω
500
Ω
FROM
DEVICE
OUTPUT
C_L
50 pF

Figure 5. Three-State Enable/Disable (for Surface-mount packages only)

SWITCHING TEST WAVEFORM (Cont'd.)

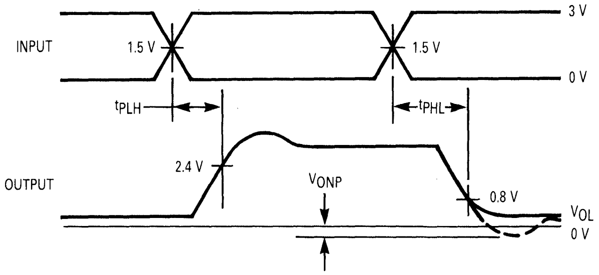
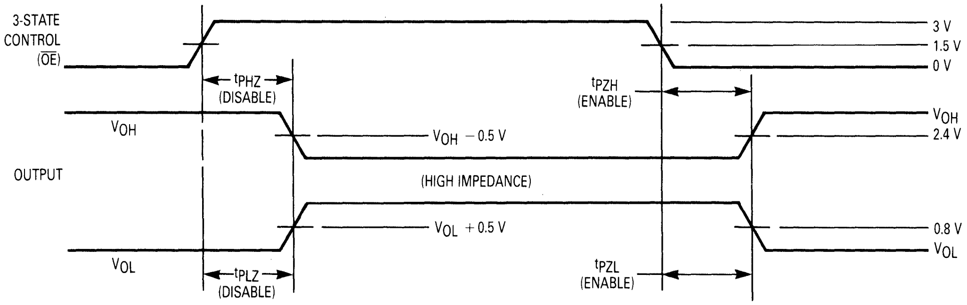

INPUT
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
OUTPUT
2.4 V
V_{ONP}
0.8 V
V_{OL}
0 V

Figure 6. Output Drivers Levels


3-STATE
CONTROL
($\overline{OE}$)
3 V
1.5 V
0 V
t_{PHZ}
(DISABLE)
t_{PZH}
(ENABLE)
V_{OH}
V_{OH} − 0.5 V
V_{OH}
2.4 V
OUTPUT
(HIGH IMPEDANCE)
V_{OL} + 0.5 V
0.8 V
V_{OL}
V_{OL}
t_{PLZ}
(DISABLE)
t_{PZL}
(ENABLE)

Note: Decoupling is needed for all AC tests

Figure 7. Three-State Control Levels (for Surface-mount packages only)

SWITCHING CHARACTERISTICS (over operating range for C_L = 150 pF)

Parameter		Description	Test Conditions	Typ	Commercial		Units
					Min	Max	
1	t_{PD}	A_i to Q_i Delay	Figures 4 and 6	12	3	20	ns
2	t_{PD}	RASI to $\overline{RAS}_i$		10	3	18	ns
3	t_{PD}	CASI to $\overline{CAS}_i$		8	3	17	ns
4	t_{PD}	MSEL to Q_i		12	3	20	ns
5	t_{PD}	MC_i to Q_i		15	5	24	ns
6	t_{PD}	LE to $\overline{RAS}_i$		15		25	ns
7	t_{PD}	LE to $\overline{CAS}_i$		14		24	ns
8	t_{PD}	MC_i to $\overline{RAS}_i$		14	3	21	ns
9	t_{PD}	MC_i to $\overline{CAS}_i$		12	3	19	ns
10	t_{PD}	LE to Q_i		15	5	25	ns
11	t_{PWL}	RASI, CASI		10	20		ns
12	t_{PWH}	RASI, CASI		10	20		ns
13	t_S	A_i to LE		1	5		ns
14	t_H	A_i to LE		1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_i		16		23	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_i$		12		20	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_i$		11		19	ns
18	t_{PD}	SEL_i to $\overline{RAS}_i$		12		20	ns
19	t_{PD}	SEL_i to $\overline{CAS}_i$		11		18	ns
20	t_S	SEL_i to LE		1	5		ns
21	t_H	SEL_i to LE		1	5		ns
22	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 10)		10		17	ns
23	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 00,01)		10		17	ns
24	t_{SKEW}	Q_i to $\overline{RAS}_i$		2		10	ns
25	t_{SKEW}	Q_i to $\overline{CAS}_i$		12		17	ns
26	t_H	MC_1 to RASI	C_L = 50 pF		5		ns
27	t_S	$\overline{CS}$ to RASI	C_L = 50 pF		5		ns
28	t_S	SEL_1 to RASI	C_L = 50 pF		5		ns
	t_{PLZ}	Output Disable Time From LOW, HIGH (Note 1)	Figures 5 and 7 S = 1	15		22	ns
	t_{PHZ}		S = 2	13		20	ns
	t_{PZL}	Output Enable Time From LOW, HIGH (Note 1)	Figures 5 and 7 S = 1	13		19	ns
	t_{PZH}		S = 2	14		21	ns
	V_{ONP}	Output Undershoot Voltage	Figures 4 and 6	0		−0.5	V

Note: 1. Three-state ($\overline{OE}$) applies only to surface-mount packages.

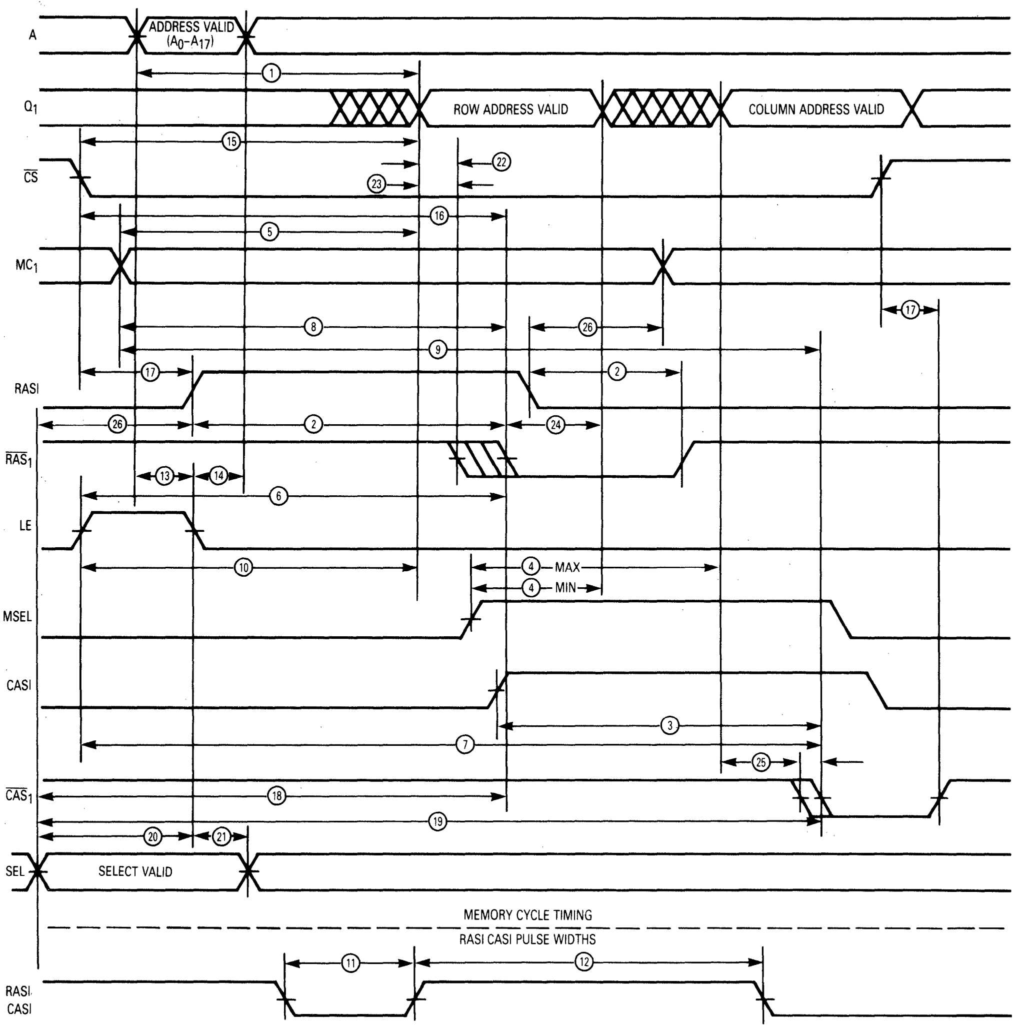
SWITCHING CHARACTERISTICS (over operating range for C_L = 500 pF)

Parameter		Description	Test Conditions	Typ	Commercial		Units
					Min	Max	
1	t_{PD}	A_i to Q_i Delay	Figures 4 and 6	16	9	24	ns
2	t_{PD}	RASI to $\overline{RAS}_i$		15	9	23	ns
3	t_{PD}	CASI to $\overline{CAS}_i$		14	9	22	ns
4	t_{PD}	MSEL to Q_i		17	9	26	ns
5	t_{PD}	MC_i to Q_i		18	10	28	ns
6	t_{PD}	LE to $\overline{RAS}_i$		20		28	ns
7	t_{PD}	LE to $\overline{CAS}_i$		19		27	ns
8	t_{PD}	MC_i to $\overline{RAS}_i$		19	9	25	ns
9	t_{PD}	MC_i to $\overline{CAS}_i$		17	9	23	ns
10	t_{PD}	LE to Q_i		20	10	27	ns
11	t_{PWL}	RASI, CASI		10	20		ns
12	t_{PWH}	RASI, CASI		10	20		ns
13	t_S	A_i to LE		1	5		ns
14	t_H	A_i to LE		1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_i		19		27	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_i$		14		22	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_i$		14		22	ns
18	t_{PD}	SEL_i to $\overline{RAS}_i$		15		23	ns
19	t_{PD}	SEL_i to $\overline{CAS}_i$		14		22	ns
20	t_S	SEL_i to LE		1	5		ns
21	t_H	SEL_i to LE		1	5		ns
22	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 10)		10		15	ns
23	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 00,01)		10		17	ns
24	t_{SKEW}	Q_i to $\overline{RAS}_i$		2		8	ns
25	t_{SKEW}	Q_i to $\overline{CAS}_i$		15		17	ns
26	t_H	MC_1 to RASI	C_L = 150 pF		5		ns
27	t_S	$\overline{CS}$ to RASI	C_L = 150 pF		5		ns
28	t_S	SEL_1 to RASI	C_L = 150 pF		5		ns
	V_{ONP}	Output Undershoot Voltage		0		−0.5	V

SWITCHING CHARACTERISTICS (over operating range for C_L = 500 pF)

Parameter		Description	Test Conditions	Typ	Commercial		Units
					Min	Max	
1	t_{PD}	A_i to Q_i Delay	Figures 4 and 6	29	12	40	ns
2	t_{PD}	RASI to $\overline{RAS}_i$		28	12	40	ns
3	t_{PD}	CASI to $\overline{CAS}_i$		26	12	37	ns
4	t_{PD}	MSEL to Q_i		29	12	42	ns
5	t_{PD}	MC_i to Q_i		30	12	44	ns
6	t_{PD}	LE to $\overline{RAS}_i$		32		46	ns
7	t_{PD}	LE to $\overline{CAS}_i$		31		45	ns
8	t_{PD}	MC_i to $\overline{RAS}_i$		30	12	40	ns
9	t_{PD}	MC_i to $\overline{CAS}_i$		28	12	40	ns
10	t_{PD}	LE to Q_i		32	12	46	ns
11	t_{PWL}	RASI, CASI		10	20		ns
12	t_{PWH}	RASI, CASI		10	20		ns
13	t_S	A_i to LE		1	5		ns
14	t_H	A_i to LE		1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_i		30		45	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_i$		27		40	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_i$		26		38	ns
18	t_{PD}	SEL_i to $\overline{RAS}_i$		31		42	ns
19	t_{PD}	SEL_i to $\overline{CAS}_i$		28		41	ns
20	t_S	SEL_i to LE		1	5		ns
21	t_H	SEL_i to LE		1	5		ns
22	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 10)		10		18	ns
23	t_{SKEW}	Q_i to $\overline{RAS}_i$ (MC_i = 00,01)		10		18	ns
24	t_{SKEW}	Q_i to $\overline{RAS}_i$		2		8	ns
25	t_{SKEW}	Q_i to $\overline{CAS}_i$		15		20	ns
26	t_H	MC_1 to RASI	C_L = 500 pF		5		ns
27	t_S	$\overline{CS}$ to RASI	C_L = 500 pF		5		ns
28	t_S	SEL_1 to RASI	C_L = 500 pF		5		ns
	V_{ONP}	Output Undershoot Voltage		0		−0.5	V

SWITCHING WAVEFORMS


A
ADDRESS VALID (A0–A17)
Q1
ROW ADDRESS VALID
COLUMN ADDRESS VALID
CS
MC1
RASI
RAS1
LE
MSEL
CASI
CAS1
SEL
SELECT VALID
MEMORY CYCLE TIMING
RASI CASI PULSE WIDTHS
RASI
CASI
①
⑮
㉒
㉓
⑯
⑤
⑰
⑧
㉖
⑨
②
㉔
⑬
⑭
⑥
⑩
④ MAX
④ MIN
③
⑦
㉕
⑱
⑲
⑳
㉑
⑪
⑫

F2968A Dynamic Memory Controller Timing

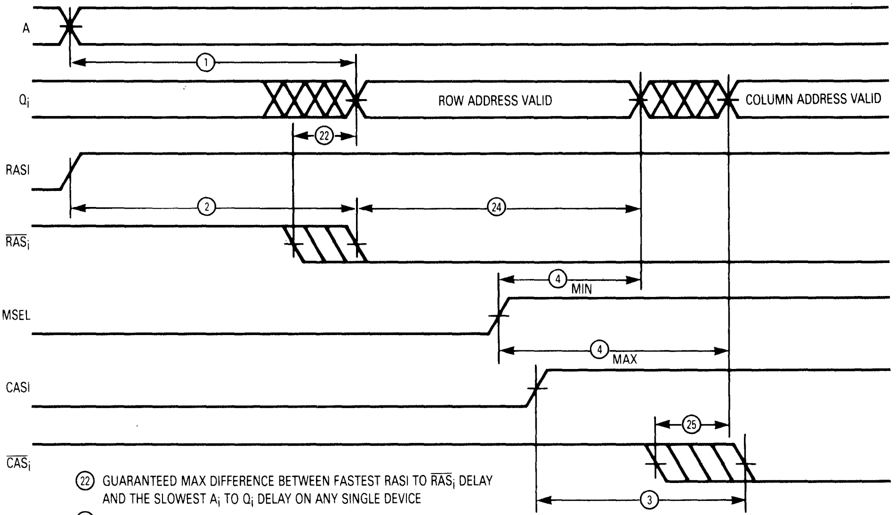
MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 8. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

The minimum requirement for T_1, T_2 and T_3 are as follows:

T_1 Min = $t_{ASR} + t_{22}$
T_2 Min = $t_{RAH} + t_{24}$
T_3 Min = $T_2 + t_{25} + t_{ASC}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.

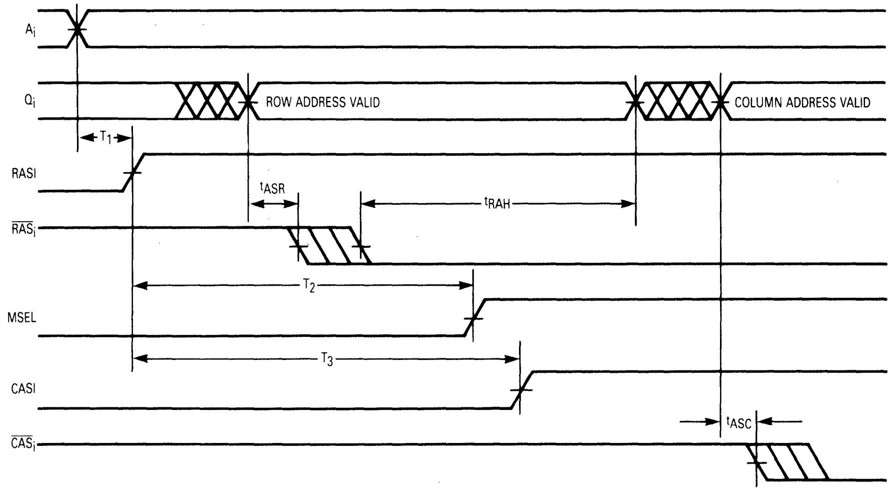

A
Qi
RASI
$\overline{RAS_i}$
MSEL
CASI
$\overline{CAS_i}$
①
㉒
②
㉔
④ MIN
④ MAX
㉕
③
ROW ADDRESS VALID
COLUMN ADDRESS VALID

㉒ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS_i}$ DELAY AND THE SLOWEST A_i TO Q_i DELAY ON ANY SINGLE DEVICE

㉔ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST MSEL TO Q_i DELAY AND THE SLOWEST RASI TO RAS_i DELAY ON ANY SINGLE DEVICE

㉕ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST CASI TO $\overline{CAS_i}$ DELAY AND THE SLOWEST MSEL TO Q_i DELAY ON ANY SINGLE DEVICE

Figure 8. Memory Cycle Timing
a. Specifications Applicable to Memory Cycle Timing (MC_i = 1, 0)


A_i
Q_i
RASI
$\overline{RAS_i}$
MSEL
CASI
$\overline{CAS_i}$
T_1
t_{ASR}
t_{RAH}
T_2
T_3
t_{ASC}
ROW ADDRESS VALID
COLUMN ADDRESS VALID

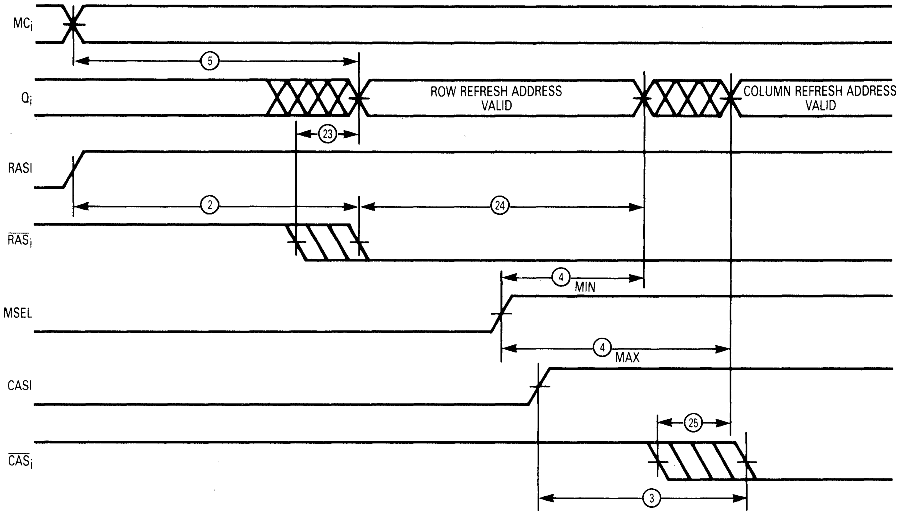
b. Desired System Timing

REFRESH CYCLE TIMING

The timing relationships for refresh are shown in Figure 9.

T_4 minimum is calculated as follows:

$T_4 \text{ Min} = t_{ASR} + t_{23}$


MC_i
Q_i
ROW REFRESH ADDRESS VALID
COLUMN REFRESH ADDRESS VALID
RASI
$\overline{RAS}_i$
MSEL
CASI
$\overline{CAS}_i$
⑤
㉓
②
㉔
④ MIN
④ MAX
㉕
③

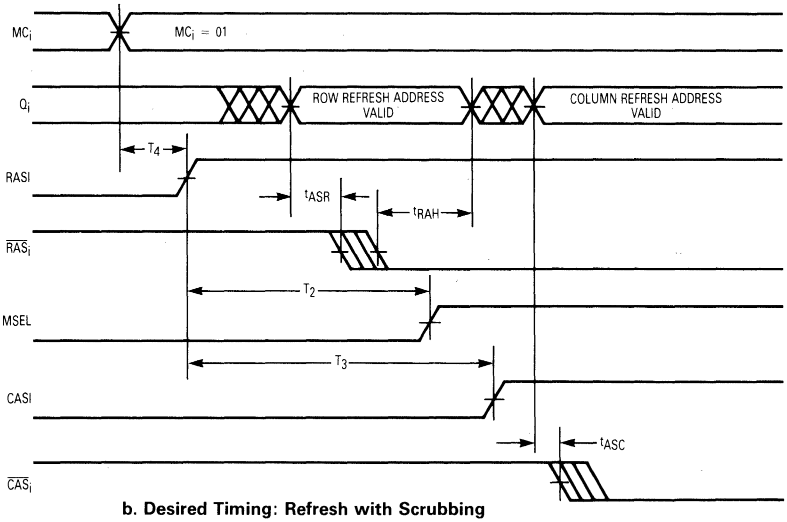
㉒ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_i$ DELAY AND THE SLOWEST A_i TO Q_i DELAY ON ANY SINGLE DEVICE

㉓ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_i$ DELAY AND THE SLOWEST MC_i TO Q_i DELAY ON ANY SINGLE DEVICE

㉔ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST MSEL TO Q_i DELAY AND THE SLOWEST RASI TO $\overline{RAS}_i$ DELAY ON ANY SINGLE DEVICE

㉕ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST CASI TO CAS_i DELAY AND THE SLOWEST MSEL TO Q_i DELAY ON ANY SINGLE DEVICE

Figure 9. Refresh Cycle Timing
a. Specifications Applicable to Refresh Cycle Timing (MC_i = 00, 01)


MC_i
MC_i = 01
Q_i
ROW REFRESH ADDRESS VALID
COLUMN REFRESH ADDRESS VALID
T_4
RASI
t_ASR
t_RAH
$\overline{RAS}_i$
T_2
MSEL
T_3
CASI
t_ASC
$\overline{CAS}_i$

b. Desired Timing: Refresh with Scrubbing

REFRESH CYCLE TIMING

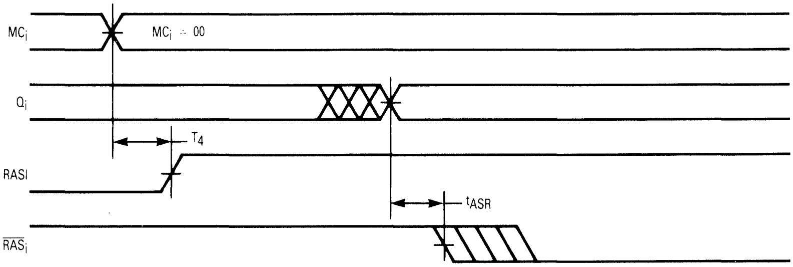
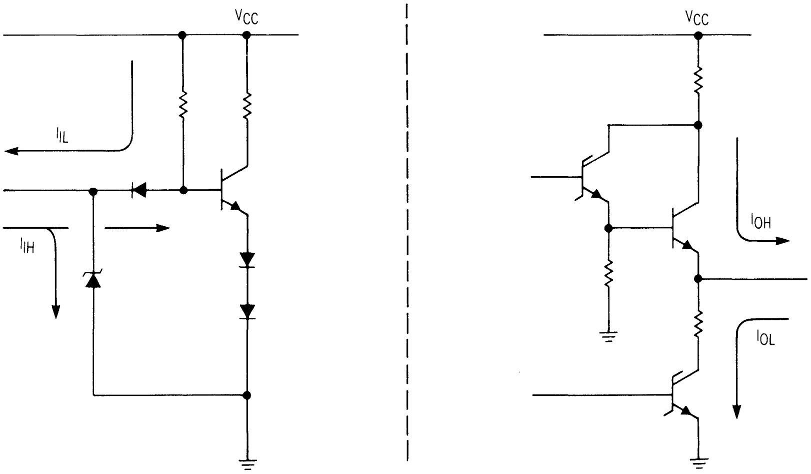

MC_i
$MC_i = 00$
Q_i
T_4
RASI
t_{ASR}
$\overline{RAS_i}$

Figure 9. Refresh Cycle Timing (Cont'd.)
c. Desired Timing: Refresh without Scrubbing

INPUT/OUTPUT CURRENT DIAGRAM


Driven Input

Driving Output

V_{CC}
I_{IL}
I_{IH}
V_{CC}
I_{OH}
I_{OL}

MOTOROLA

MC74F2970/
Am2970

MEMORY TIMING CONTROLLER

Advance Information

MEMORY TIMING CONTROLLER

The MC74F2970 will be dual marked with the AMD part number Am2970 to indicate plug-in compatibility. Dual marking will also apply to the MC74F2968A referred to in this data sheet. Both devices will be referred to as MC74F2970 and MC74F2968A in the remainder of this specification.

DESCRIPTION — The MC74F2970 is a high performance Memory Timing Controller (MTC). The MC74F2970 is designed to be used in memory systems which use the MC74F2968A Dynamic Memory Controller (DMC). All control signals needed by the DMC are generated by the MC74F2970 MTC.

The MC74F2970 uses a delay line to provide maximum flexibility to the memory system designer, allowing achievement of maximum performance. The delay line is the timing reference from which the MTC generates the control signals.

The MC74F2970 provides an internal refresh interval timer to generate refresh requests independent of the CPU. This guarantees proper refresh timing under all combinations of CPU and DMA requests.

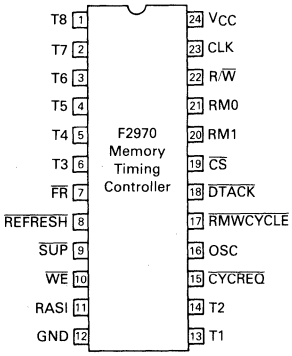
The MC74F2970 will be supplied in 24-lead, 300 mil plastic and ceramic DIP packages as well as 28-lead PLCC packages.

The MC74F2970:

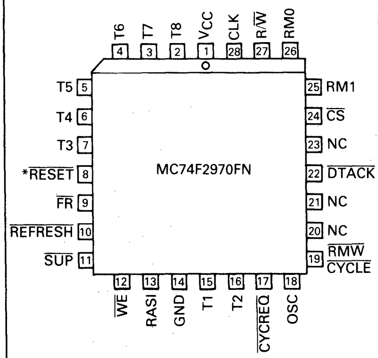
- Provides complete timing control for 64K/256K DRAM memory systems in configurations up to 1 Megaword by 16 bits utilizing the MC74F2968A DMC.
- Supports extended cycle timing needed for byte-write operations
- Internal or external control of refresh
- Burst (up to 512 cycle), distributed, or hidden refresh
- Memory access/refresh request arbitration

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CONNECTION DIAGRAMS
Top View


T8 1
T7 2
T6 3
T5 4
T4 5
T3 6
FR 7
REFRESH 8
SUP 9
WE 10
RASI 11
GND 12
F2970
Memory
Timing
Controller
24 VCC
23 CLK
22 R/W
21 RM0
20 RM1
19 CS
18 DTACK
17 RMWCYCLE
16 OSC
15 CYCREQ
14 T2
13 T1

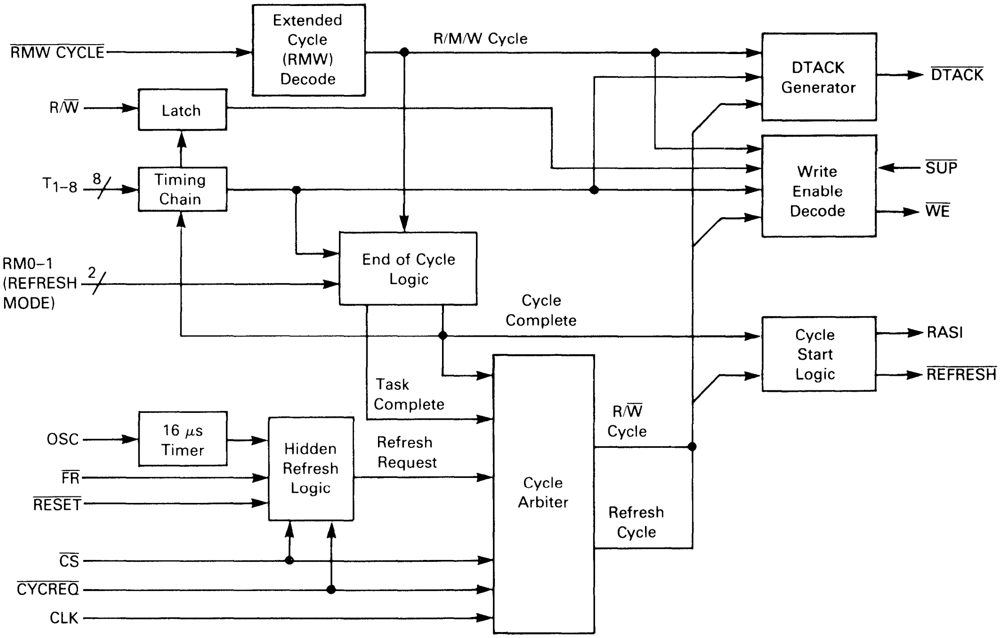
N Suffix — Case 724-02 (Plastic)
J Suffix — Case 758-01 (Ceramic)


T6 4
T7 3
T8 2
VCC 1
CLK 28
R/W 27
RM0 26
T5 5
T4 6
T3 7
*RESET 8
FR 9
REFRESH 10
SUP 11
MC74F2970FN
25 RM1
24 CS
23 NC
22 DTACK
21 NC
20 NC
19 RMW CYCLE
12 WE
13 RASI
14 GND
15 T1
16 T2
17 CYCREQ
18 OSC

FN Suffix — Case 776-02 (PLCC)

*RESET input available only in PLCC

F2970 DYNAMIC MEMORY TIMING CONTROLLER BLOCK DIAGRAM


$\overline{\text{RMW CYCLE}}$
Extended Cycle (RMW) Decode
R/M/W Cycle
DTACK Generator
$\overline{\text{DTACK}}$
R/$\overline{\text{W}}$
Latch
T_{1-8}
8
Timing Chain
Write Enable Decode
$\overline{\text{SUP}}$
$\overline{\text{WE}}$
RM0–1 (REFRESH MODE)
2
End of Cycle Logic
Cycle Complete
Cycle Start Logic
RASI
$\overline{\text{REFRESH}}$
Task Complete
R/$\overline{\text{W}}$ Cycle
OSC
16 μs Timer
Hidden Refresh Logic
Refresh Request
$\overline{\text{FR}}$
$\overline{\text{RESET}}$
Cycle Arbiter
Refresh Cycle
$\overline{\text{CS}}$
$\overline{\text{CYCREQ}}$
CLK

PIN DESCRIPTION

Name	I/O	Description
$\overline{\text{CS}}$	I	When $\overline{\text{CHIP SELECT}}$ is low, it indicates that the bank/board controlled by the F2970 is selected and enabled. A memory read/write cycle can only be performed when $\overline{\text{CS}}$ is active, while refresh cycles are independent of $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is HIGH, all memory requests (HIGH-to-LOW transition of $\overline{\text{CYCREQ}}$) will be interpreted as 'Hidden Refresh' requests.
$\overline{\text{CYCREQ}}$	I	When $\overline{\text{CS}}$ is LOW, this input will generate an internal memory request for the F2970 on the HIGH-to-LOW transition of $\overline{\text{CYCREQ}}$.
$\overline{\text{DTACK}}$	O	The HIGH-to-LOW transition of $\overline{\text{DTACK}}$ informs the CPU that a write cycle has begun, or that valid data will be on the system bus at the correct time during a read cycle.
$\overline{\text{FR}}$	I	This input is used to force a refresh cycle at user-designated times. The falling edge of $\overline{\text{FR}}$ latches an internal refresh request. If the memory is busy, the refresh is done at the completion of the current cycle.
$\overline{\text{REFRESH}}$	O	This output, when low, indicates that a refresh cycle will be performed. It should be connected to the MC1 input of the F2968A Dynamic Memory Controller. The MC0 input of the DMC should be tied low.
OSC	I	This input, when connected to an external R/C circuit is used to generate an internal refresh clock. If $\overline{\text{FR}}$ is not active, the oscillator will initiate the refresh cycles.
RM0, RM1	I	The REFRESH MODE inputs control the type of refresh cycle the F2970 will perform, as described in Table 1.
CLK	I	For systems requiring synchronous arbitration of memory access and refresh requests, this input would receive the system clock. For asynchronous arbitration, this input must be tied high.
RASI	O	The ROW ADDRESS STROBE drives the delay line and the RASI input of the DMC. The rising edge initiates a memory access for the DMC and starts the timing reference.
R/$\overline{\text{W}}$	I	This input indicates a memory read request when HIGH, and a write request when LOW.

PIN DESCRIPTION

Name	I/O	Description
SUP	I	When SUPPRESS is driven LOW, it inhibits access to memory by disabling WE. It can be used to prevent illegal access in memory-access protected systems.
WE	O	WRITE ENABLE, when LOW, causes data to be written to memory. WE is inhibited if SUP is LOW. This output can drive a 500 pF load.
RMWCYCLE	I	This input, when LOW, indicates that the current cycle is a read-modify-write cycle. The F2970 will adjust the necessary timing for an extended cycle. This input is not latched and must be valid for the entire memory cycle, given that it meets the set-up time with respect to the first timing tap that is driven by the delay-line.
T1–T8	I	These inputs are the positive-edge triggered timing tap outputs from the timing reference (delay-line). They provide the necessary timing information for the F2970 to control memory cycles. The definition of the eight timing taps is given in Table 2.
RESET	I	This input is provided only in the PLCC package. It is intended to be connected to the RESET signal of the processor, so that the F2970 is reset during the system initialization sequence when RESET is LOW. The functioning of the different modes of operation is not affected when RESET is HIGH.

ARCHITECTURE

The MC74F2970 Memory Timing Controller replaces much of the MSI "glue" logic which is commonly necessary in controlling dynamic memory systems. It is responsible for controlling/arbitrating memory access, refresh, and hand shaking with the processor. The MTC also provides an extended (Read-Modify-Write) cycle which is needed for byte operations.

These tasks are performed by the following functions in the block diagram.

Memory Access Control:
Cycle Arbiter
Cycle Start Logic
Timing Chain Logic
WE Decode
End of Cycle Logic

Refresh Support:
Refresh Timer
Hidden Refresh Logic

Processor Interface:
DTACK Logic

CYCLE ARBITER

This circuitry determines whether a refresh or a read/write cycle is to be performed. If a refresh and read/write cycle are requested at the same time, the read/write cycle is performed first followed by the refresh cycle.

The arbiter can be synchronous through the use of the CLK input. In this mode, the CYCREQ and refresh inputs are examined on the negative edge of the CLK input.

The arbiter can also function asynchronously (with the CLK input tied HIGH). In this mode, the first memory request to occur will be serviced, but not until after an internal delay to avoid metastable states.

CYCLE START LOGIC

This block decodes the internal state of the F2970 and initiates a memory cycle by asserting RASI. Before the memory cycle is started, this block indicates which type of access the F2968A Dynamic Memory Controller will perform via the REFRESH output.

TIMING CHAIN LOGIC

Since timing information is only contained in the positive edge of the Timing tap inputs, (an output is asserted on the positive edge of Tx and negated on the positive edge of Ty) this block conditions these inputs into usable signals for the various decode blocks.

It is possible to have 2 positive transitions on some timing inputs during an extended cycle preceded by a normal cycle. To facilitate design, the F2970 will only recognize the following sequence of positive transitions on the extended cycle timing inputs:

T4: WE asserted
T7: Reset of RASI
T8: End of extended cycle

For example, a positive edge of T8 before a positive edge on T4 will be ignored.

WE DECODE (OR WRITE ENABLE DECODE)

This block decodes the internal states of the F2970 and asserts WE on T3 for write cycles or T4 for read-modify-write cycles. WE is forced HIGH if SUP is LOW.

END OF CYCLE LOGIC

This block determines when a memory cycle or memory task is complete. A memory cycle will end on the positive edge of T6 or T8, depending on whether a normal or extended (read-modify-write) cycle is being executed. Normally, a memory task consists of a single memory access. However, this block also contains counter logic to keep track of multiple access tasks such as burst refreshes.

REFRESH TIMER

This block provides an on-chip refresh interval timer whose frequency is determined by an external RC network. If the refresh clock is provided via the FR input, the internal oscillator may be disabled by connecting the OSC pin to ground.

HIDDEN REFRESH LOGIC

This block determines the source of the internal refresh clock which could be either the FR input, or the output of the internal oscillator. In addition, this block will also assert "hidden refresh" requests under certain conditions.

A complete description of the refresh modes is covered under System Considerations.

DTACK LOGIC

This logic decodes the type of memory access and asserts DATA TRANSFER ACKNOWLEDGE (DTACK) at the appropriate time. DTACK is asserted on T1 for normal read/write cycles and on T2 for read-modify-write cycles. DTACK is negated when CYCREQ is taken HIGH.

SYSTEMS CONSIDERATIONS

The F2970 allows maximum performance and flexibility for dynamic memory systems. It receives and arbitrates memory access requests, initiates the read/write cycles and handshakes with the processor.

The MTC performs four types of memory cycles — read, write, refresh and read-modify-write. The timing of these cycles is shown in Figures 3 through 10.

Other types of memory access such as Nibble Mode, Page Mode and Static Column are possible by adding additional "glue" logic.

SYNCHRONOUS versus ASYNCHRONOUS ARBITRATION

The F2970 arbitrates between processor (read/write) and refresh requests for a memory cycle. Synchronous arbitration requires that the inputs requiring memory, FR and CYCREQ, be clocked into the F2970. In many applications, the phase relationship of the system block to the FR and CYCREQ inputs may change to the point where setup and hold time requirements cannot be guaranteed. In these instances, asynchronous arbitration (CLK tied HIGH) can be used. Timing for synchronous and asynchronous arbitration can be found in Figures 3 and 4.

REFRESH OPERATIONS

The MTC can support a variety of refresh schemes. The type of refresh is controlled via the RM0, RM1 and FR inputs. Basic refresh types include distributed, or a 128, 256, or 512 cycle burst. It has to be noted that any burst refresh request will be ignored while the F2970 is servicing consecutive processor requests.

The internal refresh clock is equivalent to the FR input, or the output of the internal oscillator as follows:

- In the burst mode of operation, the FR input is always the refresh clock.
- The FR input can also be used as the refresh clock in the distributed refresh (non-burst) mode. However, the internal oscillator takes over as the refresh clock if it goes through three cycles without a LOW level appearing on the FR input. This provision allows the primary refresh clock (FR) to be interrupted while it is in the HIGH logic state, and for refresh operations to be resumed at the internal oscillator frequency.
- It is also possible to use the on-chip oscillator as the refresh clock in the distributed refresh mode. In this case, the FR input should be tied HIGH. However, since the on-chip oscillator is asynchronous to the external CLK input, it is necessary to provide a synchronous refresh clock via the FR input if synchronous arbitration is desired.

The F2970 has the ability to increase memory bandwidth by inserting refresh requests when the processor is accessing other devices or I/O (CYCREQ = LOW, CS = HIGH). A hidden refresh can only be performed once every refresh clock period, and occurs only with distributed refreshing. When a hidden refresh is performed, the F2970 will skip the next refresh request. (See Figure 1.)

Depending on the system configuration and operation, it is possible for the DRAM to appear "static" providing that a hidden refresh can be performed every refresh clock period.

FIGURE 1 — HIDDEN REFRESH CYCLE

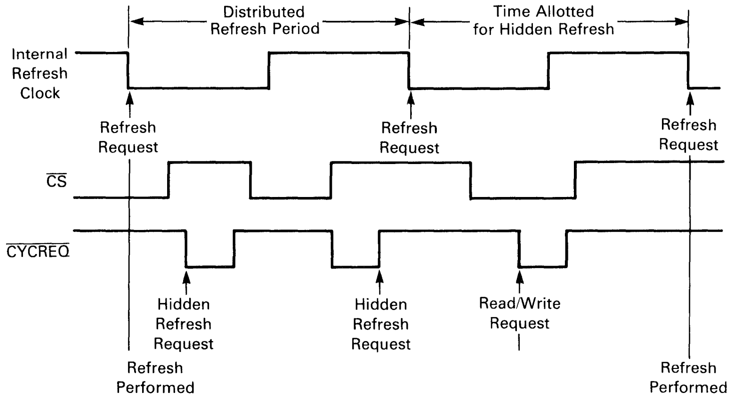


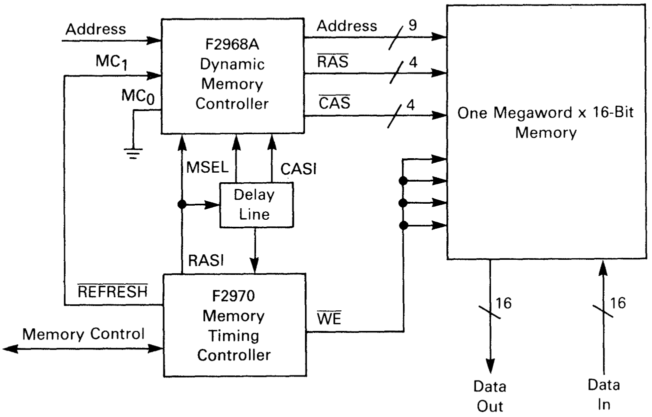
TABLE 1 — REFRESH MODES

RM1	RM0	Refresh Mode
0	0	Not Burst (Distributed)
0	1	128-Cycle Burst
1	0	256-Cycle Burst
1	1	512-Cycle Burst

TABLE 2 — TIMING TAP DEFINITION

Tap No.	Function
T1	Controls when $\overline{\text{DTACK}}$ will go active during read cycles.
T2	Controls when $\overline{\text{DTACK}}$ will go active during read-modify-write cycles.
T3	Indicates when valid data is available on the memory bus during write cycles.
T4	Indicates when valid data is available on the memory bus during read-modify-write cycles.
T5	Controls the rising edge of $\overline{\text{RAS}}$ (falling edge of RASI) on read, write and refresh cycles.
T6	Indicates that a new memory cycle may begin after a read, write or refresh cycle. (T5 + trp)
T7	Controls the rising edge of $\overline{\text{RAS}}$ (falling edge of RASI) on read-modify-write cycles.
T8	Indicates that a new memory cycle may begin after a read-modify-write cycle. (T7 + trp)

FIGURE 2 — ONE MEGAWORD DYNAMIC MEMORY SYSTEM


Address
MC1
MC0
F2968A Dynamic Memory Controller
Address
9
RAS
4
CAS
4
One Megaword x 16-Bit Memory
MSEL
CASI
Delay Line
RASI
REFRESH
F2970 Memory Timing Controller
WE
Memory Control
16
16
Data Out
Data In

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (Except OSC)	V_{in}	−0.5 to +5.5	V
Output Voltage $\overline{\text{DTACK}}$	V_{out}	−0.5 to +5.5	V
Output Voltage (all others)	V_{out}	−0.5 to V_{CC} value	V
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	140	°C

THERMAL CHARACTERISTICS

Characteristics	Package	Symbol	Value	Units
Thermal Resistance	24-Ld Plastic	θ_{JA}	50	°C/W
	24-Ld Ceramic		50	
	28-Ld PLCC		50	

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature	0	25	70	°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits		Units	Test Conditions	
			Min	Max			
V_{IH}	Input HIGH Voltage Except OSC		2.0		V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage Except OSC			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage on All Outputs Except $\overline{\text{DTACK}}$		2.4		V	V_{CC} = MIN, I_{OH} = −1.0 mA	
V_{OL}	Output LOW Voltage	$\overline{\text{WE}}$		0.5	V	V_{CC} = MIN	I_{OL} = 2.4 mA
				0.8			I_{OL} = 12 mA
		Others		0.5	V		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	$\overline{\text{SUP}}$, $\overline{\text{CS}}$		40	μA	V_{CC} = MAX	V_{IN} = 2.7 V
		Others Except OSC		20			
		All Except OSC		100			V_{IN} = 5.5 V
I_{IL}	Input LOW Current	$\overline{\text{SUP}}$, $\overline{\text{CS}}$		−800	μA	V_{CC} = MAX	V_{IN} = 0.5 V
		Others Except OSC		−400			
I_{OS}	Output Short Circuit Current (1)		−50	−250	mA	V_{CC} = MAX	V_{OUT} = 0 V
I_{CC}	Supply Current			125	mA	V_{CC} = MAX	OSC Input LOW All Others HIGH
I_{OX}	Output HIGH Current on $\overline{\text{DTACK}}$ Output			250	μA	V_{CC} = MIN	V_{OH} = 5.5 V

(1) Not more than one output should be shorted at a time

AC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE (C_L = 50 pF unless otherwise specified)

Test No.	Symbol	Path		Ref. Fig.	System Operating Conditions	Min	Max
		From	To				
1	t_{PLH}	CLK High-to-Low	RASI	3, 5	Synchronous Read/Write Cycles		23
2		$\overline{\text{CYCREQ}}$ High-to-Low		6	Asynchronous Read/Write Cycles		30
3		T6 Low-to-High		3	Async. Back-to-Back Cycles ($\overline{\text{RMWCYCLE}}$ = 1)		46
4		T8 Low-to-High		3	Async. Back-to-Back Cycles ($\overline{\text{RMWCYCLE}}$ = 0)		50
5	t_{PHL}	T5 Low-to-High	RASI	3	All modes ($\overline{\text{RMWCYCLE}}$ = 1)		21
6		T7 Low-to-High		3	All modes ($\overline{\text{RMWCYCLE}}$ = 0)		23
7	t_{SKEW}	$\overline{\text{REFRESH}}$ High-to-Low	RASI Low-to-High	3, 7	All Refresh Cycles	18	
8		$\overline{\text{REFRESH}}$ Low-to-High	RASI High-to-Low	3, 7	All Refresh Cycles	5	
9	t_{PHL}	T1 Low-to-High	$\overline{\text{DTACK}}$	5, 6	Read/Write Cycles ($\overline{\text{RMWCYCLE}}$ = 1)		16
10		T2 Low-to-High		5, 6	Read/Write Cycles ($\overline{\text{RMWCYCLE}}$ = 0)		16
11	t_{PLH}	$\overline{\text{CYCREQ}}$ Low-to-High	$\overline{\text{DTACK}}$	5, 6	Read/Write Cycles		31

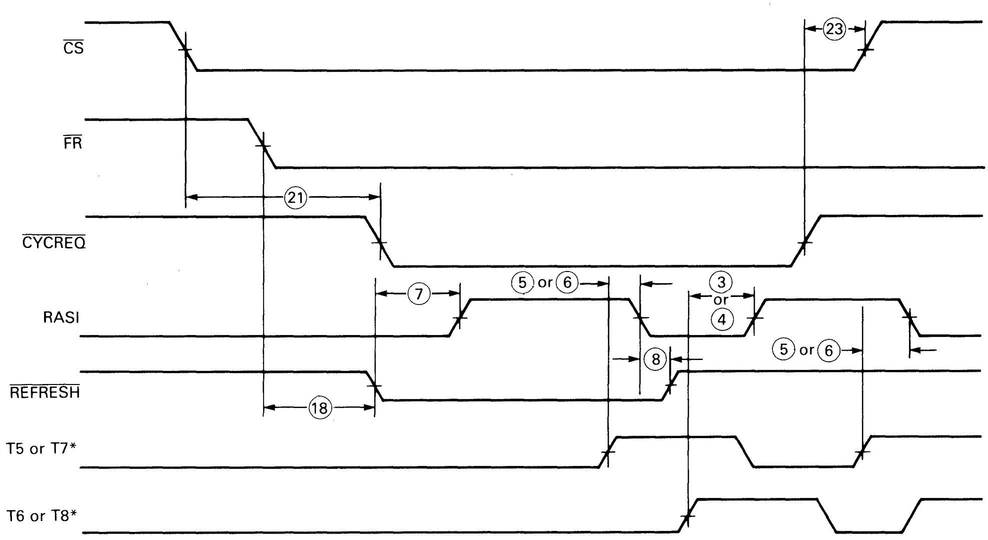
AC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE — continued (C_L = 50 pF unless otherwise specified)

Test No.	Symbol	Path		Ref. Fig.	System Operating Conditions		Min	Max
		From	To					
12	t_{PHL}	T3 Low-to-High	$\overline{WE}$	5, 6	Write Cycle	C_L = 50 pF		13
					$\overline{RMWCYCLE}$ = 1	C_L = 150 pF		21
						C_L = 500 pF		31
13		T4 Low-to-High		5, 8	Write Cycle	C_L = 50 pF		13
					$\overline{RMWCYCLE}$ = 0	C_L = 150 pF		21
						C_L = 500 pF		31
14	t_{PLH}	T5 Low-to-High	$\overline{WE}$	5, 6	Write Cycle	C_L = 50 pF		24
					$\overline{RMWCYCLE}$ = 1	C_L = 150 pF		30
						C_L = 500 pF		40
15		T7 Low-to-High		5, 8	Write Cycle	C_L = 50 pF		32
					$\overline{RMWCYCLE}$ = 0	C_L = 150 pF		38
						C_L = 500 pF		48
16	t_{PHL}	$\overline{CYCREQ}$ High-to-Low	$\overline{REFRESH}$	9	Async. Hidden Refresh Cycles			44
17		CLK High-to-Low		7	Sync. Refresh Cycles			18
18		$\overline{FR}$ High-to-Low		8	Async. Refresh Cycles			44
19		T6 Low-to-High		4	Back-to-Back Refresh Cycles ($\overline{RMWCYCLE}$ = 1)			46
20		T8 Low-to-High		4	Back-to-Back Refresh Cycles ($\overline{RMWCYCLE}$ = 0)			46
21	t_{SET}	$\overline{CS}$ High-to-Low	$\overline{CYCREQ}$ High-to-Low	5, 6	Read/Write Cycles		0	
22	t_{SET}	$\overline{CS}$ Low-to-High		9	Hidden Refresh Cycles		0	
23	t_{HOLD}	$\overline{CS}$ Low-to-High	$\overline{CYCREQ}$ Low-to-High	5, 6	Read/Write Cycles		5	
24	t_{HOLD}	$\overline{CS}$ High-to-Low	$\overline{CYCREQ}$ High-to-Low		Hidden Refresh Cycles		26	
25	t_{SET}	$\overline{CYCREQ}$ High-to-Low	CLK High-to-Low	4, 5	Read/Write Cycles		18	
26	t_{SET}				Hidden Refresh Cycles		32	
27	t_{SET}	$\overline{FR}$ High-to-Low		7	Forced Refresh Cycles		34	
28	t_{SET}	T6 Low-to-High			Back-to-Back Cycles $\overline{RMWCYCLE}$ = 1		35	
29	t_{SET}	T8 Low-to-High			Back-to-Back Cycles $\overline{RMWCYCLE}$ = 0		35	
30	t_{SET}	R/$\overline{W}$ (1 or 0)	T3 Low-to-High	5, 6	All modes		4	
31	t_{HOLD}			5, 6			10	
32	t_{SET}	$\overline{SUP}$ (1 or 0)	T3 Low-to-High	5, 6	Write Cycles $\overline{RMWCYCLE}$ = 1		5	
33	t_{SET}	$\overline{SUP}$ (1 or 0)	T4 Low-to-High	5, 8	$\overline{RMWCYCLE}$ = 0		5	
34	t_{HOLD}	$\overline{SUP}$ (1 or 0)	T5 Low-to-High	5, 8	Write Cycles $\overline{RMWCYCLE}$ = 1		22	
35	t_{HOLD}	$\overline{SUP}$ (1 or 0)	T7 Low-to-High	5, 8	$\overline{RMWCYCLE}$ = 0		28	
36	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T1 Low-to-High				21	
37	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T2 Low-to-High				16	

AC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE — continued (C_L = 50 pF unless otherwise specified)

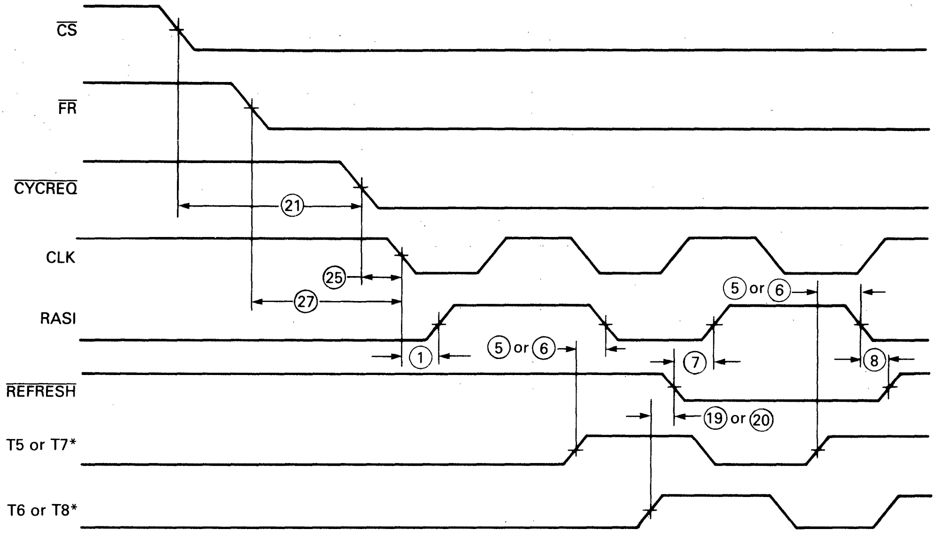
Test No.	Symbol	Path From	Path To	Ref. Fig.	System Operating Conditions	Min	Max
38	t_{SET}	$\overline{\text{RMWCYCLE}}$ (1 or 0)	T3 Low-to-High	5, 6		10	
39	t_{SET}	$\overline{\text{RMWCYCLE}}$ (1 or 0)	T4 Low-to-High	5, 6		10	
40	t_{SET}	T4 Low-to-High	T7 Low-to-High	8	$\overline{\text{RMWCYCLE}}$ = 0	15	
41	t_{SET}	T7 Low-to-High	T8 Low-to-High	8	$\overline{\text{RMWCYCLE}}$ = 0	15	
42	t_{PW}	T1–T8 High		8	All Cycles	10	
43	t_{PW}	$\overline{\text{FR}}$ High		8	Forced Refresh Cycles	15	
44	t_{PW}	CLK High or Low		5	All Synchronous Cycles	10	
45	t_{PW}	$\overline{\text{CYCREQ}}$ Low		9	Hidden Refresh Cycles	15	

FIGURE 3 — ASYNCHRONOUS ARBITRATION



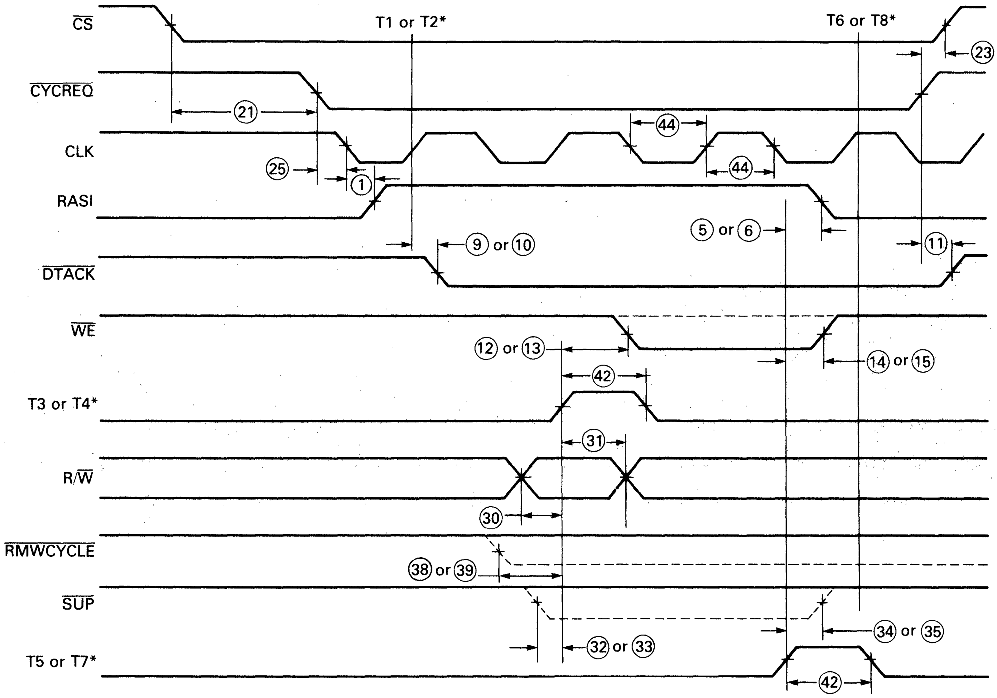
*Active when $\overline{\text{RMWCYCLE}}$ = 0

FIGURE 4 — SYNCHRONOUS ARBITRATION


CS
FR
CYCREQ
CLK
RASI
REFRESH
T5 or T7*
T6 or T8*
21
25
27
1
5 or 6
5 or 6
7
8
19 or 20

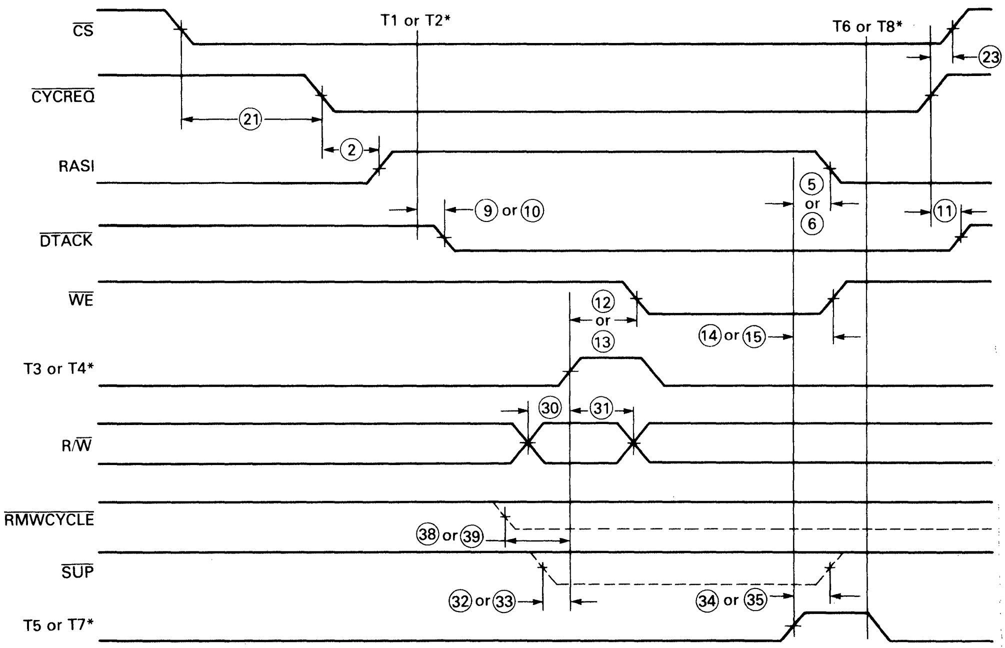
*Active when $\overline{\text{RMWCYCLE}}$ = 0

FIGURE 5 — SYNCHRONOUS READ/$\overline{\text{WRITE}}$


T1 or T2*
T6 or T8*
CS
CYCREQ
CLK
RASI
DTACK
WE
T3 or T4*
R/W
RMWCYCLE
SUP
T5 or T7*
21
25
1
23
44
44
9 or 10
5 or 6
11
12 or 13
14 or 15
42
31
30
38 or 39
32 or 33
34 or 35
42

*Active when $\overline{\text{RMWCYCLE}}$ = 0

FIGURE 6 — ASYNCHRONOUS READ/$\overline{\text{WRITE}}$


$\overline{\text{CS}}$
$\overline{\text{CYCREQ}}$
RASI
$\overline{\text{DTACK}}$
$\overline{\text{WE}}$
T3 or T4*
R/$\overline{\text{W}}$
$\overline{\text{RMWCYCLE}}$
$\overline{\text{SUP}}$
T5 or T7*
T1 or T2*
T6 or T8*
㉓
㉑
②
⑤ or ⑥
⑨ or ⑩
⑪
⑫ or ⑬
⑭ or ⑮
㉚
㉛
㊳ or ㊴
㉜ or ㉝
㉞ or ㉟

*Active when $\overline{\text{RMWCYCLE}}$ = 0

FIGURE 7 — SYNCHRONOUS FORCED REFRESH
(SHOWN WHEN $\overline{\text{RMWCYCLE}}$ = 1)

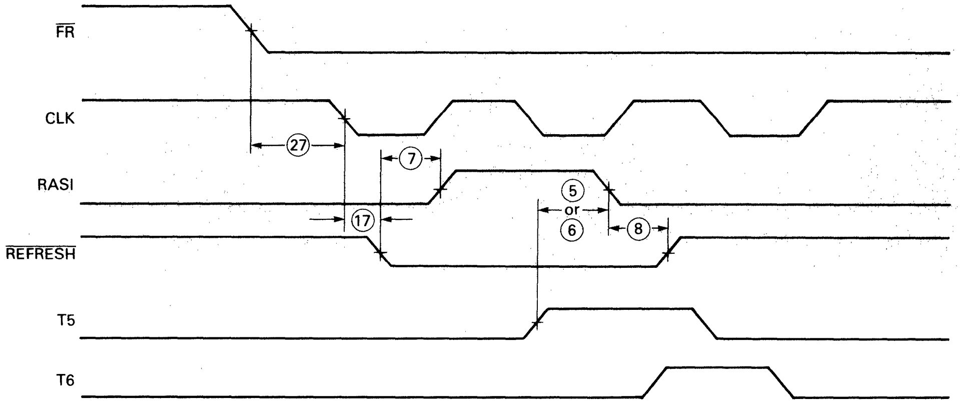

$\overline{\text{FR}}$
CLK
RASI
$\overline{\text{REFRESH}}$
T5
T6
㉗
⑦
⑰
⑤ or ⑥
⑧

FIGURE 8 — ASYNCHRONOUS FORCED REFRESH (SHOWN WHEN $\overline{\text{RMWCYCLE}}$ = 0)

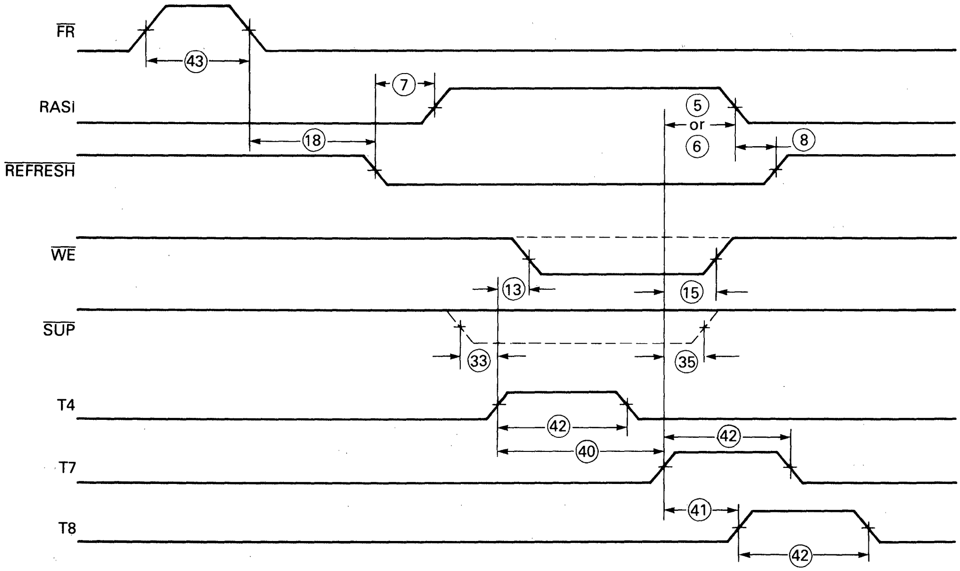
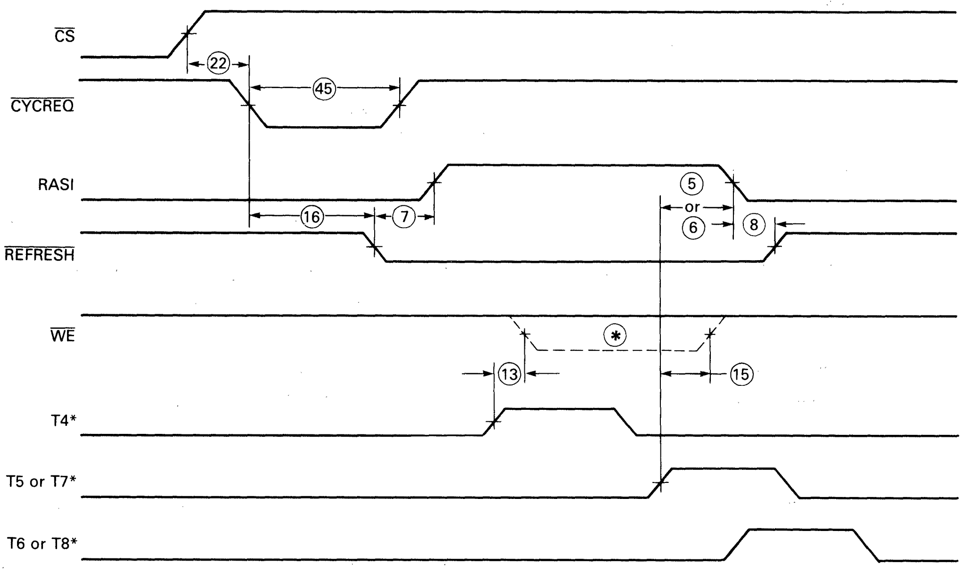
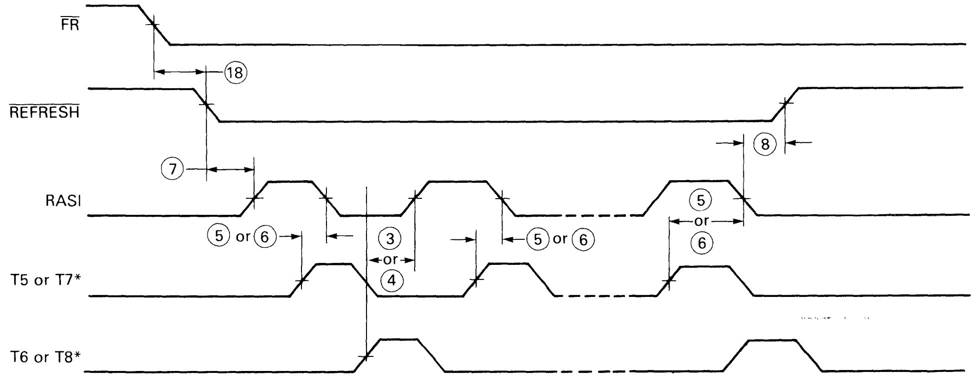

$\overline{\text{FR}}$
43
RASI
7
5
or
6
18
8
$\overline{\text{REFRESH}}$
$\overline{\text{WE}}$
13
15
$\overline{\text{SUP}}$
33
35
T4
42
42
40
T7
41
T8
42

FIGURE 9 — ASYNCHRONOUS HIDDEN REFRESH (SHOWN WHEN $\overline{\text{SUP}}$ = 1)


$\overline{\text{CS}}$
22
$\overline{\text{CYCREQ}}$
45
RASI
5
or
6
16
7
8
$\overline{\text{REFRESH}}$
$\overline{\text{WE}}$
✱
13
15
T4*
T5 or T7*
T6 or T8*

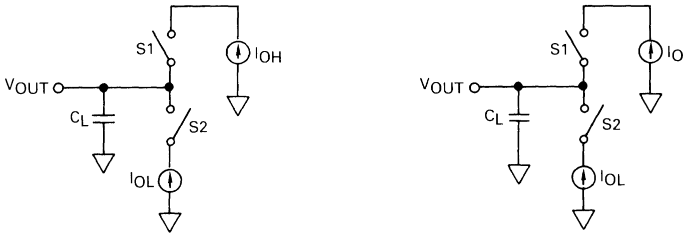
*Active when $\overline{\text{RMWCYCLE}}$ = 0

FIGURE 10 — ASYNCHRONOUS BURST REFRESH


$\overline{\text{FR}}$
18
$\overline{\text{REFRESH}}$
8
7
RASI
5
or
6
5 or 6
3
or
4
5 or 6
T5 or T7*
T6 or T8*

*Active when $\overline{\text{RMWCYCLE}}$ = 0

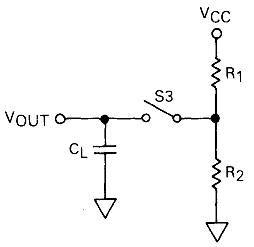
SWITCHING TEST CIRCUITS


S1
I_{OH}
V_{OUT}
C_L
S2
I_{OL}
S1
I_{OH}
V_{OUT}
C_L
S2
I_{OL}

A. RASI & $\overline{\text{REFRESH}}$ Outputs

B. $\overline{\text{WE}}$ Output

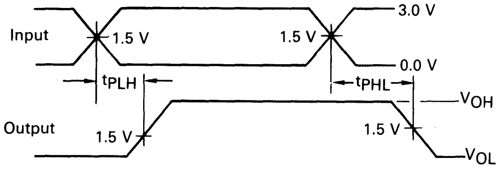
TEST OUTPUT LOADS					
Test Circuit	**R_1 (ohm)**	**R_2 (ohm)**	**C_L (pF)**	**I_{OH} (mA)**	**I_{OL} (mA)**
A			50	−1.0	8.0
B			50, 150, 500	−1.0	12
C	680	1600	50		


V_{CC}
R_1
S3
V_{OUT}
C_L
R_2

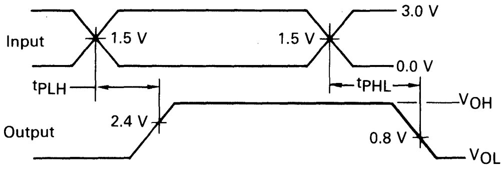
C. $\overline{\text{DTACK}}$ Output (Open Collector)

Notes: 1. C_L, the load capacitance, includes scope, probe, wiring, and stray capacitance without the device in the test fixture.
2. S_1, S_2, and S_3 are open during all dc and functional testing.
3. During ac testing, switches are set as follows:
1) S_3 is closed
2) For $V_{OUT} > 1.5$ V, S_1 is closed and S_2 open
3) For $V_{OUT} < 1.5$ V, S_1 is open and S_2 closed
4. $\overline{\text{DTACK}}$ Load:
V_{CC} = 4.5, 5.0, and 5.5 V
R_1 is selected to give I_{OL} (Max) with V_{CC} = 5.5 V
R_2 is selected to give V_{OUT} (dc) = 0.7 V_{CC} when the output $\overline{\text{DTACK}}$ is off

SWITCHING TEST WAVEFORMS

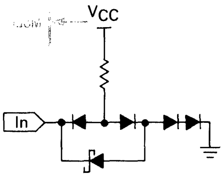

Input
1.5 V
1.5 V
3.0 V
0.0 V
tPLH
tPHL
VOH
Output
1.5 V
1.5 V
VOL

RASI, $\overline{\text{REFRESH}}$, and $\overline{\text{DTACK}}$ Outputs

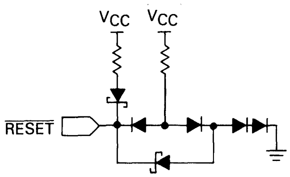

Input
1.5 V
1.5 V
3.0 V
0.0 V
tPLH
tPHL
VOH
Output
2.4 V
0.8 V
VOL

$\overline{\text{WE}}$ Output

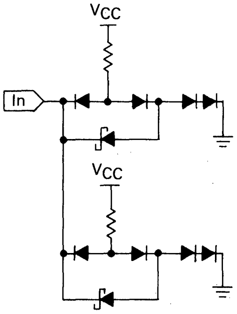
INPUT/OUTPUT CURRENT INTERFACE DIAGRAMS



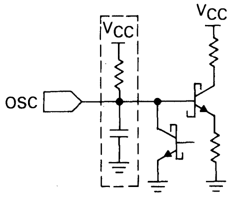
Typical Input


VCC
VCC
RESET

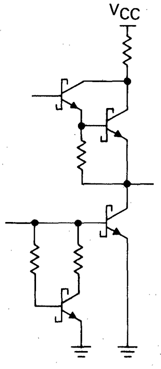
$\overline{\text{RESET}}$ Input



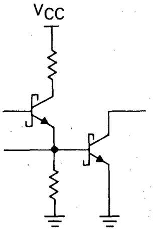
T_1, T_2, R/W, SUP, CS Inputs



OSC Input



Typical Output



$\overline{\text{DTACK}}$ Output

Product Preview

1 Megabit Dynamic Memory Controller (DMC)

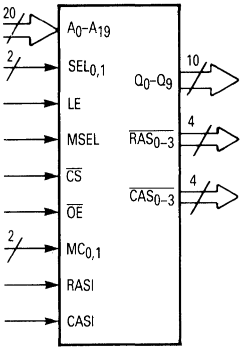
MC74F29368

The MC74F29368 Dynamic Memory Controller (DMC) is designed to be an integral part of today's high performance memory systems. The DMC functions as the address controller between any processor and Dynamic memory array. Using its two 10-bit address latches, the DMC holds the Row and Column addresses for any DRAM up to 1 megabit. These latches and the two 10-bit Row/Column Refresh address counters feed into a 10-bit, 4-input MUX, for output to the Dynamic RAM address lines. Each of the four $\overline{RAS}_n$ and $\overline{CAS}_n$ outputs is selected by the outputs of the Bank Select latch, which is driven by the two high-order address bits.

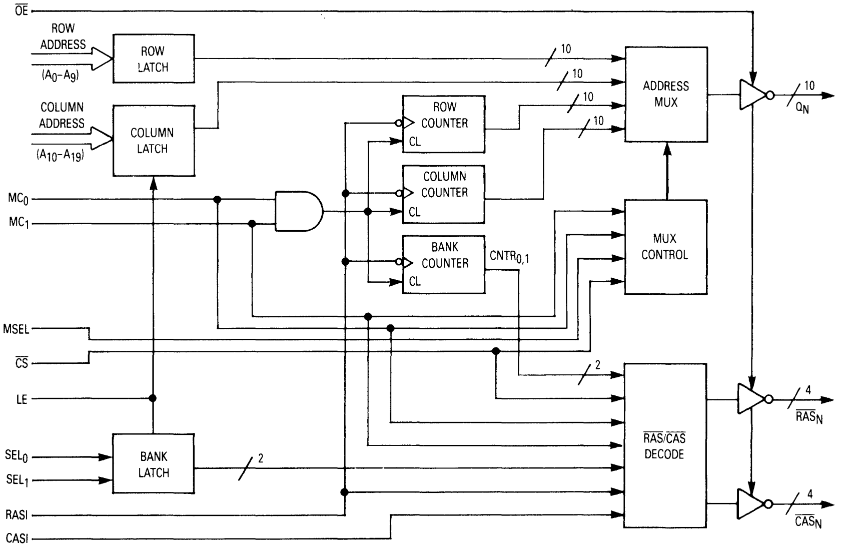
The MC74F29368 has two basic modes of operation, read/write and refresh. In the refresh mode, the Row and Column counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the Row counter is used, generating up to 1024 addresses to refresh a 1024-cycle-refresh 1-Mbit DRAM. When memory scrubbing is being performed, both the Row and Column counters are utilized to perform read-modify-write cycles. In this mode, all $\overline{RAS}_n$ outputs will be active, while only $\overline{CAS}_n$ output is active at a time.

- Provides Control for 16K, 64K, and 256K and 1-Megabit Dynamic RAMs
- Outputs Directly Drive up to 88 DRAMs, with a Guaranteed Worst-Case Limit on the Undershoot
- Highest-Order Two Address Bits Select One of Four Banks of RAMs
- Separate Output Enable for Multi-Channel Access to Memory
- Supports Scrubbing Operations and Other Specialty Access Modes
- Upgradable from F2968A 256K DRAM

LOGIC DIAGRAM

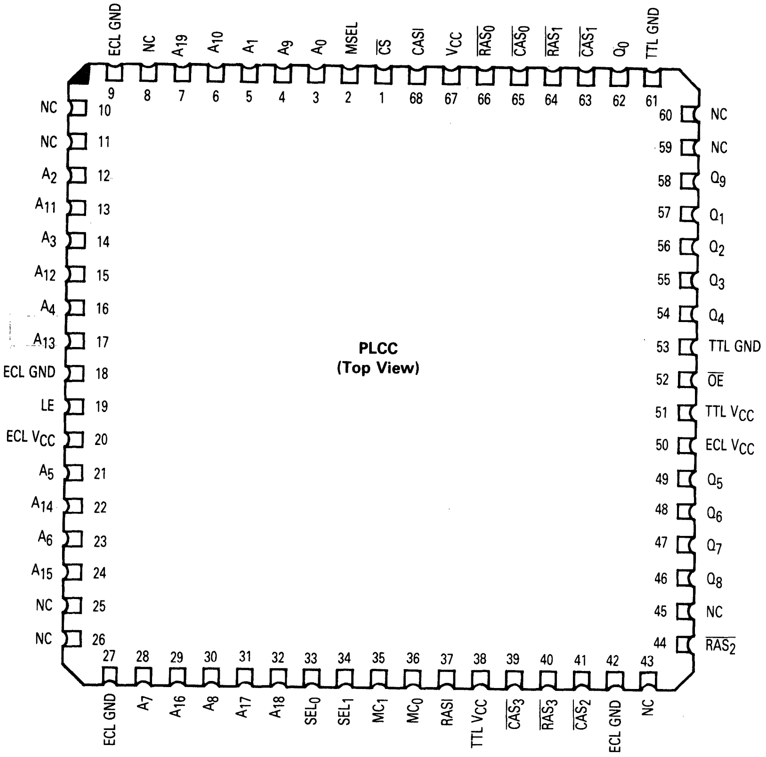

20
A0-A19
2
SEL0,1
LE
MSEL
CS
OE
2
MC0,1
RASI
CASI
10
Q0-Q9
4
RAS0-3
4
CAS0-3

BLOCK DIAGRAM

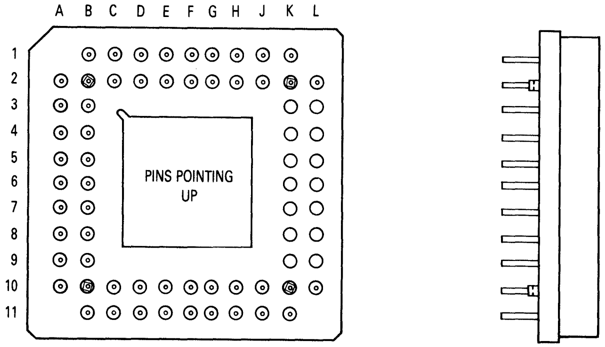

OE
ROW ADDRESS
(A0-A9)
ROW LATCH
COLUMN ADDRESS
(A10-A19)
COLUMN LATCH
MC0
MC1
MSEL
CS
LE
SEL0
SEL1
RASI
CASI
BANK LATCH
2
ROW COUNTER
CL
COLUMN COUNTER
CL
BANK COUNTER
CL
CNTR0,1
10
10
10
10
ADDRESS MUX
MUX CONTROL
2
RAS/CAS DECODE
10
QN
4
RASN
4
CASN

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

CONNECTIONS DIAGRAMS


ECL GND 9
NC 8
A_{19} 7
A_{10} 6
A_1 5
A_9 4
A_0 3
MSEL 2
$\overline{CS}$ 1
CASI 68
V_{CC} 67
$\overline{RAS_0}$ 66
$\overline{CAS_0}$ 65
$\overline{RAS_1}$ 64
$\overline{CAS_1}$ 63
Q_0 62
TTL GND 61
NC 10
NC 11
A_2 12
A_{11} 13
A_3 14
A_{12} 15
A_4 16
A_{13} 17
ECL GND 18
LE 19
ECL V_{CC} 20
A_5 21
A_{14} 22
A_6 23
A_{15} 24
NC 25
NC 26
60 NC
59 NC
58 Q_9
57 Q_1
56 Q_2
55 Q_3
54 Q_4
53 TTL GND
52 $\overline{OE}$
51 TTL V_{CC}
50 ECL V_{CC}
49 Q_5
48 Q_6
47 Q_7
46 Q_8
45 NC
44 $\overline{RAS_2}$
PLCC
(Top View)
27 ECL GND
28 A_7
29 A_{16}
30 A_8
31 A_{17}
32 A_{18}
33 SEL_0
34 SEL_1
35 MC_1
36 MC_0
37 RASI
38 TTL V_{CC}
39 $\overline{CAS_3}$
40 $\overline{RAS_3}$
41 $\overline{CAS_2}$
42 ECL GND
43 NC

PGA


A B C D E F G H J K L
1 2 3 4 5 6 7 8 9 10 11
PINS POINTING UP

PIN DESIGNATIONS							
(SORTED BY PIN NAME)				(SORTED BY PIN NUMBER)			
PIN NAME	**PIN NO.**	**PIN NAME**	**PIN NO.**	**PIN NO.**	**PIN NAME**	**PIN NO.**	**PIN NAME**
A_0	E-2	**NC**	A-10	**A-2**	GND	**G-1**	V_{CC}
A_1	D-1	**NC**	B-2	**A-3**	A_2	**G-2**	$\overline{\text{RAS}}_0$
A_2	A-3	**NC**	B-3	**A-4**	A_3	**G-10**	SEL_1
A_3	A-4	**NC**	B-10	**A-5**	A_4	**G-11**	SEL_0
A_4	A-5	**NC**	B-11	**A-6**	GND	**H-1**	$\overline{\text{CAS}}_0$
A_5	A-8	**NC**	C-1	**A-7**	LE	**H-2**	$\overline{\text{RAS}}_1$
A_6	A-9	**NC**	C-11	**A-8**	A_5	**H-10**	MC_0
A_7	D-10	**NC**	D-11	**A-9**	A_6	**H-11**	MC_1
A_8	E-11	**NC**	K-2	**A-10**	NC	**J-1**	$\overline{\text{CAS}}_1$
A_9	D-1	**$\overline{\text{OE}}$**	K-5	**B-1**	A_{19}	**J-2**	Q_0
A_{10}	C-2	**Q_0**	J-2	**B-2**	NC	**J-10**	V_{CC}
A_{11}	B-4	**Q_1**	K-3	**B-3**	NC	**J-11**	RASI
A_{12}	B-5	**Q_2**	L-3	**B-4**	A_{11}	**K-1**	GND
A_{13}	B-6	**Q_3**	K-4	**B-5**	A_{12}	**K-2**	NC
A_{14}	B-8	**Q_4**	L-4	**B-6**	A_{13}	**K-3**	Q_1
A_{15}	B-9	**Q_5**	L-7	**B-7**	V_{CC}	**K-4**	Q_3
A_{16}	E-10	**Q_6**	K-7	**B-8**	A_{14}	**K-5**	$\overline{\text{OE}}$
A_{17}	F-11	**Q_7**	L-8	**B-9**	A_{15}	**K-6**	V_{CC}
A_{18}	F-10	**Q_8**	K-8	**B-10**	NC	**K-7**	Q_6
A_{19}	B-1	**Q_9**	L-2	**B-11**	NC	**K-8**	Q_8
CASI	F-1	**RASI**	J-11	**C-1**	NC	**K-9**	GND
$\overline{\text{CAS}}_0$	H-1	**$\overline{\text{RAS}}_0$**	G-2	**C-2**	A_{10}	**K-10**	$\overline{\text{RAS}}_3$
$\overline{\text{CAS}}_1$	J-1	**$\overline{\text{RAS}}_1$**	H-2	**C-10**	GND	**K-11**	$\overline{\text{CAS}}_3$
$\overline{\text{CAS}}_2$	L-10	**$\overline{\text{RAS}}_2$**	L-9	**C-11**	NC	**L-2**	Q_9
$\overline{\text{CAS}}_3$	K-11	**$\overline{\text{RAS}}_3$**	K-10	**D-1**	A_9	**L-3**	Q_2
CS	F-2	**SEL_0**	G-11	**D-2**	A_1	**L-4**	Q_4
GND	A-2	**SEL_1**	G-10	**D-10**	A_7	**L-5**	GND
GND	A-6	**V_{CC}**	L-6	**D-11**	NC	**L-6**	V_{CC}
GND	C-10	**V_{CC}**	B-7	**E-1**	MSEL	**L-7**	Q_5
GND	K-1	**V_{CC}**	J-10	**E-2**	A_0	**L-8**	Q_7
GND	L-5	**V_{CC}**	G-1	**E-10**	A_{16}	**L-9**	$\overline{\text{RAS}}_2$
GND	K-9	**V_{CC}**	K-6	**E-11**	A_8	**L-10**	$\overline{\text{CAS}}_2$
LE	A-7			**F-1**	CASI		
MC_0	H-10			**F-2**	CS		
MC_1	H-11			**F-10**	A_{18}		
MSEL	E-1			**F-11**	A_{17}		

PIN DESCRIPTION

A_0–A_{19} Address Inputs (Input (20))

A_0–A_9 are latched in as the 10-bit Row Address for the RAM. These inputs drive Q_0–Q_9 when the F29368 is in the Read/Write mode and MSEL is LOW. A_{10}–A_{19} are latched in as the Column Address, and will drive Q_0–Q_9 when MSEL is HIGH and the DMC is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.

$\overline{\text{CAS}}_{0-3}$ $\overline{\text{Column Address Strobe}}$ (Output (4))

During normal Read/Write cycles the two select bits (SEL_0, SEL_1) determine which $\overline{\text{CAS}}_n$ output will go active following CASI going HIGH. When memory scrubbing is performed, only the $\overline{\text{CAS}}_n$ signal selected by CNTR_0 and CNTR_1 will be active (see $\overline{\text{CAS}}$ Output Function Table). For non-scrubbing cycles, all four $\overline{\text{CAS}}_n$ outputs remain HIGH.

CASI Column Address Strobe (Input (1))

This input going active will cause the selected $\overline{\text{CAS}}_n$ output to be forced LOW.

$\overline{\text{CS}}$ $\overline{\text{Chip Select}}$ (Input (1))

This active-LOW input is used to select the DMC. When $\overline{\text{CS}}$ is active, the F29368 operates normally in all four modes. When $\overline{\text{CS}}$ goes HIGH, the device will not enter the Read/Write mode. This allows more than one F29368 DMC to control multiple memory banks, thus providing an easy method for expanding the memory size.

LE Latch Enable (Input (1))

This active-HIGH input causes the Row, Column, and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.

MC_{0-1} Mode Control (Input (2))

These inputs are used to specify which of the four operating modes the DMC should be using. The description of the four operating modes is given in Table 1.

MSEL Multiplexer Select (Input (1))

This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on $\text{MC}_{0,1}$.

$\overline{\text{OE}}$ $\overline{\text{Output Enable}}$ (Input (1))

This active-LOW input enables/disables the output signals. When $\overline{\text{OE}}$ is HIGH, the outputs of the DMC enter the high-impedance state.

Q_{0-9} Address Outputs (Outputs (10))

These address outputs will feed the DRAM address inputs, and provide drive for memory systems up to 500 picofarads in capacitance.

$\overline{\text{RAS}}_{0-3}$ $\overline{\text{Row Address Strobe}}$ (Output (4))

Each one of the Row Address Strobe outputs provides a $\overline{\text{RAS}}_n$ signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL_0 and SEL_1 and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.

RASI Row Address Strobe (Input (1))

During normal memory cycles, the decoded $\overline{\text{RAS}}_n$ output ($\overline{\text{RAS}}_0$, $\overline{\text{RAS}}_1$, $\overline{\text{RAS}}_2$, or $\overline{\text{RAS}}_3$) is forced LOW after receipt of RASI. In either Refresh mode, all four $\overline{\text{RAS}}_n$ outputs will go LOW following RASI going HIGH.

SEL_{0-1} Bank Select (Input (2))

These two inputs are normally the two higher-order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the $\overline{\text{RAS}}_n$ and $\overline{\text{CAS}}_n$ signals after RASI and CASI go HIGH.

FUNCTIONAL DESCRIPTION

Architecture

The F29368 provides all the required data and refresh addresses needed by the dynamic RAM memory. In normal operation, the Row and Column addresses are multiplexed to the dynamic RAM by using MSEL, with the corresponding $\overline{\text{RAS}}_n$ and $\overline{\text{CAS}}_n$ signals activated to strobe the addresses into the RAM. High capacitance drivers on the outputs allow the DMC to drive four banks of 16-bit words, including a 6-bit checkword, for a total of 88 DRAMs.

MODE CONTROL FUNCTION TABLE

MC_1	MC_0	Operating Mode
0	0	Refresh without Scrubbing. Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $\overline{\text{RAS}}_n$ outputs are active while the four $\overline{\text{CAS}}_n$ signals are kept HIGH.
0	1	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $\overline{\text{RAS}}_n$ go active in response to RASI, while only one $\overline{\text{CAS}}_n$ output goes LOW in response to CASI. The Bank Counter keeps track of which $\overline{\text{CAS}}_n$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	Read/Write. This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL. SEL_0 and SEL_1 are decoded to determine which $\overline{\text{RAS}}_n$ and $\overline{\text{CAS}}_n$ will be active.
1	1	Clear Refresh Counter. This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{\text{RAS}}_n$ are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed.

ADDRESS OUTPUT FUNCTION TABLE

$\overline{\text{CS}}$	MC_1	MC_0	MSEL	Mode	MUX Output
0	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	1	Read/Write	Column Address Latch
			0		Row Address Latch
	1	1	X	Clear Refresh Counter	Zero
1	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	X	Read/Write	Zero
	1	1	X	Clear Refresh Counter	Zero

$\overline{\text{RAS}}$ OUTPUT FUNCTION TABLE

RASI	$\overline{\text{CS}}$	MC_1	MC_0	SEL_1	SEL_0	Mode	$\overline{\text{RAS}}_0$	$\overline{\text{RAS}}_1$	$\overline{\text{RAS}}_2$	$\overline{\text{RAS}}_3$
0	X	X	X	X	X	X	1	1	1	1
1	0	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1	X	X	Refresh with Scrubbing	0	0	0	0
		1	0	0	0	Read/Write	0	1	1	1
				0	1		1	0	1	1
				1	0		1	1	0	1
				1	1		1	1	1	0
		1	1	X	X	Clear Refresh Counter	0	0	0	0
	1	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1			Refresh with Scrubbing	0	0	0	0
		1	0			Read/Write	1	1	1	1
		1	1			Clear Refresh Counter	0	0	0	0

$\overline{CAS}$ OUTPUT FUNCTION TABLE

Inputs						Internal		Outputs			
CASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	$CNTR_1$	$CNTR_0$	$\overline{CAS_0}$	$\overline{CAS_1}$	$\overline{CAS_2}$	$\overline{CAS_3}$
1	0	0	0	X	X	X	X	1	1	1	1
		0	1	X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	0	0	X	X	0	1	1	1
				0	1			1	0	1	1
				1	0			1	1	0	1
				1	1			1	1	1	0
		1	1	X	X	X	X	1	1	1	1
	1	0	0	X	X	X	X	1	1	1	1
		0	1	X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	X	X	X	X	1	1	1	1
		1	1								
0	X	X	X	X	X	X	X	1	1	1	1

Input Latches

For those systems where addresses and data are multiplexed onto a single bus, the DMC has latches to hold the address information. The twenty input latches (Row, Column, and Bank Select) are transparent when Latch Enable (LE) is HIGH and will latch the input data meeting setup and hold time requirements when LE goes LOW. For systems where the processor has separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counters

The two 10-bit refresh counters make it possible to support 128, 256, 512, and 1024 line refresh. External control over which type of refresh is to be performed allows the user maximum flexibility when choosing the refreshing scheme. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counters are advanced at the HIGH-to-LOW transition of RASI. This assures a stable counter output for the next refresh cycle.

Refresh with Error Correction

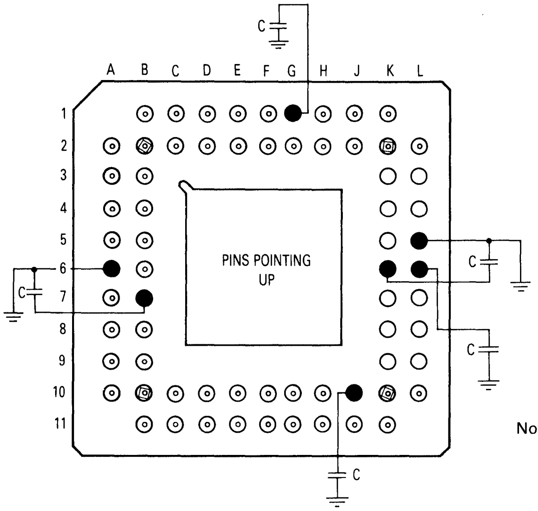
The F29368 makes it possible to correct single-bit errors in parallel with performing dynamic RAM refresh cycles. This "scrubbing" of memory can be done periodically as a background routine when the memory is not being used by the processor. In a memory scrubbing cycle ($MC_{1,0}$ = 01), the Row Address is strobed into all four banks with all four $\overline{RAS_n}$ outputs going LOW.

The Column Address is strobed into a single bank with the activated $\overline{CAS_n}$ output being selected by the Bank Counter. This type of cycle is used to simultaneously refresh the addressed row in all banks and read and correct (if necessary) one word in memory; thereby reducing the overhead associated with Error Detection and Correction. When doing refresh with memory scrubbing, both the Row and Column counters are multiplexed to the dynamic RAM address lines by using MSEL. Using the Refresh with Memory Scrubbing mode implies the presence of an error correcting facility such as the F2960A EDC unit. When doing refresh without scrubbing, all four $\overline{RAS_n}$ still go LOW but the $\overline{CAS_n}$ outputs are all driven HIGH so as not to activate the output lines of the memory.

Decoupling

Due to the high switching speeds and high drive capability of the F29368, it is necessary to decouple the device for proper operation. 1 μF multilayer ceramic capacitors are recommended for decoupling (see Figures 1a & 1b). It is important to mount the capacitors as close as possible to the power pins (V_{CC}, GND) to minimize lead inductance and noise. A ground plane is recommended.

It is strongly recommended that the F29368 be directly surface mounted whenever possible. Should a PLCC or PGA socket be required, a one-time-insertion-only socket with minimal lead lengths is necessary for proper device functioning.


C
A
B
C
D
E
F
G
H
J
K
L
1
2
3
4
5
6
7
8
9
10
11
PINS POINTING UP
C
C
C
C

PGA Hook-Ups

V_{CC}	GND
K6	L5
L6	GP
G1	GP
J10	GP
B7	A6

GP = Ground Plane

Note: PGA package has a different footprint from LCC or PLCC in a socket.

Figure 1a. PGA Decoupling Connection Diagram

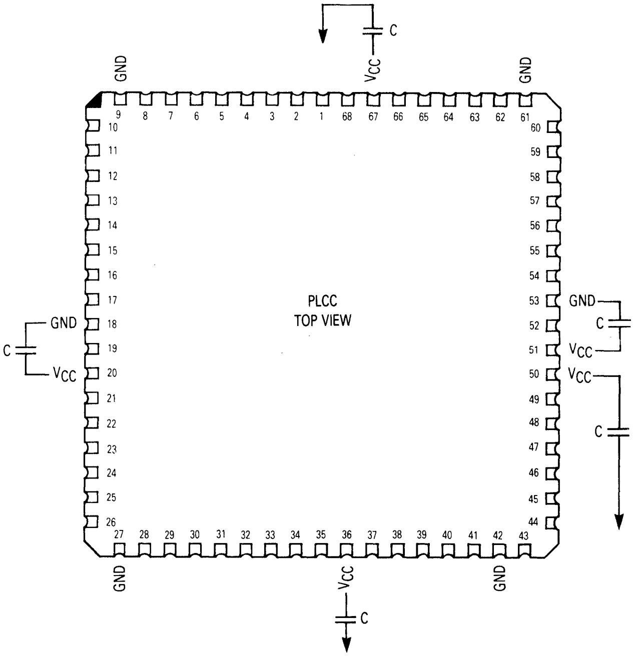

C
GND
V_{CC}
GND
PLCC
TOP VIEW
GND
C
V_{CC}
GND
C
V_{CC}
V_{CC}
C
GND
V_{CC}
GND
C

Figure 1b. PLCC Decoupling Connection Diagram

V_{ONP}

The guaranteed maximum undershoot voltage of the F29368 is −1.5 volts. V_{ONP} is measured with respect to ground (see Figure 1c). Note that the ground of the capacitive load must be the same as for the V_{CC} pin(s). As loading increases, V_{ONP} will approach zero.

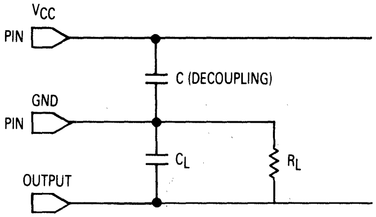
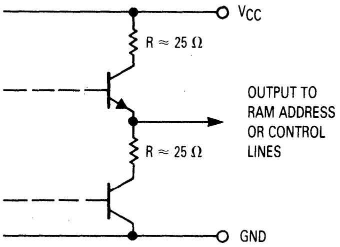


Figure 1c. V_{ONP} with Respect to Ground

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25 Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels. External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.



Typical Output Driver

APPLICATIONS

Timing Control

To obtain optimum performance and maximum design flexibility, the timing and control logic for the memory system has been kept a separate function. For systems implementing Error Detection and Correction, the F2969 Memory Timing Controller (MTC) provides all the necessary control signals for the F29368, F2961A/62A EDC Bus Buffers, and the F2960A EDC unit (See Figure 2a). Systems not using EDC, can use the F2970 MTC to provide the control for the F29368 (See Figure 2b). Both the F2969 and F2970 Memory Timing Controllers use a delay line to provide the most accurate timing reference from which the control signals are derived.

Memory Expansion

With a 10-bit address path, the F29368 can control up to one megaword memory when using 1M dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to double the memory size by using two F29368s. Memory can be increased in four megaword increments by adding another DMC unit. A sixteen-megaword memory system implementing EDC is shown in Figure 3.

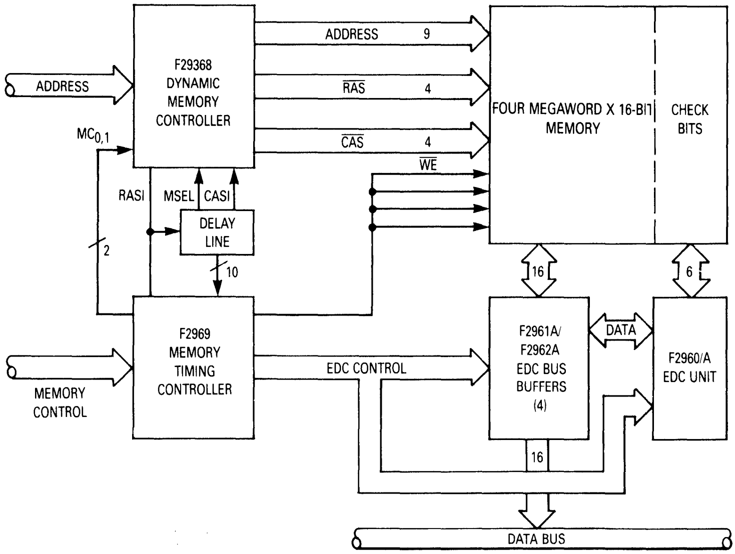

ADDRESS
MC0,1
2
F29368
DYNAMIC
MEMORY
CONTROLLER
RASI
MSEL
CASI
DELAY
LINE
10
ADDRESS 9
RAS 4
CAS 4
WE
FOUR MEGAWORD X 16-BIT
MEMORY
CHECK
BITS
16
6
F2969
MEMORY
TIMING
CONTROLLER
MEMORY
CONTROL
EDC CONTROL
F2961A/
F2962A
EDC BUS
BUFFERS
(4)
DATA
F2960/A
EDC UNIT
16
DATA BUS

Figure 2a. Four Megaword Dynamic Memory with Error Detection and Correction

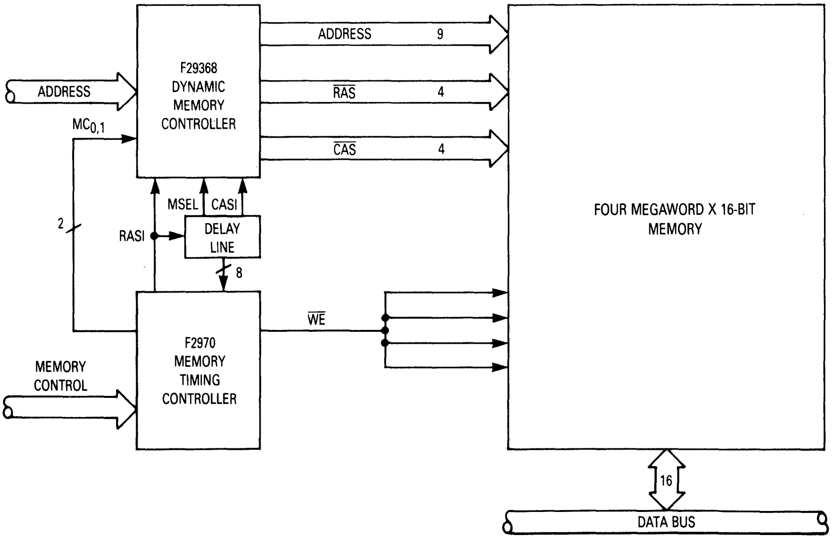

ADDRESS
MC0,1
2
F29368
DYNAMIC
MEMORY
CONTROLLER
MSEL
CASI
RASI
DELAY
LINE
8
ADDRESS 9
RAS 4
CAS 4
F2970
MEMORY
TIMING
CONTROLLER
MEMORY
CONTROL
WE
FOUR MEGAWORD X 16-BIT
MEMORY
16
DATA BUS

Figure 2b. Four Megaword Dynamic Memory

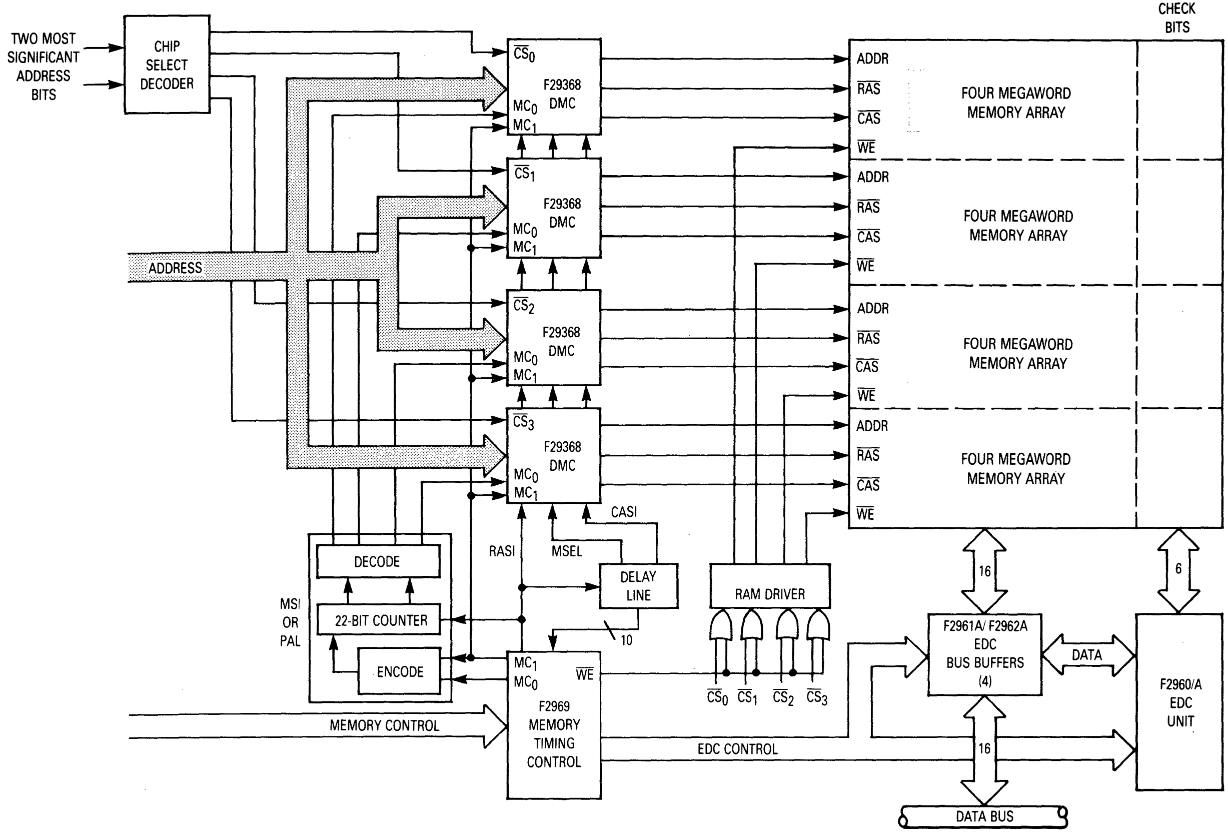

TWO MOST SIGNIFICANT ADDRESS BITS
CHIP SELECT DECODER
ADDRESS
$\overline{CS}_0$
F29368 DMC
MC_0
MC_1
$\overline{CS}_1$
$\overline{CS}_2$
$\overline{CS}_3$
CASI
RASI
MSEL
DELAY LINE
10
DECODE
22-BIT COUNTER
ENCODE
MSI OR PAL
MC_1
MC_0
$\overline{WE}$
F2969 MEMORY TIMING CONTROL
MEMORY CONTROL
EDC CONTROL
RAM DRIVER
$\overline{CS}_0$ $\overline{CS}_1$ $\overline{CS}_2$ $\overline{CS}_3$
ADDR
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
FOUR MEGAWORD MEMORY ARRAY
CHECK BITS
16
6
F2961A/ F2962A EDC BUS BUFFERS (4)
DATA
F2960/A EDC UNIT
16
DATA BUS

Figure 3. Sixteen Megaword Error Correcting Memory

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . −65°C to +150°C
Ambient Temperature with
Power Applied . . . . −55°C to +125°C
Supply Voltage . . . . −0.5 V to +7 V
DC Input Voltage . . . . −0.5 V to +5.5 V
DC Input Current . . . . −30 mA to +5 mA

GUARANTEED OPERATING RANGES

Commercial
T_A (Ambient) . . . . 0 to +70°C
V_{CC} . . . . 5 V to ±10%
Min . . . . 4.5 V
Max . . . . 5.5 V

DC CHARACTERISTICS (over operating ranges unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_{OH} = −1 mA	COMM	2.7			Volts
			MIL	2.5			
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1 mA			0.5	Volts
			I_{OL} = 12 mA			0.8	
V_{IH}	Input HIGH Level	Guaranteed input logical-HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical-LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4 V				−400	µA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 2.4 V				20	µA
I_I	Input HIGH Current	V_{CC} = Max, V_{IN} = 5.5 V				100	µA
I_{OZH}	Off-State Current	V_O = 2.4 V				50	µA
I_{OZL}	Off-State Current	V_O = 0.4 V				−50	µA
I_{OL}	Output Sink Current	V_{OL} = 2 V		45			mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max (Note 1)		−60	−95	−275	mA
I_{CC}	Power Supply Current	V_{CC} = Max	25°C, 5 V		260		mA
			0°C to +70°C			375	
			−55°C to 125°C			415	

Note 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (over operating range unless otherwise specified)

Light Capacitive Loading (Small System)

No.	Parameter	Description	Test Conditions	Min	Max	Units
ADDRESS/RASI/CASI/LE LINES (Note 1)						
1	t_{PD}	A_n to Q_n	C_L = 50 pF	3	20	ns
2	t_{PD}	MSEL to Q_n	C_L = 50 pF	3	20	ns
3	t_{PD}	MC_n to Q_n	C_L = 50 pF	5	24	ns
4	t_{PD}	LE to Q_n	C_L = 50 pF	5	25	ns
5	t_{PD}	$\overline{CS}$ to Q_n	C_L = 50 pF		23	ns
6	t_S	A_n/SEL_n to LE (Note 2)	C_L = 50 pF	5		ns
7	t_H	A_n/SEL_n to LE (Note 2)	C_L = 50 pF	5		ns
8	t_H	MC_1 to RASI	C_L = 50 pF	5		ns
9	t_S	$\overline{CS}$ to RASI	C_L = 50 pF	5		ns
10	t_S	SEL_n to RASI	C_L = 50 pF	5		ns
11	t_{PWL}	RASI, CASI	C_L = 50 pF	20		ns
12	t_{PWH}	RASI, CASI	C_L = 50 pF	20		ns
$\overline{RAS_n}$/$\overline{CAS_n}$ LINES (Notes 1 and 3)						
13	t_{PD}	RASI to $\overline{RAS_n}$	C_L = 50 pF	3	18	ns
14	t_{PD}	CASI to $\overline{CAS_n}$	C_L = 50 pF	3	17	ns
15	t_{PD}	LE to $\overline{RAS_n}$	C_L = 50 pF		25	ns
16	t_{PD}	LE to $\overline{CAS_n}$	C_L = 50 pF		24	ns
17	t_{PD}	MC_n to $\overline{RAS_n}$	C_L = 50 pF	3	21	ns
18	t_{PD}	MC_n to $\overline{CAS_n}$	C_L = 50 pF	3	19	ns
19	t_{PD}	$\overline{CS}$ to $\overline{RAS_n}$	C_L = 50 pF		20	ns
20	t_{PD}	$\overline{CS}$ to $\overline{CAS_n}$	C_L = 50 pF		19	ns
21	t_{PD}	SEL_n to $\overline{RAS_n}$	C_L = 50 pF		20	ns
22	t_{PD}	SEL_n to $\overline{CAS_n}$	C_L = 50 pF		18	ns
23	t_{SKEW}	[t_{PD} (RASI to $\overline{RAS_n}$) − t_{PD} (A_n to Q_n)] (MC_n = 10)	C_L = 50 pF			ns
			C_L = 50 pF			
24	t_{SKEW}	[t_{PD} (RASI to $\overline{RAS_n}$) − t_{PD} (MC_n to Q_n)] (MC_n = 00, 01)	C_L = 50 pF			ns
			C_L = 50 pF			
25	t_{SKEW}	[t_{PD} (MSEL to $\overline{Q_n}$) − t_{PD} (RASI to $\overline{RAS_n}$)]	C_L = 50 pF			ns
			C_L = 50 pF			
26	t_{SKEW}	[t_{PD} (CASI to $\overline{CAS_n}$) − (MSEL to Q_n)]	C_L = 50 pF			ns
			C_L = 50 pF			
THREE-STATE OUTPUTS/UNDERSHOOT (Note 4)						
27	t_{PLZ}	Output Disable Time from LOW, HIGH	C_L = 50 pF S = 1			ns
28	t_{PHZ}		S = 2			
29	t_{PZL}	Output Enable Time from LOW, HIGH	C_L = 50 pF S = 1			ns
30	t_{PZH}		S = 2			
31	V_{ONP}	Output Undershoot Voltage (Note 5)	C_L = 50 pF			V

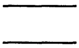
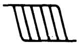
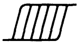
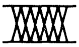
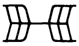
SWITCHING CHARACTERISTICS — continued (over operating range unless otherwise specified)

Heavy Capacitive Loading (Large Systems)

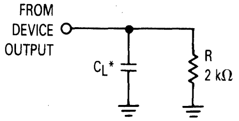
No.	Parameter	Description	Test Conditions	Min	Max	Units
ADDRESS/RASI/CASI/LE LINES (Note 1)						
1	t_{PD}	A_n to Q_n	C_L = 500 pF	12	40	ns
2	t_{PD}	MSEL to Q_n	C_L = 500 pF	12	42	ns
3	t_{PD}	MC_n to Q_n	C_L = 500 pF	12	44	ns
4	t_{PD}	LE to Q_n	C_L = 500 pF	12	46	ns
5	t_{PD}	$\overline{CS}$ to Q_n	C_L = 500 pF		45	ns
6	t_S	A_n/SEL_n to LE	C_L = 500 pF	5		ns
7	t_H	A_n/SEL_n to LE (Note 2)	C_L = 500 pF	5		ns
8	t_H	MC_1 to RASI (Note 2)	C_L = 500 pF	5		ns
9	t_S	$\overline{CS}$ to RASI	C_L = 500 pF	5		ns
10	t_S	SEL_n to RASI	C_L = 500 pF	5		ns
11	t_{PWL}	RASI, CASI	C_L = 500 pF	20		ns
12	t_{PWH}	RASI, CASI	C_L = 500 pF	20		ns
$\overline{RAS_n}/\overline{CAS_n}$ LINES (Notes 1 and 3)						
13	t_{PD}	RASI to $\overline{RAS_n}$	C_L = 200 pF	10	25	ns
			C_L = 350 pF	11	33	
14	t_{PD}	CASI to $\overline{CAS_n}$	C_L = 200 pF	10	24	ns
			C_L = 350 pF	11	31	
15	t_{PD}	LE to $\overline{RAS_n}$	C_L = 200 pF		31	ns
			C_L = 350 pF		38	
16	t_{PD}	LE to $\overline{CAS_n}$	C_L = 200 pF		30	ns
			C_L = 350 pF		37	
17	t_{PD}	MC_n to $\overline{RAS_n}$	C_L = 200 pF	10	27	ns
			C_L = 350 pF	11	34	
18	t_{PD}	MC_n to $\overline{CAS_n}$	C_L = 200 pF	10	29	ns
			C_L = 350 pF	11	37	
19	t_{PD}	$\overline{CS}$ to $\overline{RAS_n}$	C_L = 200 pF		25	ns
			C_L = 350 pF		32	
20	t_{PD}	$\overline{CS}$ to $\overline{CAS_n}$	C_L = 200 pF		24	ns
			C_L = 350 pF		31	
21	t_{PD}	SEL_n to $\overline{RAS_n}$	C_L = 200 pF		26	ns
			C_L = 350 pF		34	
22	t_{PD}	SEL_n to $\overline{CAS_n}$	C_L = 200 pF		25	ns
			C_L = 350 pF		33	
23	t_{SKEW}	[t_{PD} (RASI to $\overline{RAS_n}$) − t_{PD} (A_n to Q_n)] (MC_n = 10)	C_L = 200 pF	−17	−3	ns
			C_L = 350 pF	−13	−3	
24	t_{SKEW}	[t_{PD} (RASI to $\overline{RAS_n}$) − t_{PD} (MC_n to Q_n)] (MC_n = 00, 01)	C_L = 200 pF	−16	−1	ns
			C_L = 350 pF	−16	−1	
25	t_{SKEW}	[t_{PD} (MSEL to $\overline{Q_n}$) − t_{PD} (RASI to $\overline{RAS_n}$)]	C_L = 200 pF	−6	11	ns
			C_L = 350 pF	−6	6	
26	t_{SKEW}	[t_{PD} (CASI to $\overline{CAS_n}$) − (MSEL to Q_n)]	C_L = 200 pF	−18	−5	ns
			C_L = 350 pF	−13	−5	

Notes:
1. Reference Figures A and C apply to all parameters except Parameters 8, 9, and 10.
2. Hold times are not tested, but are guaranteed by characterization data.
3. C_L = 200 pF loading corresponds to 4 banks, 22 bits (16 data bits + 6 check bits).
C_L = 350 pF loading corresponds to 4 banks, 39 bits (32 data bits + 7 check bits).
4. See Reference Figures B and D.
5. V_{ONP} is not production tested but is guaranteed by characterization data. Limit specified is for all outputs switching simultaneously with minimum specified loading. As loading increases, V_{ONP} will approach zero.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

SWITCHING TEST CIRCUITS


FROM
DEVICE
OUTPUT
C_L*
R
2 kΩ

*t_{pd} specified at C_L = 50 and 500 pF for Q_n
C_L = 50, 200 and 350 pF for $\overline{RAS_n}$, $\overline{CAS_n}$

Figure 4. Capacitive Load Switching

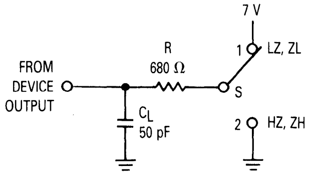
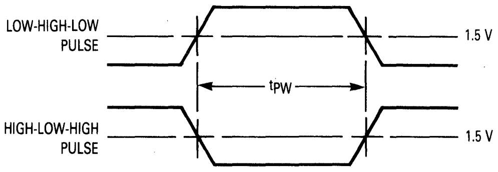

7 V
R
680 Ω
1
LZ, ZL
FROM
DEVICE
OUTPUT
S
C_L
50 pF
2
HZ, ZH

Figure 5. Three-State Enable/Disable


LOW-HIGH-LOW
PULSE
1.5 V
t_{PW}
HIGH-LOW-HIGH
PULSE
1.5 V

Pulse Width

SWITCHING TEST WAVEFORMS (Cont'd.)

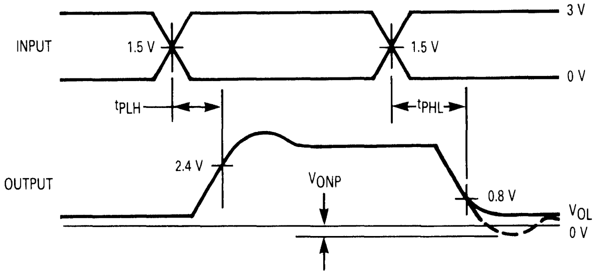
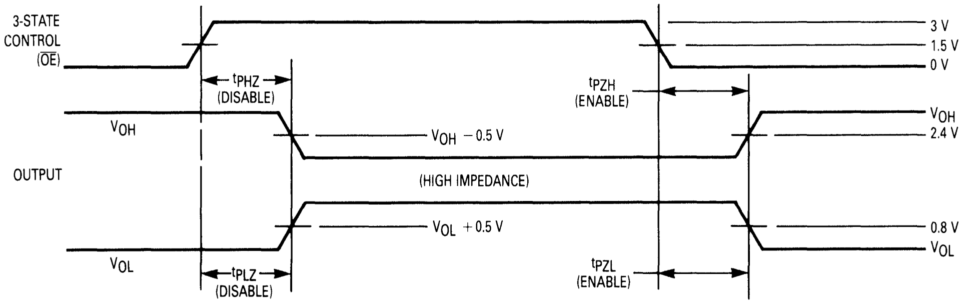

INPUT
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
OUTPUT
2.4 V
VONP
0.8 V
VOL
0 V

Figure 6. Output Drivers Levels


3-STATE CONTROL (OE)
3 V
1.5 V
0 V
tPHZ (DISABLE)
tPZH (ENABLE)
VOH
VOH − 0.5 V
VOH
2.4 V
OUTPUT
(HIGH IMPEDANCE)
VOL + 0.5 V
0.8 V
VOL
VOL
tPLZ (DISABLE)
tPZL (ENABLE)

Note: Decoupling is needed for all AC tests

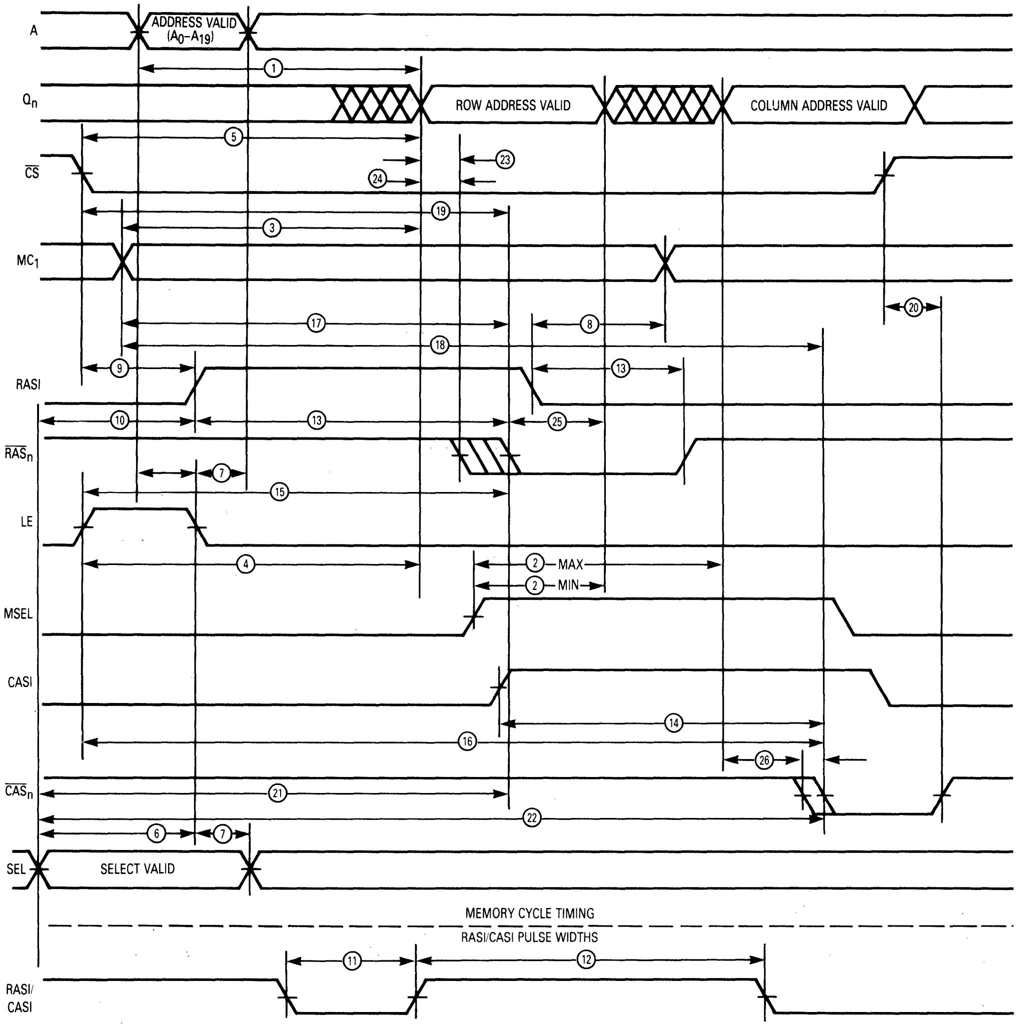
Figure 7. Three-State Control Levels

GENERAL TEST NOTES

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. Recommended levels are $V_{IL} \leq 0$ V and $V_{IH} \geq 4$ V for AC tests.
5. Automatic tester hardware and handler add additional round trip A.C. delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

SWITCHING WAVEFORMS


A
ADDRESS VALID (A0–A19)
Qn
ROW ADDRESS VALID
COLUMN ADDRESS VALID
CS
MC1
RASI
RASn
LE
MSEL
CASI
CASn
SEL
SELECT VALID
MEMORY CYCLE TIMING
RASI/CASI PULSE WIDTHS
RASI/ CASI
1
2 MAX
2 MIN
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26

F29368 Dynamic Memory Controller Timing

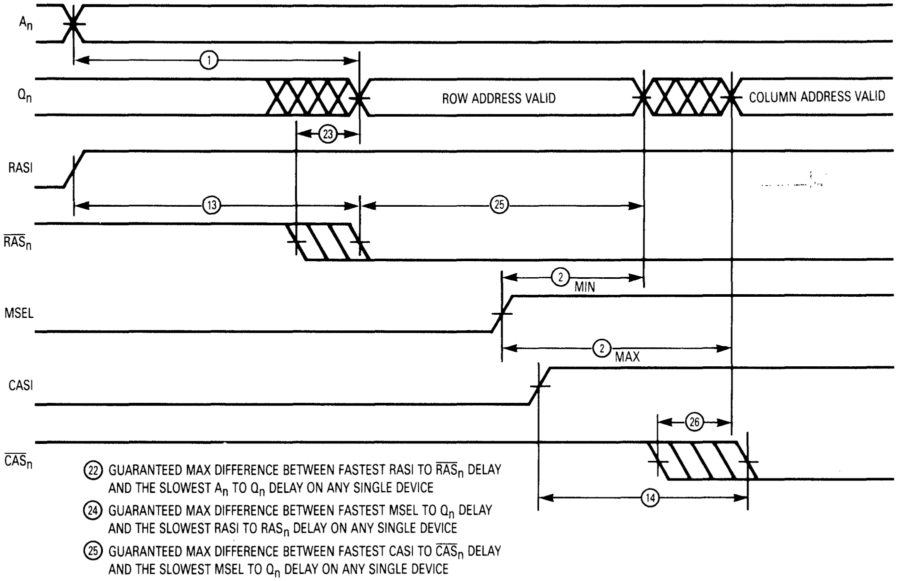
MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 8. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

The minimum requirement for T_1, T_2 and T_3 are as follows:

T_1 Min = $t_{ASR} + t_{23}$
T_2 Min = $t_{RAH} + t_{25}$
T_3 Min = $T_2 + t_{26} + t_{ASC}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.

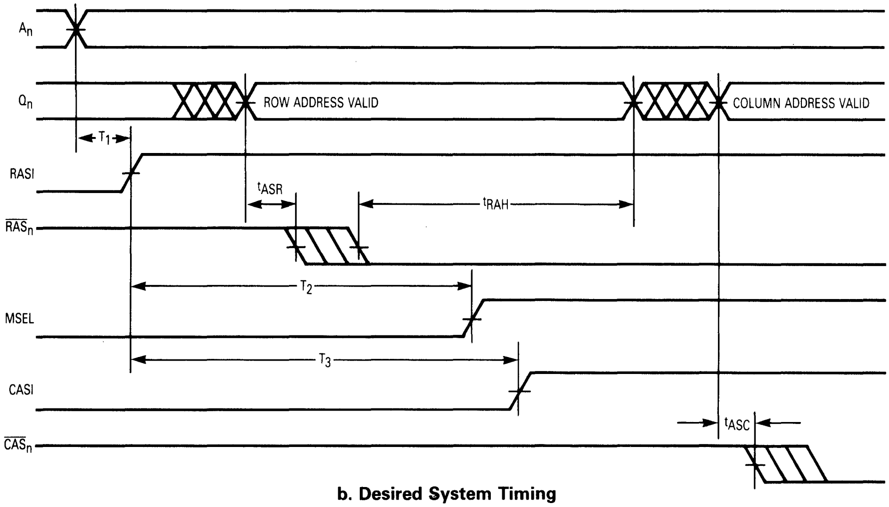

A_n
Q_n
ROW ADDRESS VALID
COLUMN ADDRESS VALID
RASI
$\overline{RAS}_n$
MSEL
CASI
$\overline{CAS}_n$
①
㉓
⑬
㉕
② MIN
② MAX
㉖
⑭

㉒ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_n$ DELAY AND THE SLOWEST A_n TO Q_n DELAY ON ANY SINGLE DEVICE

㉔ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST MSEL TO Q_n DELAY AND THE SLOWEST RASI TO RAS_n DELAY ON ANY SINGLE DEVICE

㉕ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST CASI TO $\overline{CAS}_n$ DELAY AND THE SLOWEST MSEL TO Q_n DELAY ON ANY SINGLE DEVICE

Figure 8. Memory Cycle Timing
a. Specifications Applicable to Memory Cycle Timing (MC_n = 1, 0)


A_n
Q_n
ROW ADDRESS VALID
COLUMN ADDRESS VALID
T_1
RASI
t_{ASR}
t_{RAH}
$\overline{RAS}_n$
T_2
MSEL
T_3
CASI
t_{ASC}
$\overline{CAS}_n$

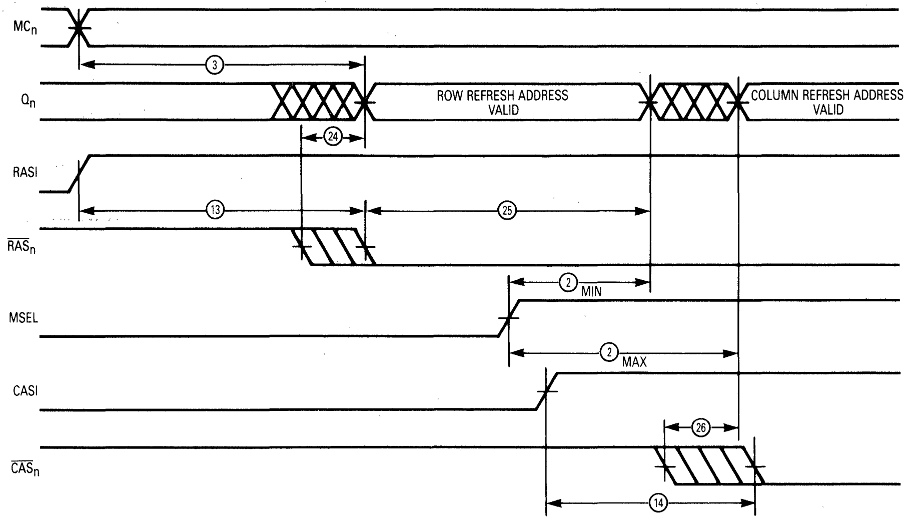
b. Desired System Timing

REFRESH CYCLE TIMING

The timing relationships for refresh are shown in Figure 9.

T_4 minimum is calculated as follows:

$T_4 \text{ Min} = t_{ASR} + t_{24}$


MCn
Qn
ROW REFRESH ADDRESS VALID
COLUMN REFRESH ADDRESS VALID
RASI
RASn
MSEL
CASI
CASn
③
㉔
⑬
㉕
② MIN
② MAX
㉖
⑭

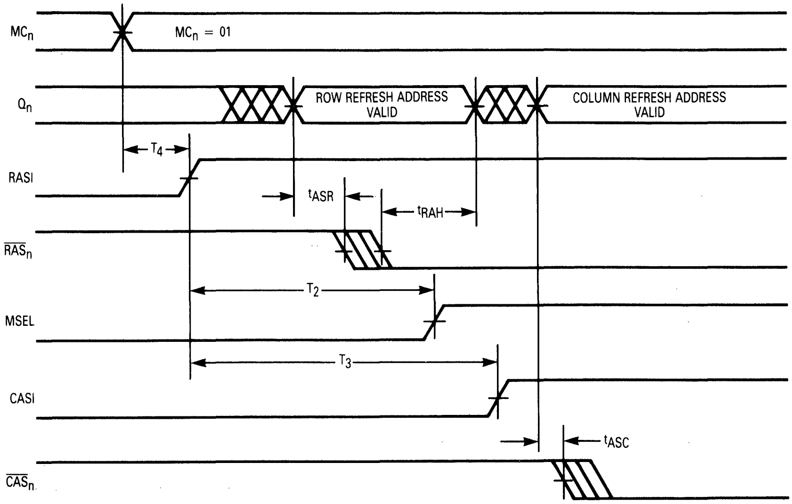
㉒ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_n$ DELAY AND THE SLOWEST A_n TO Q_n DELAY ON ANY SINGLE DEVICE

㉓ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST RASI TO $\overline{RAS}_n$ DELAY AND THE SLOWEST MC_n TO Q_n DELAY ON ANY SINGLE DEVICE

㉔ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST MSEL TO Q_n DELAY AND THE SLOWEST RASI TO $\overline{RAS}_n$ DELAY ON ANY SINGLE DEVICE

㉕ GUARANTEED MAX DIFFERENCE BETWEEN FASTEST CASI TO CAS_n DELAY AND THE SLOWEST MSEL TO Q_n DELAY ON ANY SINGLE DEVICE

Figure 9. Refresh Cycle Timing
a. Specifications Applicable to Refresh Cycle Timing (MC_n = 00, 01)


MCn
MCn = 01
Qn
ROW REFRESH ADDRESS VALID
COLUMN REFRESH ADDRESS VALID
T4
RASI
tASR
tRAH
RASn
T2
MSEL
T3
CASI
tASC
CASn

b. Desired Timing: Refresh with Scrubbing

REFRESH CYCLE TIMING

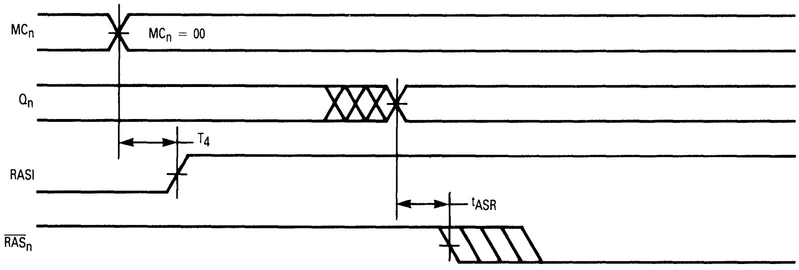


Figure 9. Refresh Cycle Timing (Cont'd.)
c. Desired Timing: Refresh without Scrubbing

TYPICAL PERFORMANCE CURVES

NANOSECONDS VERSUS PICOFARADS

The Switching Characteristics Tables specify the minimum and maximum propagation delays for effective capacitive loads of 50 pF and 500 pF on Address Lines and 50 pF, 200 pF, and 350 pF on $\overline{RAS_n}$ and $\overline{CAS_n}$ Lines. The upper limits represent the maximum calculated load for the following conditions:

Address Lines: 500 pF = 16 data bits + 6 check bits, four banks
500 pF = 32 data bits + 7 check bits, two banks

$\overline{RAS_n}/\overline{CAS_n}$: 200 pF = 16 data bits + 6 check bits, four banks
350 pF = 32 data bits + 7 check bits, four banks

A more comprehensive analysis of loading is given in the table below.

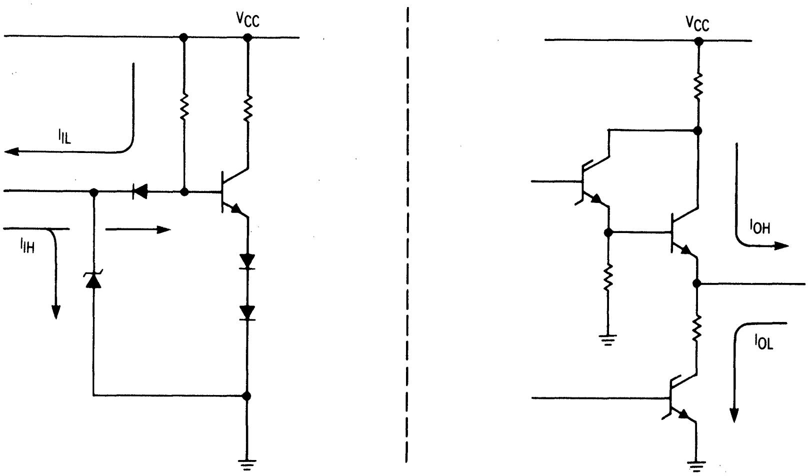
16-Bit Systems (plus 6 Check Bits for Error Detection and Correction)

DMC Output	No. of DRAMs	Line Drive	Total Required Drive for Indicated Banks 1	2	4	Specified Data Sheet Load
Q_n (Address)	16 + 6 = 22	5 pF	100 pF	220 pF	440 pF	500 pF
$\overline{RAS_n}$		8 pF	176 pF	176 pF	176 pF	200 pF
$\overline{CAS_n}$		8 pF	176 pF	176 pF	176 pF	200 pF

32-Bit Systems (plus 7 Check Bits for Error Detection and Correction)

DMC Output	No. of DRAMs	Line Drive	Total Required Drive for Indicated Banks 1	2	4	Specified Data Sheet Load
Q_n (Address)	32 + 7 = 39	5 pF	195 pF	390 pF	780 pF	500 pF
$\overline{RAS_n}$		8 pF	312 pF	312 pF	312 pF	350 pF
$\overline{CAS_n}$		8 pF	312 pF	312 pF	312 pF	350 pF

INPUT/OUTPUT CIRCUIT DIAGRAM

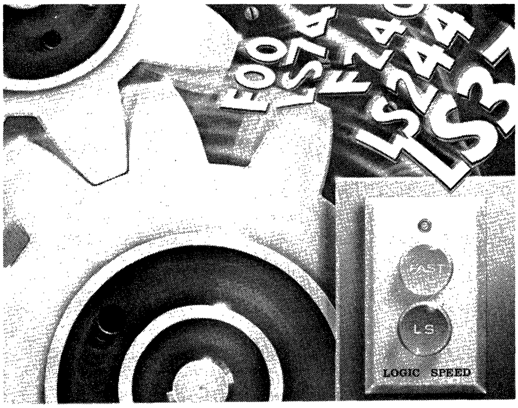


Driven Input

Driving Output

V_{CC}
I_{IL}
I_{IH}
V_{CC}
I_{OH}
I_{OL}

FAST AND LS


LS244
LS74
F00
FAST
LS
LOGIC SPEED

LS Data Sheets

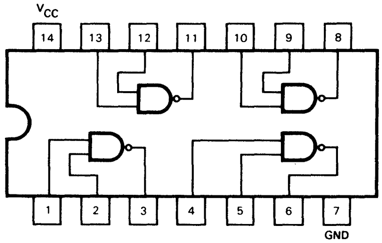
5

MOTOROLA

SN54/74LS00

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 1.6 4.4	mA	V_{CC} = MAX

AC CHARACTERISTICS: $T_A = 25°C$

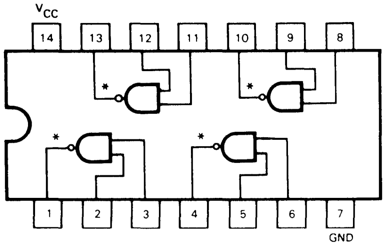
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

MOTOROLA

SN54/74LS01

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
I_{OH}	Output HIGH Current	54,74			100	μA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0$ mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
I_{CC}	Power Supply Current Total, Output HIGH				1.6	mA	V_{CC} = MAX	
	Total, Output LOW				4.4			

AC CHARACTERISTICS: $T_A = 25°C$

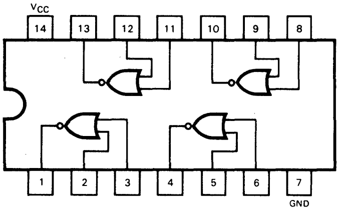
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		17	32	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF, $R_L = 2.0$ kΩ
t_{PHL}	Turn On Delay, Input to Output		15	28	ns	

MOTOROLA

SN54/74LS02

QUAD 2-INPUT NOR GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				3.2	mA	V_{CC} = MAX	
	Total, Output LOW				5.4			

AC CHARACTERISTICS: T_A = 25°C

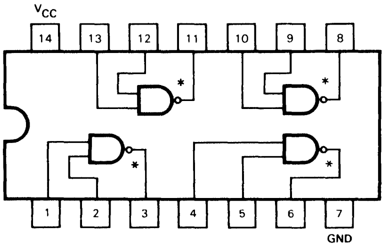
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	

MOTOROLA

SN54/74LS03

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH				1.6	mA	V_{CC} = MAX	
	Total, Output LOW				4.4			

AC CHARACTERISTICS: T_A = 25°C

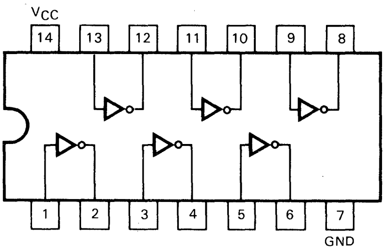
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		17	32	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL}	Turn On Delay, Input to Output		15	28	ns	

MOTOROLA

SN54/74LS04

HEX INVERTER

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

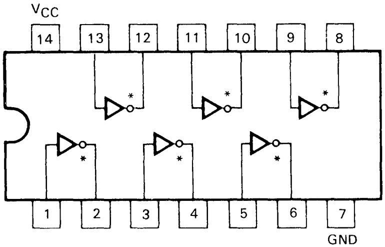
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				2.4	mA	V_{CC} = MAX
	Total, Output LOW				6.6		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

MOTOROLA



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

SN54/74LS05

HEX INVERTER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.4	mA	V_{CC} = MAX	
	Total, Output LOW				6.6			

AC CHARACTERISTICS: $T_A = 25°C$

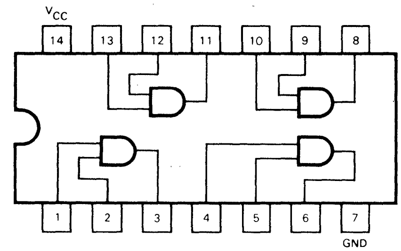
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		17	32	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL}	Turn On Delay, Input to Output		15	28	ns	

MOTOROLA

SN54/74LS08

QUAD 2-INPUT AND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				4.8	mA	V_{CC} = MAX	
	Total, Output LOW				8.8			

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AC CHARACTERISTICS: T_A = 25°C

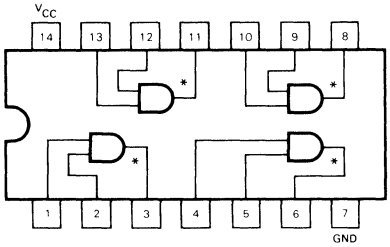
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	20	ns	C_L = 15 pF

MOTOROLA

SN54/74LS09

QUAD 2-INPUT AND GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH				4.8	mA	V_{CC} = MAX	
	Total, Output LOW				8.8			

AC CHARACTERISTICS: T_A = 25°C

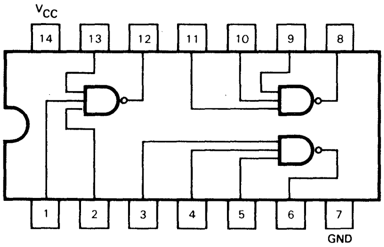
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		20	35	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL}	Turn On Delay, Input to Output		17	35	ns	

MOTOROLA

SN54/74LS10

TRIPLE 3-INPUT NAND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				1.2	mA	V_{CC} = MAX	
	Total, Output LOW				3.3			

AC CHARACTERISTICS: T_A = 25°C

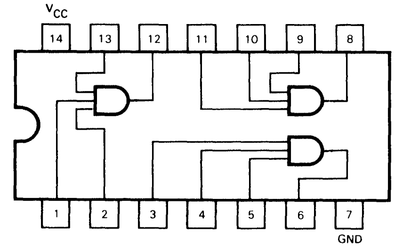
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

MOTOROLA

SN54/74LS11

TRIPLE 3-INPUT AND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				3.6	mA	V_{CC} = MAX	
	Total, Output LOW				6.6			

AC CHARACTERISTICS: T_A = 25°C

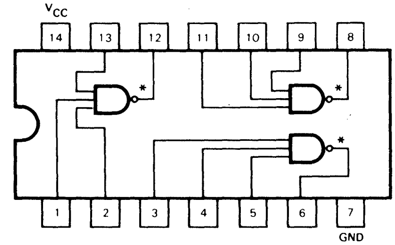
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	20	ns	C_L = 15 pF

MOTOROLA

SN54/74LS12

TRIPLE 3-INPUT NAND GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUT

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current Total, Output HIGH				1.4	mA	V_{CC} = MAX
	Total, Output LOW				3.3		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		17	32	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		15	28	ns	C_L = 15 pF, R_L = 2.0 kΩ

MOTOROLA

SN54/74LS13
SN54/74LS14

SCHMITT TRIGGERS
DUAL GATE/HEX INVERTER

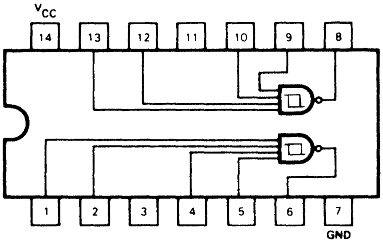
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS13 and SN54LS/74LS14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

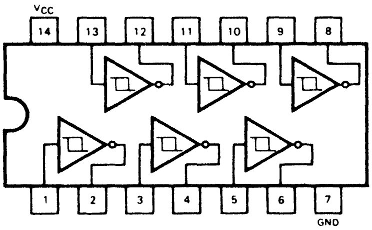
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAMS

SN54/74LS13



SN54/74LS14



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

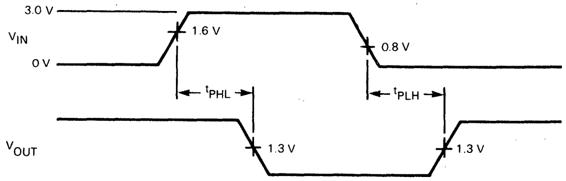
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{T+}	Positive-Going Threshold Voltage		1.5		2.0	V	$V_{CC} = 5.0$ V
V_{T-}	Negative-Going Threshold Voltage		0.6		1.1	V	$V_{CC} = 5.0$ V
V_{T+}-V_{T-}	Hysteresis		0.4	0.8		V	$V_{CC} = 5.0$ V
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, $I_{OH} = -400$ µA, $V_{IN} = V_{IL}$
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, $I_{OL} = 4.0$ mA, $V_{IN} = 2.0$ V
		74		0.35	0.5	V	V_{CC} = MIN, $I_{OL} = 8.0$ mA, $V_{IN} = 2.0$ V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T+}$
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T-}$
I_{IH}	Input HIGH Current			1.0	20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX, $V_{OUT} = 0$ V
I_{CC}	Power Supply Current Total, Output HIGH	LS13		2.9	6.0	mA	V_{CC} = MAX
		LS14		8.6	16		
	Total, Output LOW	LS13		4.1	7.0		
		LS14		12	21		

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	MAX		UNITS	TEST CONDITIONS
		LS13	LS14		
t_{PLH}	Propagation Delay, Input to Output	22	22	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PHL}	Propagation Delay, Input to Output	27	22	ns	



V_{IN} VERSUS V_{OUT} TRANSFER FUNCTION

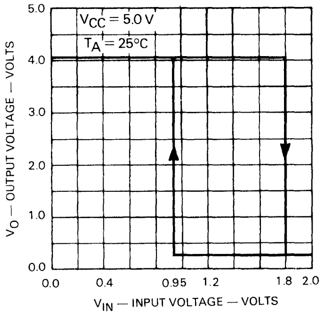


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

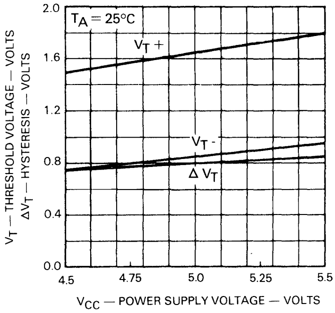


Fig. 2

THRESHOLD VOLTAGE HYSTERESIS VERSUS TEMPERATURE

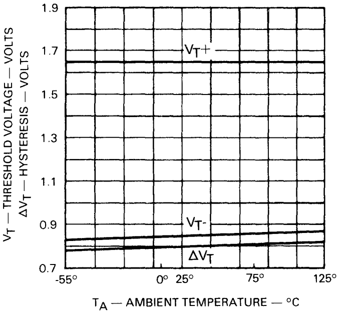


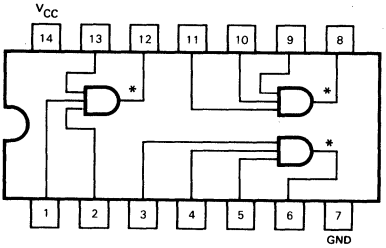
Fig. 3

MOTOROLA

SN54/74LS15

TRIPLE 3-INPUT AND GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 3.6 6.6	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

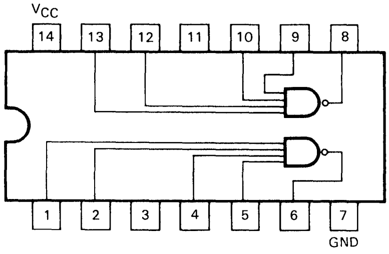
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		20	35	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL}	Turn On Delay, Input to Output		17	35	ns	

MOTOROLA

SN54/74LS20

DUAL 4-INPUT NAND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				0.8	mA	V_{CC} = MAX	
	Total, Output LOW				2.2			

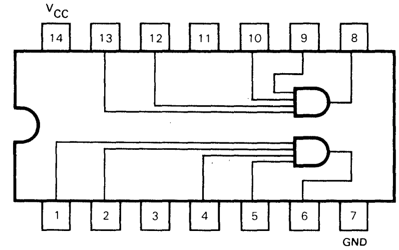
AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

SN54/74LS21

DUAL 4-INPUT AND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 2.4 4.4	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

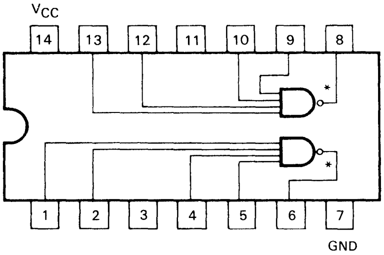
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	20	ns	C_L = 15 pF

MOTOROLA

SN54/74LS22

DUAL 4-INPUT NAND GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5 5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current	54,74			100	μA	V_{CC} = MIN, V_{OH} = MAX
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current Total, Output HIGH				0.8	mA	V_{CC} = MAX
	Total, Output LOW				2.2		

AC CHARACTERISTICS: $T_A = 25°C$

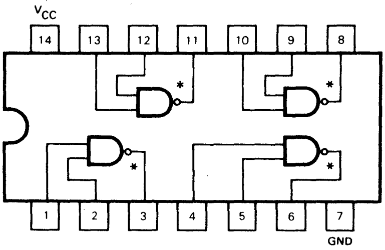
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		17	32	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL}	Turn On Delay, Input to Output		15	28	ns	

MOTOROLA

SN54/74LS26

QUAD 2-INPUT NAND BUFFER

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			15	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			1000	µA	V_{CC} = MIN, V_{OH} = MAX	
		54,74			50	µA	V_{CC} = MIN, V_{OH} = 12 V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.4 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 1.6 4.4	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

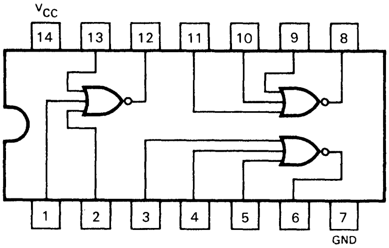
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		17	32	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL}	Turn On Delay, Input to Output		15	28	ns	

MOTOROLA

SN54/74LS27

TRIPLE 3-INPUT NOR GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				4.0 6.8	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

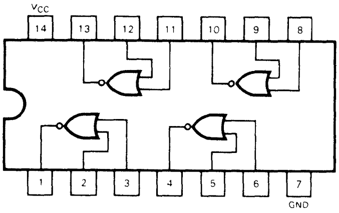
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

MOTOROLA

SN54/74LS28

QUAD 2-INPUT NOR BUFFER

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.2	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 3.6 13.8	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

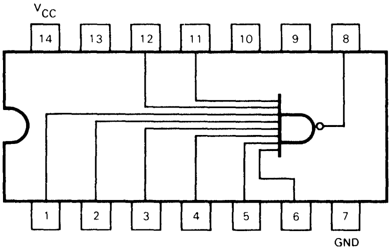
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Propagation Delay		12	24	ns	V_{CC} = 5.0 V C_L = 45 pF, R_L = 667 Ω
t_{PHL}	Propagation Delay		12	24	ns	

MOTOROLA

SN54/74LS30

8-INPUT NAND GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

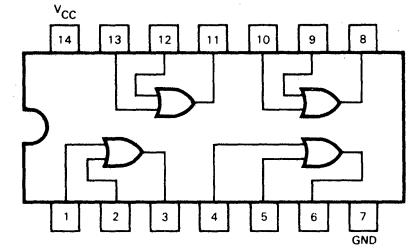
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				0.5	mA	V_{CC} = MAX
	Total, Output LOW				1.1		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		13	20	ns	C_L = 15 pF

MOTOROLA



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

SN54/74LS32

QUAD 2-INPUT OR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				6.2	mA	V_{CC} = MAX	
	Total, Output LOW				9.8			

AC CHARACTERISTICS: T_A = 25°C

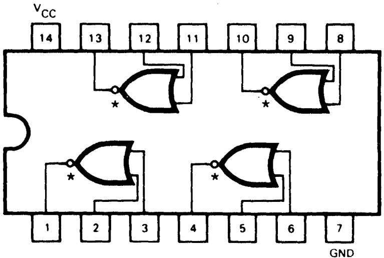
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		14	22	ns	C_L = 15 pF

MOTOROLA

SN54/74LS33

QUAD 2-INPUT NOR BUFFER

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54			12	mA
		74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			250	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH				3.6	mA	V_{CC} = MAX	
	Total, Output LOW				13.8			

AC CHARACTERISTICS: T_A = 25°C

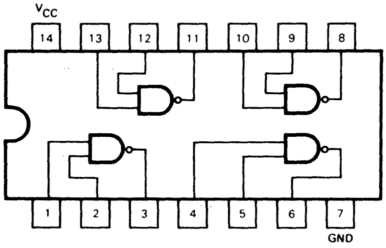
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		20	32	ns	V_{CC} = 5.0 V, R_L = 667 Ω C_L = 45 pF
t_{PHL}	Turn On Delay, Input to Output		18	28	ns	

MOTOROLA

SN54/74LS37

QUAD 2-INPUT NAND BUFFER

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.2	mA
I_{OL}	Output Current — Low	54			12	mA
		74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 2.0 12	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

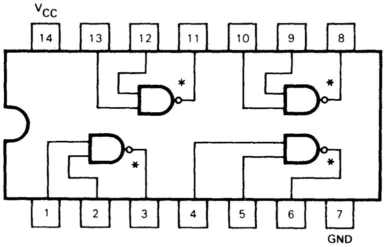
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		12	24	ns	V_{CC} = 5.0 V, R_L = 667 Ω
t_{PHL}	Turn On Delay, Input to Output		12	24	ns	C_L = 45 pF

MOTOROLA

SN54/74LS38

QUAD 2-INPUT NAND BUFFER

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			250	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.4 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.0	mA	V_{CC} = MAX	
	Total, Output LOW				12			

AC CHARACTERISTICS: T_A = 25°C

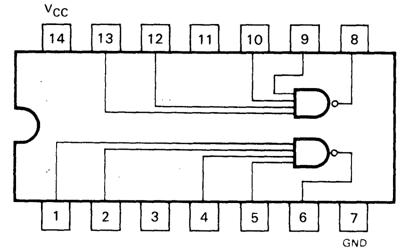
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		20	32	ns	V_{CC} = 5.0 V, R_L = 667 Ω C_L = 45 pF
t_{PHL}	Turn On Delay, Input to Output		18	28	ns	

MOTOROLA

SN54/74LS40

DUAL 4-INPUT NAND BUFFER

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.2	mA
I_{OL}	Output Current — Low	54			12	mA
		74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				1.0	mA	V_{CC} = MAX
	Total, Output LOW				6.0		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		12	24	ns	V_{CC} = 5.0 V, R_L = 667 Ω C_L = 45 pF
t_{PHL}	Turn On Delay, Input to Output		12	24	ns	

MOTOROLA

SN54/74LS42

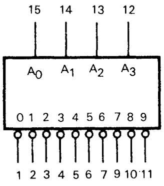
ONE-OF-TEN DECODER

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **MULTI-FUNCTON CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL

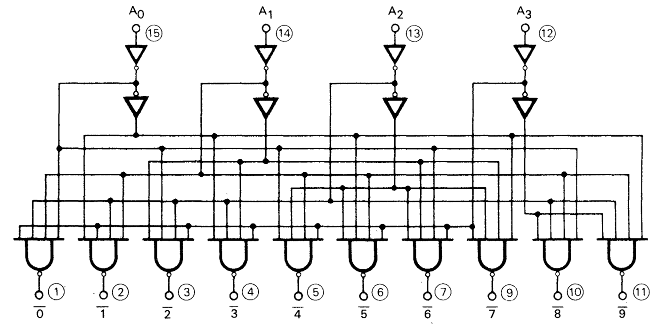

15
14
13
12
A_0
A_1
A_2
A_3
0 1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 9 10 11

V_{CC} = Pin 16
GND = Pin 8

PIN NAMES		LOADING (Note a) HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

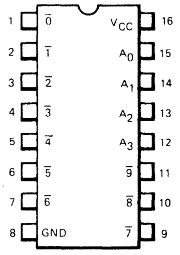
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM


A_0
A_1
A_2
A_3
⑮
⑭
⑬
⑫
①
②
③
④
⑤
⑥
⑦
⑨
⑩
⑪
$\overline{0}$
$\overline{1}$
$\overline{2}$
$\overline{3}$
$\overline{4}$
$\overline{5}$
$\overline{6}$
$\overline{7}$
$\overline{8}$
$\overline{9}$

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP
(TOP VIEW)


1
2
3
4
5
6
7
8
$\overline{0}$
$\overline{1}$
$\overline{2}$
$\overline{3}$
$\overline{4}$
$\overline{5}$
$\overline{6}$
GND
V_{CC}
A_0
A_1
A_2
A_3
$\overline{9}$
$\overline{8}$
$\overline{7}$
16
15
14
13
12
11
10
9

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				13	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)		15 15	25 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)		20 20	30 30	ns	Fig. 1	

AC WAVEFORMS

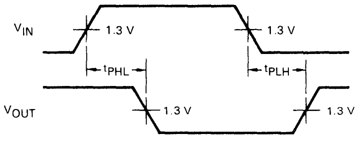


Fig. 1

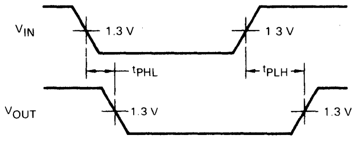


Fig. 2

MOTOROLA

SN54/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

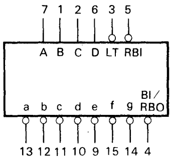
The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54LS/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54LS/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

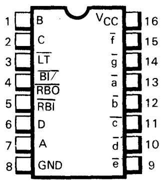
- **LAMP INTENSITY MODULATION CAPABILITY**
- **OPEN COLLECTOR OUTPUTS**
- **LAMP TEST PROVISION**
- **LEADING/TRAILING ZERO SUPPRESSION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



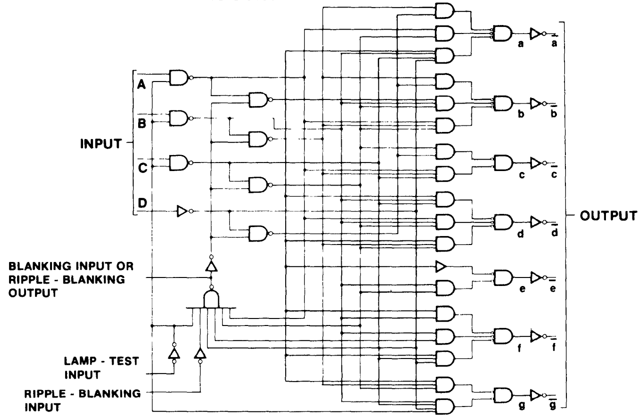
J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

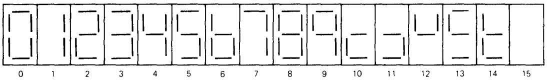
PIN NAMES **LOADING** (Note a)

		HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp Test Input	0.5 U.L.	0:25 U.L.
$\overline{BI/RBO}$	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple Blanking Output	1.2 U.L.	2.0 U.L.
$\bar{a}$, to $\bar{g}$	Outputs	Open-Collector	15 (7.5) U.L.

Notes:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM





NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS						OUTPUTS								
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI/RBO}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High $\overline{\text{BI/RBO}}$	54,74			−50	µA
I_{OL}	Output Current — Low $\overline{\text{BI/RBO}}$	54			1.6	mA
	$\overline{\text{BI/RBO}}$	74			3.2	
$V_{O\ (off)}$	Off-State Output Voltage $\bar{a}$ to $\bar{g}$	54,74			15	V
$I_{O\ (on)}$	On-State Output Current $\bar{a}$ to $\bar{g}$	54			12	mA
	$\bar{a}$ to $\bar{g}$	74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage, $\overline{\text{BI/RBO}}$		2.4	4.2		V	V_{CC} = MIN, I_{OH} = −50 µA, V_{IN} = V_{IN}or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 1.6 mA	V_{CC} = MIN, V_{IN} = V_{IN}
	$\overline{\text{BI/RBO}}$	74		0.35	0.5	V	I_{OL} = 3.2 MA	or V_{IL} per Truth Table
$I_{O\ (off)}$	Off-State Output Current $\bar{a}$ thru $\bar{g}$				250	µA	V_{CC} = MAX, V_{IN} = V_{IN} or V_{IL} per Truth Table, V_O (off) = 15 V	
$V_{O\ (on)}$	On-State Output Voltage	54,74		0.25	0.4	V	$I_{O(on)}$ = 12 mA	V_{CC}= MAX, V_{IN} = V_{IH}
	$\bar{a}$ thru $\bar{g}$	74		0.35	0.5	V	I_O(on) = 24 MA	or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{\text{BI/RBO}}$ Any Input except $\overline{\text{BI/RBO}}$				−1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS} $\overline{\text{BI/RBO}}$	Output Short Circuit Current		−0.3		−2.0	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			7.0	13	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL} t_{PLH}	Propagation Delay, Address Input to Segment Output			100 100	ns ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, $\overline{\text{RBI}}$ Input To Segment Output			100 100	ns ns	

AC WAVEFORMS

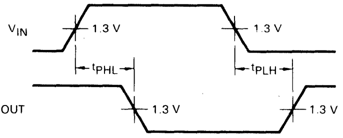


Fig. 1

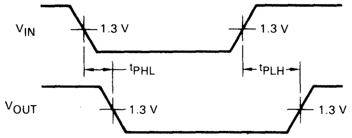


Fig. 2

MOTOROLA

SN54/74LS48

BCD TO 7-SEGMENT DECODER

LOW POWER SCHOTTKY

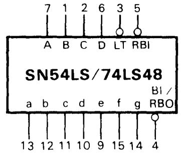
DESCRIPTION — The SN54LS/74LS48 is a BCD to 7-Segment Decoder consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the LS48.

The circuit accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

The LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

- **LAMP INTENSITY MODULATION CAPABILITY**
- **INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS**
- **INPUT CLAMP DIODES ELIMINATE HIGH-SPEED TERMINATION EFFECTS**

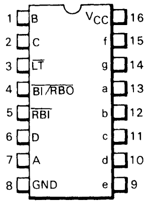
LOGIC SYMBOL



7 1 2 6 3 5
A B C D LT RBI
SN54LS/74LS48
BI/RBO
a b c d e f g
13 12 11 10 9 15 14 4

V_{CC} = Pin 16
GND = Pin 8

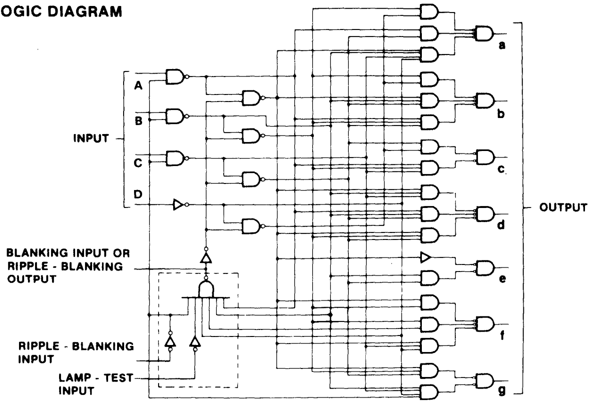
DIP (TOP VIEW)



1 B
2 C
3 LT
4 BI/RBO
5 RBI
6 D
7 A
8 GND
16 VCC
15 f
14 g
13 a
12 b
11 c
10 d
9 e

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

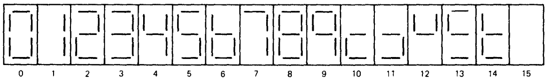
LOGIC DIAGRAM



A
B
C
D
INPUT
BLANKING INPUT OR RIPPLE - BLANKING OUTPUT
RIPPLE - BLANKING INPUT
LAMP - TEST INPUT
a
b
c
d
e
f
g
OUTPUT

PIN NAMES		**LOADING** (Note a) HIGH	**LOADING** (Note a) LOW
		0.5 U.L.	0.25 U.L.
A, B, C, D,	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{\text{RBI}}$	Ripple Blanking (Active Low) Input	0.5 U.L.	0.25 U.L.
$\overline{\text{LT}}$	Lamp Test (Active Low) Input	0.5 U.L.	0.75 U.L.
$\overline{\text{BI/RBO}}$	Blanking Input or Ripple	1.2 U.L.	2(1) U.L.
	Blanking Output (Active Low)	0.5 U.L.	0.25 U.L.
$\overline{\text{BI}}$	Blanking (Active Low) Input	Open Collector	3.75 (1.25) U.L. (48)

NOTES:
a) Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b) Output current measured at $V_{OUT} = 0.5$ V
Output LOW drive factor is SN54LS/74LS48: 1.25 U.L. for Military (54), 3.75 U.L. for Commercial (74).



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE
SN54LS/74LS48

DECIMAL OR FUNCTION	INPUTS $\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A	$\overline{\text{BI/RBO}}$	OUTPUTS a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L.	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{\text{LT}}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

(1) $\overline{\text{BI/RBO}}$ is wired-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out ($\overline{\text{BI}}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{\text{RBI}}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{\text{BI/RBO}}$) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High $\overline{a}$ to $\overline{g}$	54,74			−100	µA
I_{OH}	Output Current — High $\overline{BI}/\overline{RBO}$	54,74			−50	µA
I_{OL}	Output Current — Low $\overline{a}$ to $\overline{g}$	54 74			2.0 6.0	mA
I_{OL}	Output Current — Low $\overline{BI}/\overline{RBO}$ $\overline{BI}/\overline{RBO}$	54 74			1.6 3.2	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.4	4.2		µA	V_{CC} = MIN, I_{OH} = −50 µA, V_{IN} = V_{IH} or U.L. per Truth Table	
I_O	Output Current $\overline{a}$ to $\overline{g}$		-1.3	-2.0		mA	V_{CC} = MIN, V_O = 0.85 V Input Conditioner as for V_{OH}	
V_{OL}	Output LOW Voltage	54,74			0.4	V	I_{OL} = 2.0 mA	V_{CC}=MIN, V_{IH}=2.0 V
	$\overline{a}$ to $\overline{g}$	74			0.5	V	I_{OL} = 6.0 mA	V_{IL} = V_{IL} MAX
V_{OL}	Output LOW Voltage	54,74			0.4	V	I_{OL} = 1.6 mA	V_{CC}=MAX, V_{IH}=2.0 V
	$\overline{BI}/\overline{RBO}$	74			0.5	V	I_{OL} = 3.2 mA	V_{IL} = V_{IL} MAX
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	(Except $\overline{BI}/\overline{RBO}$)				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current (Except $\overline{BI}/\overline{RBO}$)				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IL}	Input LOW Current $\overline{BI}/\overline{RBO}$				−1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			25	38	mA	V_{CC} = MAX	
I_{OS}	Short Circuit Current $\overline{BI}/\overline{RBO}$		-0.3		-2.0	mA	V_{CC} = MAX	

AC CHARACTERISTICS: V_{CC} = 5.0 V T_A = 25°C

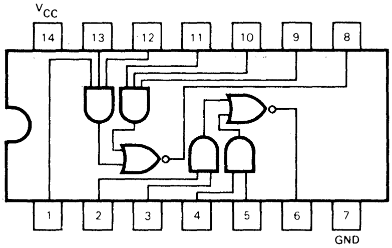
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from A Input			100	ns	C_L = 15 pF, R_L = 4.0 kΩ
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from A Input			100	ns	
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from $\overline{RBI}$ Input			100	ns	C_L = 15 pF, R_L = 6.0 kΩ
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from $\overline{RBI}$ Input			100	ns	

MOTOROLA

SN54/74LS51

DUAL 2-WIDE 2-INPUT/ 3-INPUT AND-OR-INVERT GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				 1.6 2.8	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

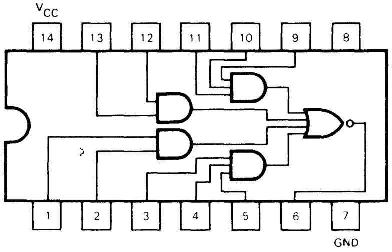
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		12	20	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay, Input to Output		12.5	20	ns	

MOTOROLA

SN54/74LS54

3-2-2-3-INPUT AND-OR-INVERT GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				1.6	mA	V_{CC} = MAX
	Total, Output LOW				2.0		

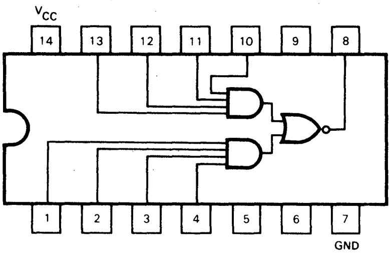
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		12	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		12.5	20	ns	C_L = 15 pF

SN54/74LS55

2-WIDE 4-INPUT AND-OR-INVERT GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				0.8	mA	V_{CC} = MAX	
	Total, Output LOW				1.3			

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		12	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		12.5	20	ns	C_L = 15 pF

MOTOROLA

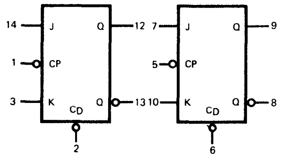
SN54/74LS73A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

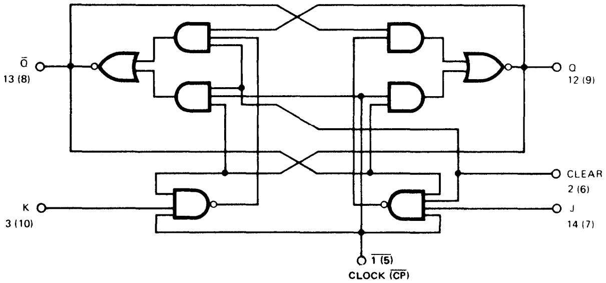
LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

LOGIC DIAGRAM (Each Flip-Flop)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Clear, Clock			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

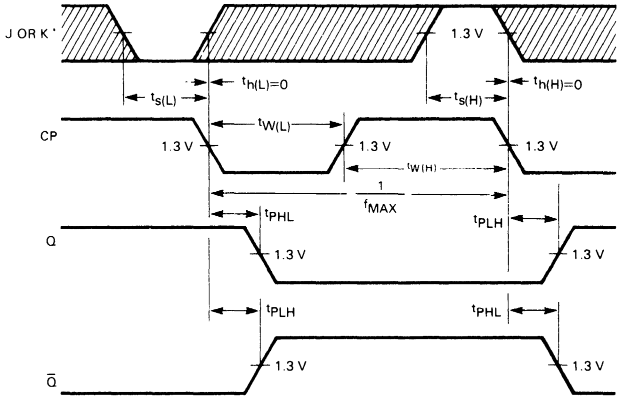
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$
t_{PLH}	Propagation Delay, Clock to Output		15	20	ns	Fig. 1	
t_{PHL}			15	20	ns		

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_W	Clock Pulse Width High	20			ns	Fig. 1	$V_{CC} = 5.0\ V$
t_W	Clear Pulse Width	25			ns	Fig. 2	
t_s	Setup Time	20			ns	Fig. 1	
t_h	Hold Time	0			ns		

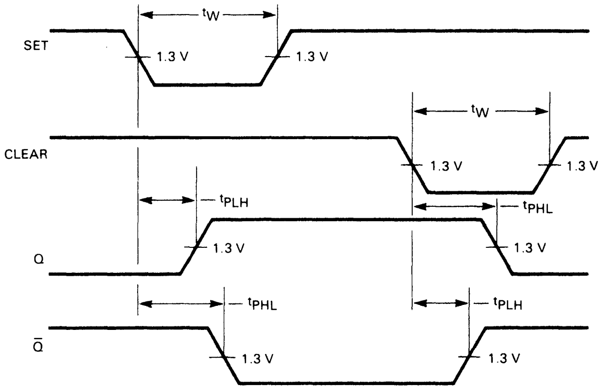
AC WAVEFORMS

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH


J OR K *
1.3 V
$t_{h(L)}=0$
$t_{s(L)}$
$t_{h(H)}=0$
$t_{s(H)}$
CP
1.3 V
$t_{W(L)}$
1.3 V
$t_{W(H)}$
1.3 V
$\frac{1}{f_{MAX}}$
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V
t_{PLH}
t_{PHL}
$\bar{Q}$
1.3 V
1.3 V

*The shaded areas indicate when the input is permitted to change for predicatable output performance.

Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS


t_W
SET
1.3 V
1.3 V
t_W
CLEAR
1.3 V
1.3 V
t_{PLH}
t_{PHL}
Q
1.3 V
1.3 V
t_{PHL}
t_{PLH}
$\bar{Q}$
1.3 V
1.3 V

MOTOROLA

SN54/74LS74A

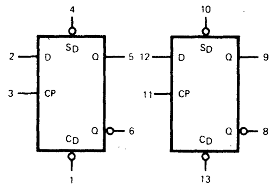
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION - The SN54LS/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

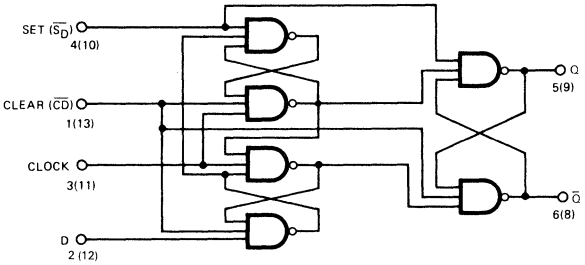
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

LOGIC DIAGRAM
(EACH FLIP-FLOP)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0$ mA	
I_{IH}	Input High Current Data, Clock Set, Clear				20 40	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
	Data, Clock Set, Clear				0.1 0.2	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current Data, Clock Set, Clear				−0.4 −0.8	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				8.0	mA	V_{CC} = MAX	

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS $\overline{S}_D$	INPUTS $\overline{C}_D$	INPUTS D	OUTPUTS Q	OUTPUTS $\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ AND $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

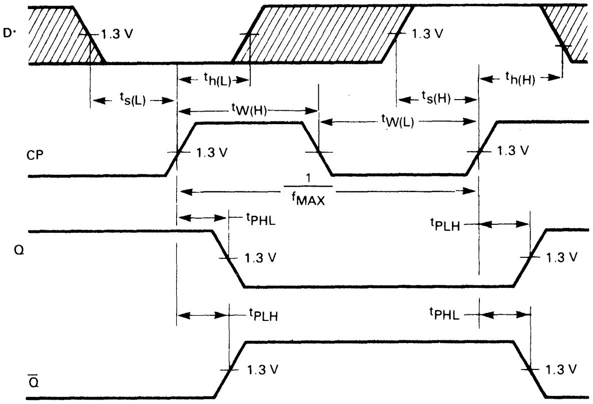
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	25	33		MHz	Fig. 1	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{PLH}	Clock, Clear, Set to Output		13	25	ns	Fig. 1	
t_{PHL}			25	40	ns		

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(H)}$	Clock	25			ns	Fig. 1	$V_{CC} = 5.0$ V
$t_{W(L)}$	Clear, Set	25			ns	Fig. 2	
t_s	Data Setup Time — HIGH	20			ns	Fig. 1	
	LOW	20			ns		
t_h	Hold Time	5.0			ns	Fig. 1	

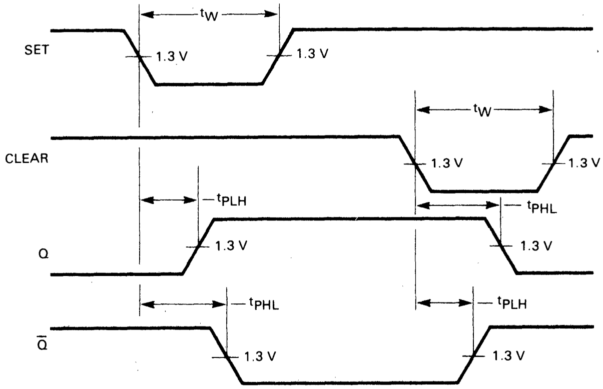
AC WAVEFORMS

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH


D*
1.3 V
1.3 V
$t_{h(L)}$
$t_{h(H)}$
$t_{s(L)}$
$t_{s(H)}$
$t_{W(H)}$
$t_{W(L)}$
CP
1.3 V
1.3 V
$\frac{1}{f_{MAX}}$
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V
t_{PLH}
t_{PHL}
$\overline{Q}$
1.3 V
1.3 V

*The shaded areas indicate when the input is permitted to change for predicatable output performance.

Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS


t_W
SET
1.3 V
1.3 V
t_W
CLEAR
1.3 V
1.3 V
t_{PLH}
t_{PHL}
Q
1.3 V
1.3 V
t_{PHL}
t_{PLH}
$\overline{Q}$
1.3 V
1.3 V

MOTOROLA

SN54/74LS75
SN54/74LS77

4-BIT D LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN54LS/74LS75 and SN54LS/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54LS/74LS75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54LS/74LS77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

PIN NAMES		LOADING (Note a) HIGH	LOADING (Note a) LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1–Q_4	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q_1}$–$\overline{Q_4}$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

Notes:
a. 1 Unit Load (U.L.) = 40 μA HIGH
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

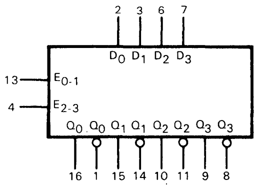
TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:
t_n = bit time before enable negative-going transition
t_{n+1} = bit time after enable negative-going transition

LOGIC SYMBOLS

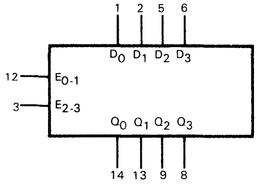
SN54LS/74LS75



2 3 6 7
D_0 D_1 D_2 D_3
13 E_{0-1}
4 E_{2-3}
Q_0 $\overline{Q}_0$ Q_1 $\overline{Q}_1$ Q_2 $\overline{Q}_2$ Q_3 $\overline{Q}_3$
16 1 15 14 10 11 9 8

V_{CC} = Pin 5
GND = Pin 12

SN54LS/74LS77

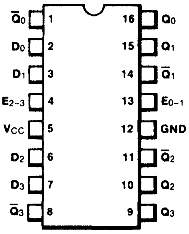


1 2 5 6
D_0 D_1 D_2 D_3
12 E_{0-1}
3 E_{2-3}
Q_0 Q_1 Q_2 Q_3
14 13 9 8

V_{CC} = Pin 4
GND = Pin 11
NC = Pin 7,10

CONNECTION DIAGRAMS
DIP (TOP VIEW)

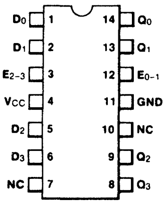
SN54LS/74LS75



$\overline{Q}_0$ 1
D_0 2
D_1 3
E_{2-3} 4
V_{CC} 5
D_2 6
D_3 7
$\overline{Q}_3$ 8
16 Q_0
15 Q_1
14 $\overline{Q}_1$
13 E_{0-1}
12 GND
11 $\overline{Q}_2$
10 Q_2
9 Q_3

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

SN54LS/74LS77



D_0 1
D_1 2
E_{2-3} 3
V_{CC} 4
D_2 5
D_3 6
NC 7
14 Q_0
13 Q_1
12 E_{0-1}
11 GND
10 NC
9 Q_2
8 Q_3

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	D Input E Input			20 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		D Input E Input			0.1 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	D Input E Input			−0.4 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				12	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		15 9.0	27 17	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Q}$		12 7.0	20 15	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		15 14	27 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$		16 7.0	30 15	ns	

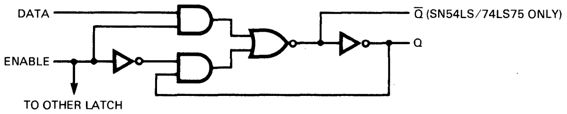
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	D Input E Input			20 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V
		D Input E Input			0.1 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	D Input E Input			−0.4 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				13	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		11 9.0	19 17	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		10 10	18 18	ns	

LOGIC DIAGRAM


DATA
ENABLE
TO OTHER LATCH
Q̄ (SN54LS/74LS75 ONLY)
Q

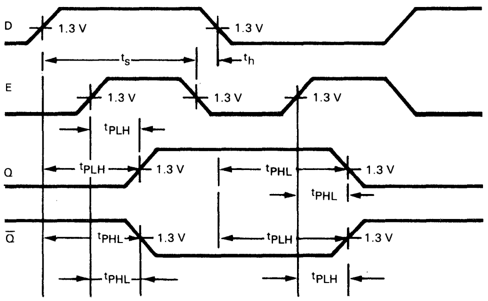
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Enable Pulse Width High	20			ns	$V_{CC} = 5.0$ V
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

AC WAVE FORMS


D
1.3 V
1.3 V
t_s
t_h
E
1.3 V
1.3 V
1.3 V
t_PLH
Q
t_PLH
1.3 V
t_PHL
1.3 V
t_PHL
Q̄
t_PHL
1.3 V
t_PLH
1.3 V
t_PHL
t_PLH

DEFINITION OF TERMS:

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

MOTOROLA

SN54/74LS76A

DUAL JK FLIP-FLOP WITH SET AND CLEAR

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

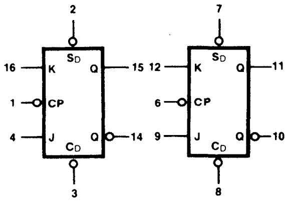
MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Immaterial
l,h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

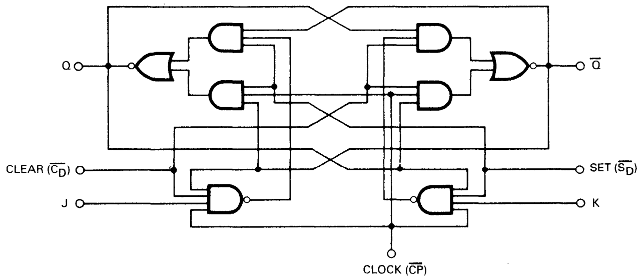
LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 13

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Clear, Clock			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Clock, Clear, Set to Output		15	20	ns	
t_{PHL}			15	20	ns	

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width High	20			ns	V_{CC} = 5.0 V
t_W	Clear Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

MOTOROLA

SN54/74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

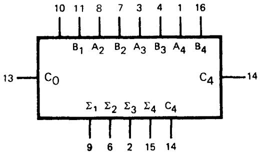
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 — A_4, B_1 — B_4) and a Carry Input (C_0). It generates the binary Sum outputs Σ_1 — Σ_4) and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54LS/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

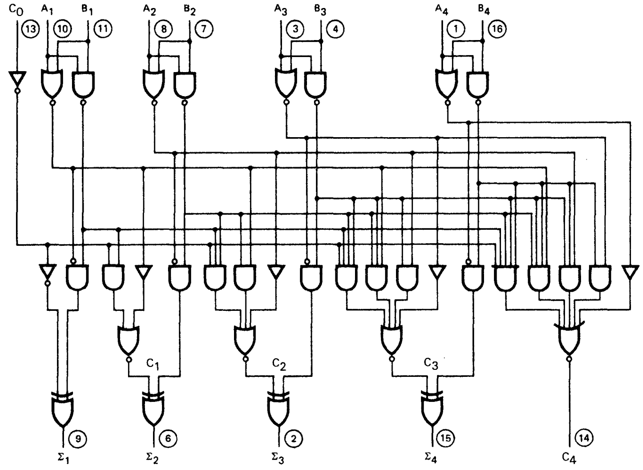
PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
A_1 — A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1 — B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
Σ_1 — Σ_4	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

LOGIC SYMBOL

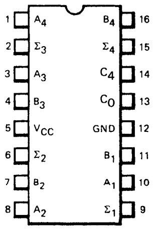

10 11 8 7 3 4 1 16
B_1 A_2 B_2 A_3 B_3 A_4 B_4
13
C_0
C_4
14
Σ_1 Σ_2 Σ_3 Σ_4 C_4
9 6 2 15 14

LOGIC DIAGRAM


C_0 A_1 B_1
13 10 11
A_2 B_2
8 7
A_3 B_3
3 4
A_4 B_4
1 16
C_1
C_2
C_3
9
Σ_1
6
Σ_2
2
Σ_3
15
Σ_4
14
C_4

V_{CC} = Pin 5
GND = Pin 12
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)


1 A_4
2 Σ_3
3 A_3
4 B_3
5 V_{CC}
6 Σ_2
7 B_2
8 A_2
16 B_4
15 Σ_4
14 C_4
13 C_0
12 GND
11 B_1
10 A_1
9 Σ_1

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 — Σ_4) and outgoing carry (C_4) outputs.

$$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

C(n-1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current C_0 A or B				 20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	C_0 A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current C_0 A or B				 −0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current All Inputs Grounded All Inputs at 4.5 V, Except B All Inputs at 4.5 V				 39 34 34	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 15	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

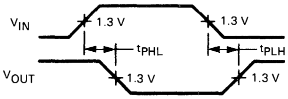


Fig. 1

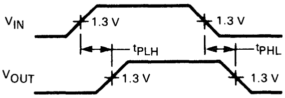


Fig. 2

MOTOROLA

SN54/74LS85

4-BIT MAGNITUDE COMPARATOR

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3, B_0-B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54LS/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

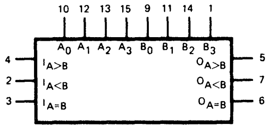
PIN NAMES		**LOADING** (Note a) HIGH	LOW
A_0-A_3, B_0-B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A<B}$	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A=B}$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

Notes:

a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

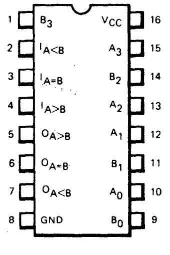
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


10
12
13
15
9
11
14
1
A_0
A_1
A_2
A_3
B_0
B_1
B_2
B_3
4
$I_{A>B}$
2
$I_{A<B}$
3
$I_{A=B}$
$O_{A>B}$
5
$O_{A<B}$
7
$O_{A=B}$
6

V_{CC} = Pin 16
GND = Pin 8

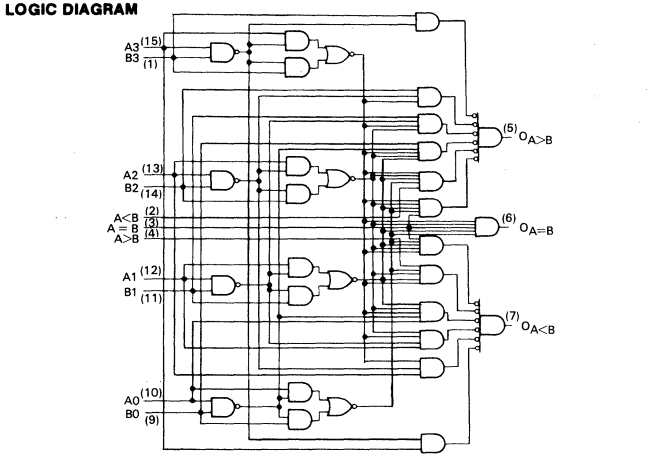
CONNECTION DIAGRAM
DIP (TOP VIEW)


1
B_3
2
$I_{A<B}$
3
$I_{A=B}$
4
$I_{A>B}$
5
$O_{A>B}$
6
$O_{A=B}$
7
$O_{A<B}$
8
GND
16
V_{CC}
15
A_3
14
B_2
13
A_2
12
A_1
11
B_1
10
A_0
9
B_0

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


A3 (15)
B3 (1)
A2 (13)
B2 (14)
A<B (2)
A=B (3)
A>B (4)
A1 (12)
B1 (11)
A0 (10)
B0 (9)
(5) $O_{A>B}$
(6) $O_{A=B}$
(7) $O_{A<B}$

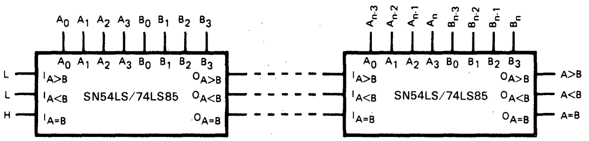
TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA



A0 A1 A2 A3 B0 B1 B2 B3
An-3 An-2 An-1 An Bn-3 Bn-2 Bn-1 Bn
L
L
H
IA>B
IA<B
IA=B
SN54LS/74LS85
OA>B
OA<B
OA=B
A>B
A<B
A=B

L = LOW Level
H = HIGH Level

Fig. 1. COMPARING TWO n-BIT WORDS

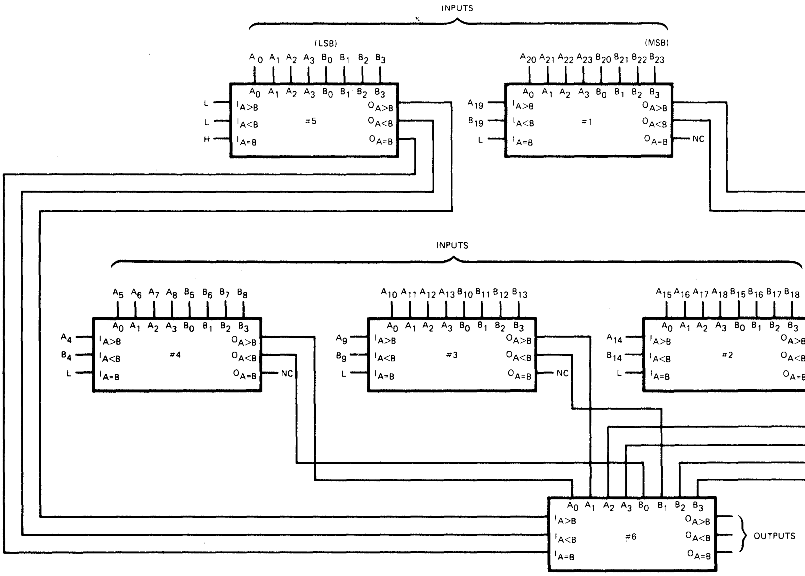
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The SN54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another SN54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.



INPUTS
(LSB)
(MSB)
A0 A1 A2 A3 B0 B1 B2 B3
A20 A21 A22 A23 B20 B21 B22 B23
#5
#1
A19
B19
L
L
H
NC
INPUTS
A5 A6 A7 A8 B5 B6 B7 B8
A10 A11 A12 A13 B10 B11 B12 B13
A15 A16 A17 A18 B15 B16 B17 B18
A4
B4
A9
B9
A14
B14
#4
#3
#2
NC
IA>B
IA<B
IA=B
OA>B
OA<B
OA=B
#6
OUTPUTS

MSB = Most Significant Bit
LSB = Least Significant Bit
L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current A<B, A>B Other Inputs				20 60	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	A<B, A>B Other Inputs				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current A<B, A>B Other Inputs				−0.4 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				20	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Any A or B to A < B, A > B		24 20	36 30	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Any A or B to A = B		27 23	45 45	ns	
t_{PLH} t_{PHL}	A < B or A = B to A > B		14 11	22 17	ns	
t_{PLH} t_{PHL}	A = B to A = B		13 13	20 26	ns	
t_{PLH} t_{PHL}	A > B or A = B to A < B		14 11	22 17	ns	

AC WAVEFORMS

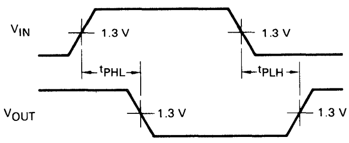


Fig. 3

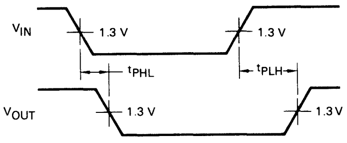


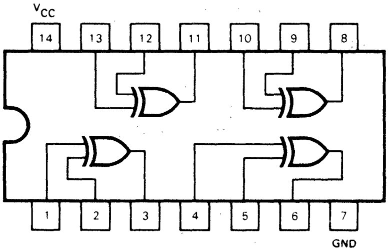
Fig. 4

MOTOROLA

SN54/74LS86

QUAD 2-INPUT EXCLUSIVE OR GATE

LOW POWER SCHOTTKY



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		12 10	23 17	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		20 13	30 22	ns	

MOTOROLA

SN54/74LS90
SN54/74LS92
SN54/74LS93

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

LOW POWER SCHOTTKY

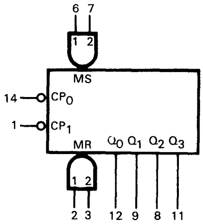
DESCRIPTION — The SN54LS/74LS90, SN54LS/74LS92 and SN54LS/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggerd by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

- **LOW POWER CONSUMPTION . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . TYPICALLY 42 MHz**
- **CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

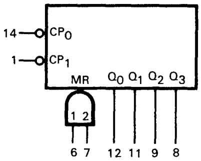
LOGIC SYMBOL

LS90



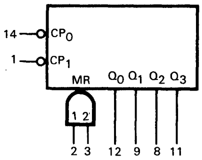
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

LS92



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

LS93



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

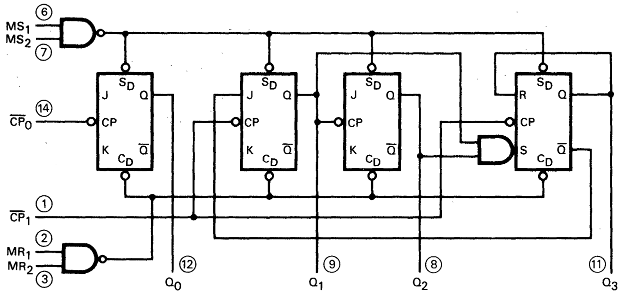
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5(2.5) U.L.

Notes:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

LOGIC DIAGRAM

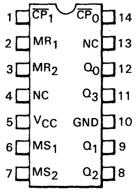
LS90



MS1
MS2
⑥
⑦
⑭
CP0
CP1
①
MR1
MR2
②
③
SD
J
Q
CP
K
CD
Q
R
S
⑫
Q0
⑨
Q1
⑧
Q2
⑪
Q3

○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



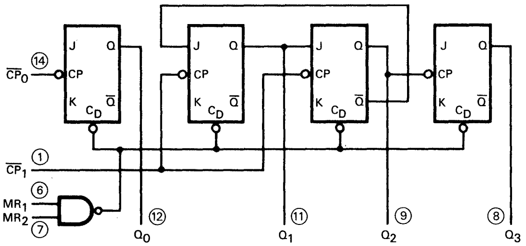
1 CP1
2 MR1
3 MR2
4 NC
5 VCC
6 MS1
7 MS2
14 CP0
13 NC
12 Q0
11 Q3
10 GND
9 Q1
8 Q2

NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM

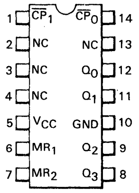
LS92



⑭
CP0
①
CP1
⑥
MR1
MR2
⑦
J
Q
CP
K
CD
Q
⑫
Q0
⑪
Q1
⑨
Q2
⑧
Q3

○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



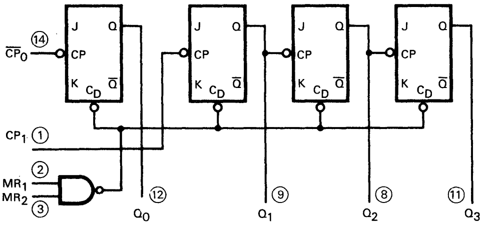
1 CP1
2 NC
3 NC
4 NC
5 VCC
6 MR1
7 MR2
14 CP0
13 NC
12 Q0
11 Q1
10 GND
9 Q2
8 Q3

NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM

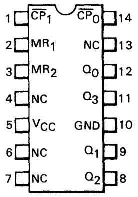
LS93



⑭
CP0
CP1 ①
②
MR1
MR2
③
J
Q
CP
K
CD
Q
⑫
Q0
⑨
Q1
⑧
Q2
⑪
Q3

○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 CP1
2 MR1
3 MR2
4 NC
5 VCC
6 NC
7 NC
14 CP0
13 NC
12 Q0
11 Q3
10 GND
9 Q1
8 Q2

NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90 BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input $\overline{CP}_1$ for BCD count.

LS92 TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$.

LS93 TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0$ mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS90, LS92) $\overline{CP}_1$ (LS93)				 −0.4 −2.4 −3.2 −1.6	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS									UNITS
		LS90			LS92			LS93			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	$\overline{CP}_0$ Input Clock Frequency	32			32			32			MHz
f_{MAX}	$\overline{CP}_1$ Input Clock Frequency	16			16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		20	30							ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40							ns
t_{PHL}	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS						UNITS
		LS90		LS92		LS93		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns
t_W	MS Pulse Width	15						ns
t_W	MR Pulse Width	15		15		15		ns
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVE FORMS

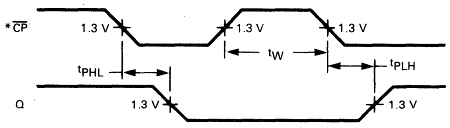


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

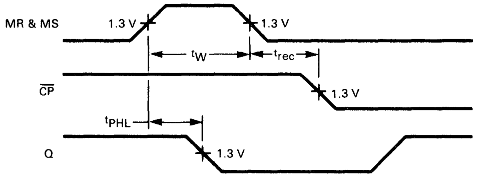


Fig. 2

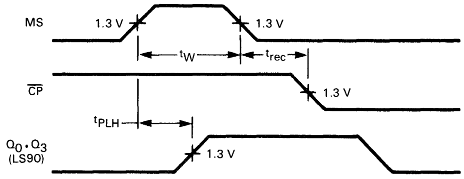


Fig. 3

MOTOROLA

SN54/74LS95B

4-BIT SHIFT REGISTER

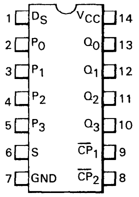
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SYNCHRONOUS, EXPANDABLE SHIFT RIGHT
- SYNCHRONOUS SHIFT LEFT CAPABILITY
- SYNCHRONOUS PARALLEL LOAD
- SEPARATE SHIFT AND LOAD CLOCK INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{CC} = Pin 14
GND = Pin 7

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

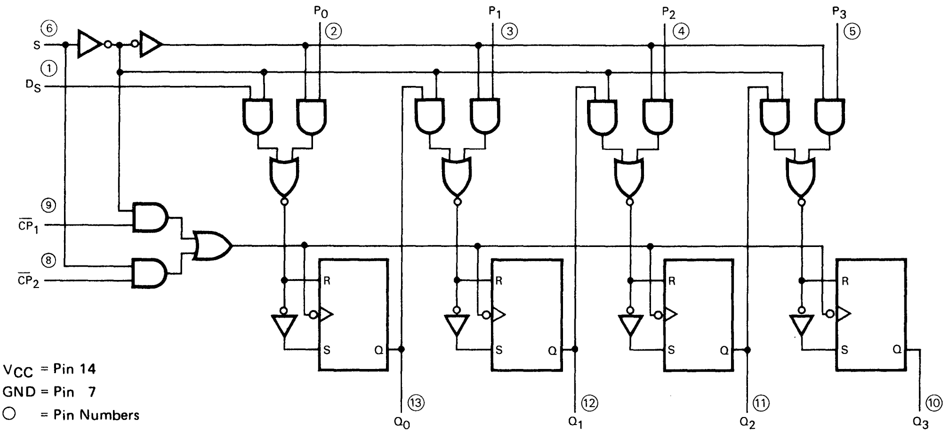
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOADING (Note a) LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 — P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$Q_0 — Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5)U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0 — P_3) Data inputs and four Parallel Data outputs (Q_0 — Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the P_0 — P_3 inputs to the Q_0 — Q_3 outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	┐	X	l	X	L	q_0	q_1	q_2
	L	┐	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	┐	X	p_n	p_0	p_1	p_2	p_3
Mode Change	┐	L	L	X	X	No Change			
	┌	L	L	X	X	No Change			
	┐	H	L	X	X	No Change			
	┌	H	L	X	X	Undetermined			
	┐	L	H	X	X	Undetermined			
	┌	L	H	X	X	No Change			
	┐	H	H	X	X	Undetermined			
	┌	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA $V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0$ mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				21	mA	V_{CC} = MAX

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Clock Frequency	25	36		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	$\overline{CP}$ to Output		18	27	ns	
t_{PHL}			21	32	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	$\overline{CP}$ Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	20			ns	
t_s	Mode Control Setup Time	20			ns	
t_h	Mode Control Hold Time	20			ns	

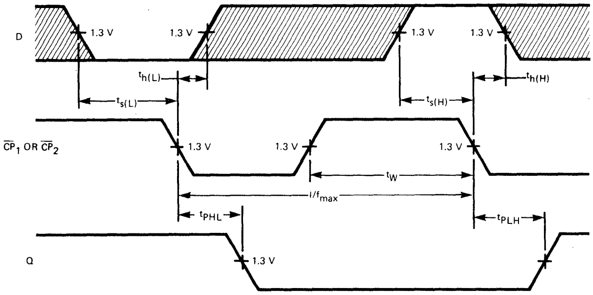
DESCRIPTIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.


D
1.3 V
1.3 V
1.3 V
1.3 V
$t_{h(L)}$
$t_{h(H)}$
$t_{s(L)}$
$t_{s(H)}$
$\overline{CP}_1$ OR $\overline{CP}_2$
1.3 V
1.3 V
1.3 V
t_W
$1/f_{max}$
t_{PHL}
t_{PLH}
Q
1.3 V

*The Data Input is (D_S for $\overline{CP_1}$) or (P_n for $\overline{CP_2}$).

Fig. 1

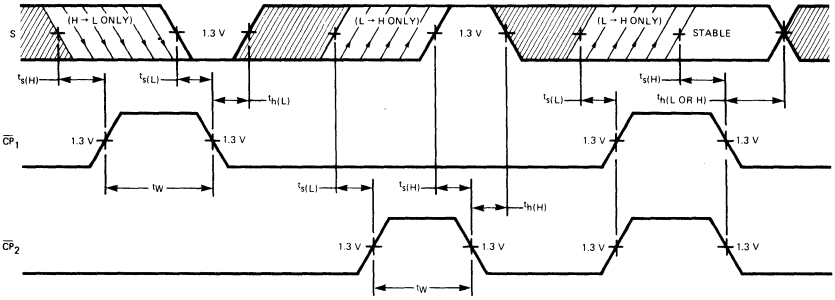

S
(H → L ONLY)
1.3 V
(L → H ONLY)
1.3 V
(L → H ONLY)
STABLE
$t_{s(H)}$
$t_{s(L)}$
$t_{h(L)}$
$t_{s(L)}$
$t_{s(H)}$
$t_{h(L OR H)}$
$\overline{CP}_1$
1.3 V
1.3 V
1.3 V
1.3 V
t_W
$t_{s(L)}$
$t_{s(H)}$
$t_{h(H)}$
$\overline{CP}_2$
1.3 V
1.3 V
1.3 V
1.3 V
t_W

Fig. 2

MOTOROLA

SN54/74LS107A

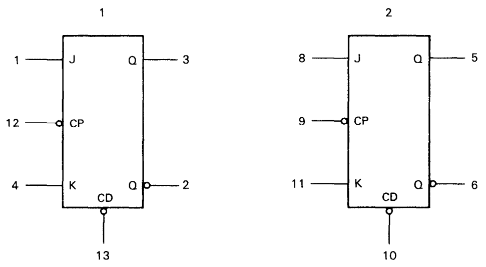
DUAL JK FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS107A is a Dual JK Flip-Flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH-to-LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

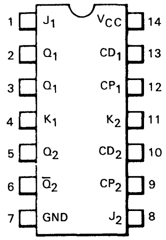
The SN54LS/74LS107A is the same as the SN54LS/74LS73A but has corner power pins.

LOGIC SYMBOL


1
2
1
J
Q
3
12
CP
4
K
Q
2
CD
13
8
J
Q
5
9
CP
11
K
Q
6
CD
10

V_{CC} = 14
GND = 7

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
J1
VCC
14
2
Q1
CD1
13
3
Q1
CP1
12
4
K1
K2
11
5
Q2
CD2
10
6
Q̄2
CP2
9
7
GND
J2
8

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		Clear			60			
		Clock			80			
		J, K			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		Clear			0.3			
		Clock			0.4			
I_{IL}	Input LOW Current	J, K			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Clear and Clock			−0.8			
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Propagation Delay,		15	20	ns	
t_{PHL}	Clock to Output		15	20	ns	

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	20			ns	V_{CC} = 5.0 V
t_W	Clear Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

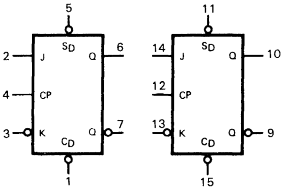
SN54/74LS109A

DESCRIPTION — The SN54LS/74LS109A consists of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

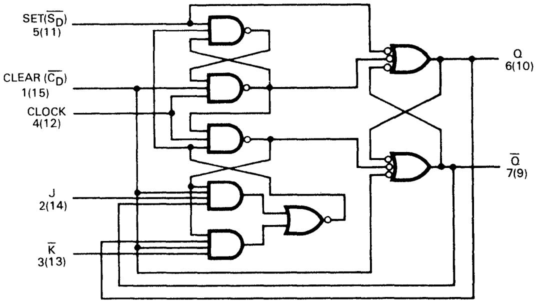
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current J, $\overline{K}$, Clock Set, Clear				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	J, $\overline{K}$, Clock Set, Clear				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current J, $\overline{K}$, Clock Set, Clear				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				8.0	mA	V_{CC} = MAX	

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	33		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Clock, Clear, Set to Output		13	25	ns	
t_{PHL}			25	40	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock High Clear, Set Pulse Width	25			ns	$V_{CC} = 5.0$ V
t_s	Data Setup Time — HIGH	35			ns	
	LOW	25			ns	
t_h	Hold Time	5.0			ns	

MOTOROLA

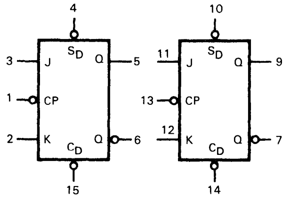
SN54/74LS112A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

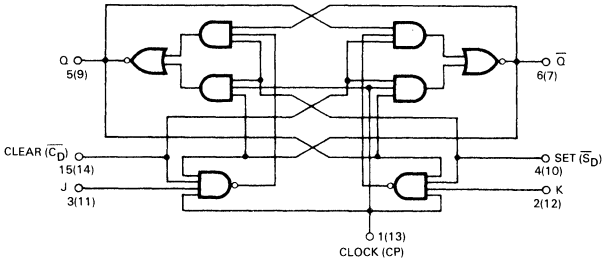
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

LOGIC DIAGRAM
(EACH FLIP-FLOP)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	J, K Set, Clear Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V
		J, K Set, Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	J, K Clear,Set,Clk			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25°C, V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$
t_{PLH}	Propagation Delay, Clock		15	20	ns	
t_{PHL}	Clear, Set to Output		15	20	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C, V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width High	20			ns	$V_{CC} = 5.0\ V$
t_W	Clear, Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

MOTOROLA

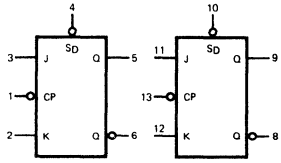
SN54/74LS113A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

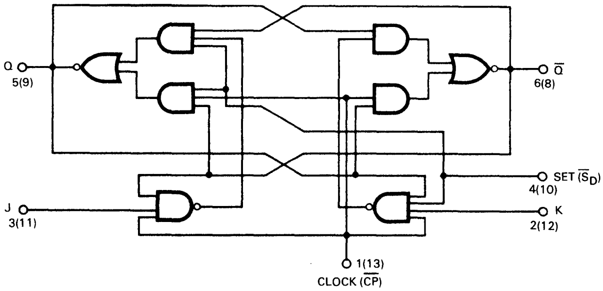
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

LOGIC DIAGRAM
(EACH FLIP-FLOP)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Set Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Set Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Set, Clock			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Propagation Delay, Clock		15	20	ns	
t_{PHL}	Set to Output		15	20	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width High	20			ns	$V_{CC} = 5.0$ V
t_W	Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

MOTOROLA

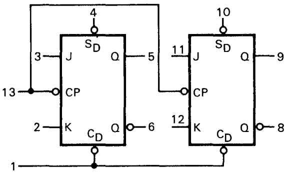
SN54/74LS114A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS114A offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

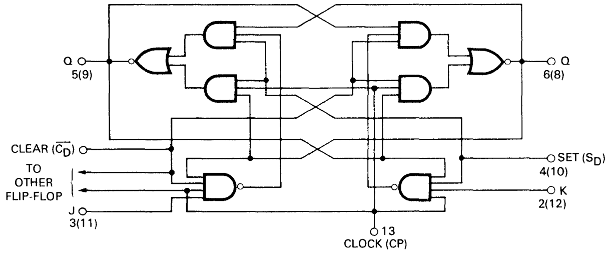
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

LOGIC DIAGRAM
(EACH FLIP-FLOP)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	J, K Set Clear Clock			20 60 120 160	µA	V_{CC} = MAX, V_{IN} = 2.7 V
		J, K Set Clear Clock			0.1 0.3 0.6 0.8	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	J, K Set Clear, Clock			−0.4 −0.8 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Propagation Delay, Clock,		15	20	ns	
t_{PHL}	Clear, Set to Output		15	20	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width High	20			ns	$V_{CC} = 5.0$ V
t_W	Clear, Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

MOTOROLA

SN54/74LS122
SN54/74LS123

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

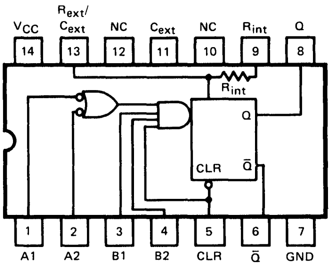
LOW POWER SCHOTTKY

DESCRIPTION — These d-c triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

The LS122 and LS123 have Schmitt trigger inputs to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

- **OVERRIDING CLEAR TERMINATES OUTPUT PULSE**
- **COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **D-C TRIGGERED FROM ACTIVE-HIGH OR ACTIVE-LOW GATED LOGIC INPUTS**
- **RETRIGGERABLE FOR VERY LONG OUTPUT PULSES, UP TO 100% DUTY CYCLE**
- **INTERNAL TIMING RESISTORS ON LS122**

SN54LS/74LS122
(TOP VIEW) (SEE NOTES 1 THRU 4)



V_{CC}
R_{ext}/C_{ext}
NC
C_{ext}
NC
R_{int}
Q
14
13
12
11
10
9
8
R_{int}
Q
CLR
$\bar{Q}$
1
2
3
4
5
6
7
A1
A2
B1
B2
CLR
$\bar{Q}$
GND

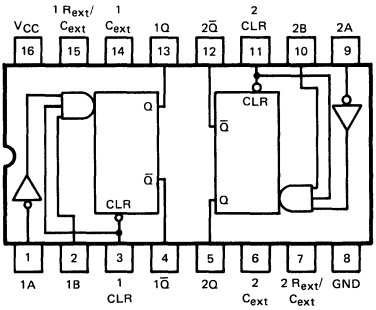
J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NC — NO internal connection.

LS122
FUNCTIONAL TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

SN54LS/74LS123
(TOP VIEW) (SEE NOTES 1 THRU 4)



V_{CC}
1 R_{ext}/C_{ext}
1 C_{ext}
1Q
$2\bar{Q}$
2 CLR
2B
2A
16
15
14
13
12
11
10
9
Q
$\bar{Q}$
CLR
CLR
$\bar{Q}$
Q
1
2
3
4
5
6
7
8
1A
1B
1 CLR
$1\bar{Q}$
2Q
2 C_{ext}
2 R_{ext}/C_{ext}
GND

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

LS123
FUNCTIONAL TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

NOTES:

1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of the LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int}/C_{ext} and V_{CC}.

TYPICAL APPLICATION DATA

The output pulse t_W is a function of the external components, C_{ext} and R_{ext} or C_{ext} and R_{int} on the LS122. For values of $C_{ext} \geqslant 1000$ pF, the output pulse at $V_{CC} = 5.0$ V and $V_{RC} = 5.0$ V (see Figures 1, 2, and 3) is given by

$t_W = K\, R_{ext}\, C_{ext}$ where K is nominally 0.45

If C_{ext} is on pF and R_{ext} is in kΩ then t_W is in nanoseconds.

The C_{ext} terminal of the LS122 and LS123 is an internal connection to ground, however for the best system performance C_{ext} should be hard-wired to ground.

Care should be taken to keep R_{ext} and C_{ext} as close to the monostable as possible with a minimum amount of inductance between the R_{ext}/C_{ext} junction and the R_{ext}/C_{ext} pin. Good groundplane and adequate bypassing should be designed into the system for optimum performance to insure that no false triggering occurs.

It should be noted that the C_{ext} pin is internally connected to ground on the LS122 and LS123, but not on the LS221. Therefore, if C_{ext} is hard-wired externally to ground, substitution of a LS221 onto a LS123 socket will cause the LS221 to become non-functional.

The switching diode is not needed for electrolytic capacitance application and should not be used on the LS122 and LS123.

To find the value of K for $C_{ext} \geqslant 1000$ pF, refer to Figure 4. Variations on V_{CC} or V_{RC} can cause the value of K to change, as can the temperature of the LS123, LS122. Figures 5 and 6 show the behaviour of the circuit shown in Figures 1 and 2 if separate power supplies are used for V_{CC} and V_{RC}. If V_{CC} is tied to V_{RC}, Figure 7 shows how K will vary with V_{CC} and temperature. Remember, the changes in R_{ext} and C_{ext} with temperature are not calculated and included in the graph.

As long as $C_{ext} \geqslant 1000$ pF and $5K \leqslant R_{ext} \leqslant 260$ K (SN74LS122/123) or $5K \leqslant R_{ext} \leqslant 160$ K (SN54LS122/123), the change in K with respect to R_{ext} is negligable.

If $C_{ext} \leqslant 1000$ pF the graph shown on Figure 8 can be used to determine the output pulse width. Figure 9 shows how K will change for $C_{ext} \leqslant 1000$ pF if V_{CC} and V_{RC} are connected to the same power supply. The pulse width t_W in nanoseconds is approximated by

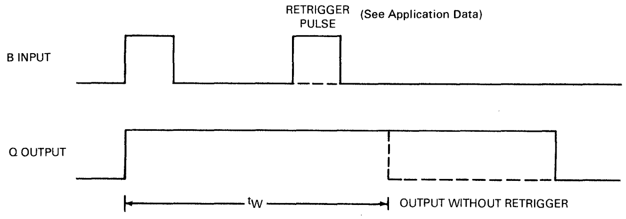
$t_W = 6 + 0.05\, C_{ext}\,(\text{pF}) + 0.45\, R_{ext}\,(\text{k}\Omega)\, C_{ext} + 11.6\, R_{ext}$

In order to trim the output pulse width, it is necessary to include a variable resistor between V_{CC} and the R_{ext}/C_{ext} pin or between V_{CC} and the R_{ext} pin of the LS122. Figure 10, 11, and 12 show how this can be done. R_{ext} remote should be kept as close to the monostable as possible.

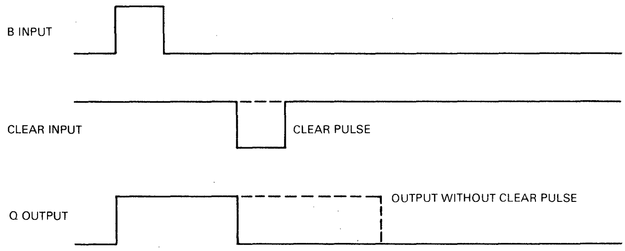
Retriggering of the part, as shown in Figure 3, must not occur before C_{ext} is discharged or the retrigger pulse will not have any effect. The discharge time of C_{ext} in nanoseconds is guaranteed to be less than 0.22 C_{ext} (pF) and is typically 0.05 C_{ext} (pF).

For the smallest possible deviation in output pulse widths from various devices, it is suggested that C_{ext} be kept $\geqslant 1000$ pF.

WAVEFORMS



EXTENDING PULSE WIDTH



OVERRIDING THE OUTPUT PULSE

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	
R_{ext}	External Timing Resistance	54	5.0		180	kΩ
		74	5.0		260	
C_{ext}	External Capacitance	54,74	No Restriction			
R_{ext}/C_{ext}	Wiring Capacitance at R_{ext}/C_{ext} Terminal	54,74			50	pF

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current	LS122			11	mA	V_{CC} = MAX
		LS123			20		

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A to Q		23	33	ns	C_{ext} = 0 C_L = 15 pF R_{ext} = 5.0 kΩ R_L = 2.0 kΩ
t_{PHL}	Propagation Delay, A to $\overline{Q}$		32	45		
t_{PLH}	Propagation Delay, B to Q		23	44	ns	
t_{PHL}	Propagation Delay, B to $\overline{Q}$		34	56		
t_{PLH}	Propagation Delay, Clear to $\overline{Q}$		28	45	ns	
t_{PHL}	Propagation Delay, Clear to Q		20	27		
$t_{W\ min}$	A or B to Q		116	200	ns	
t_{WQ}	A to B to Q	4.0	4.5	5.0	µs	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 2.0 kΩ

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
t_W	Pulse Width	40			ns

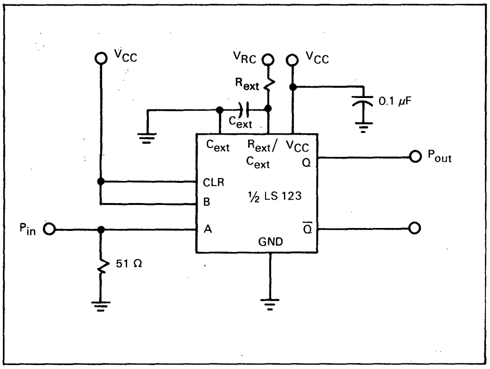

VCC
VRC
VCC
Rext
0.1 μF
Cext
Cext
Rext/Cext
VCC
Q
Pout
CLR
B
½ LS 123
Pin
A
Q̄
GND
51 Ω

Fig. 1

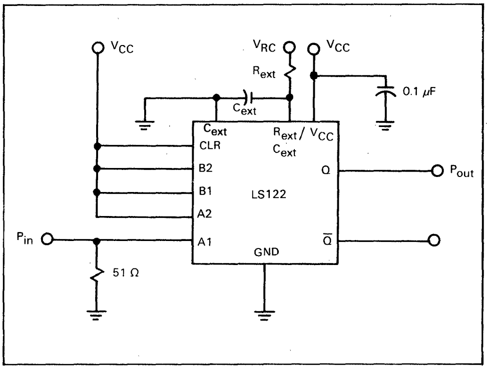

VCC
VRC
VCC
Rext
0.1 μF
Cext
Cext
CLR
Rext/VCC
Cext
B2
Q
Pout
B1
LS122
A2
Pin
A1
GND
Q̄
51 Ω

Fig. 2

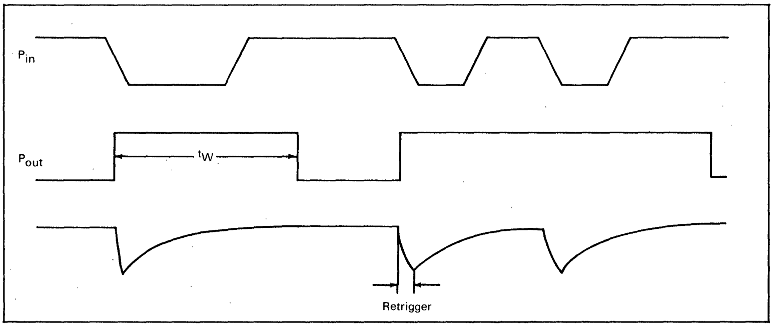

Pin
Pout
tW
Retrigger

Fig. 3

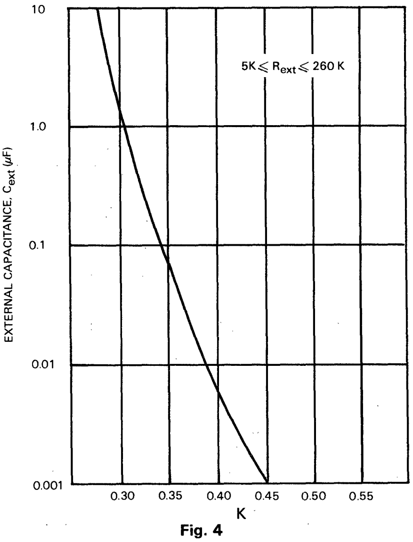


Fig. 4

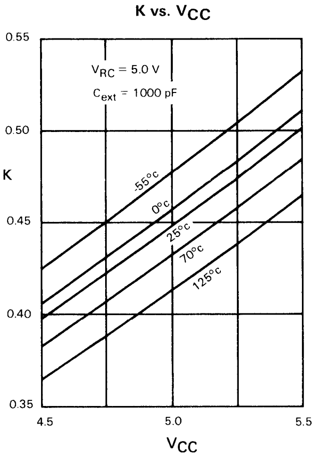


Fig. 5

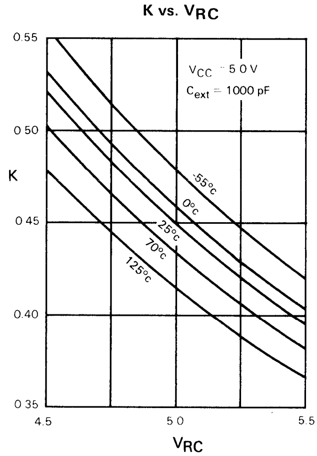


Fig. 6

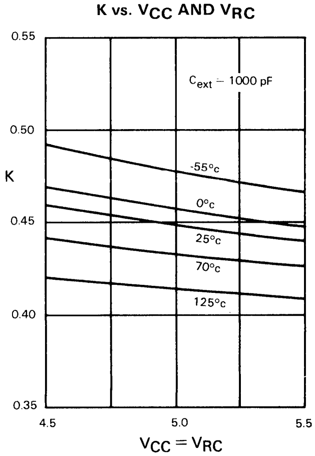


Fig. 7

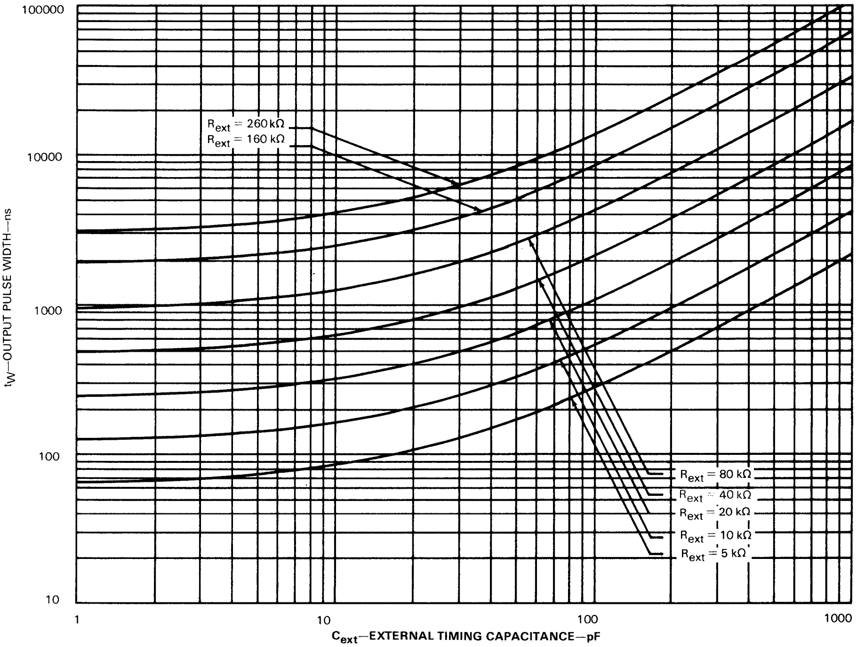


Fig. 8

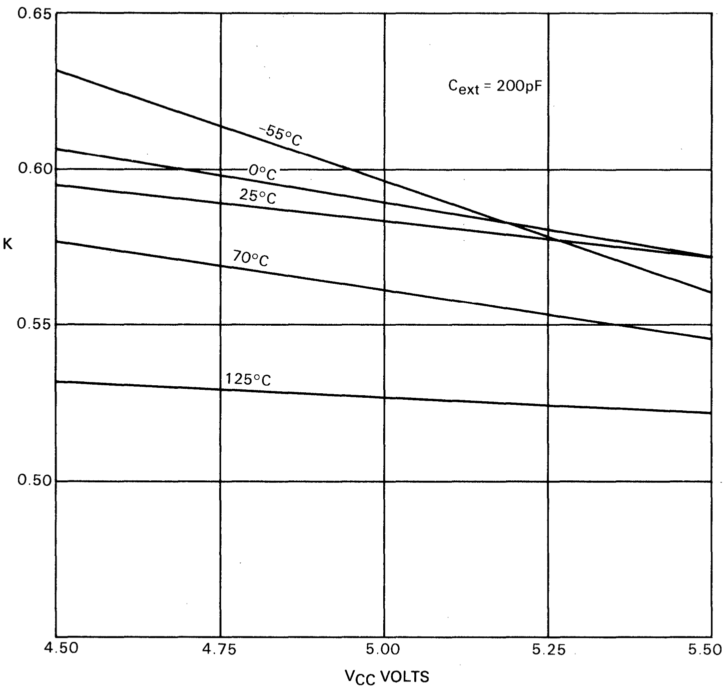


Fig. 9

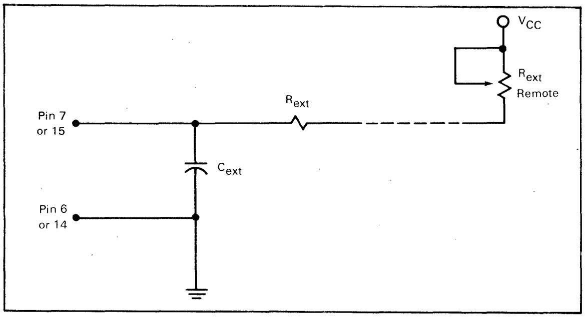

V_{CC}
R_{ext}
Remote
R_{ext}
Pin 7
or 15
C_{ext}
Pin 6
or 14

Fig. 10 — LS123 REMOTE TRIMMING CIRCUIT

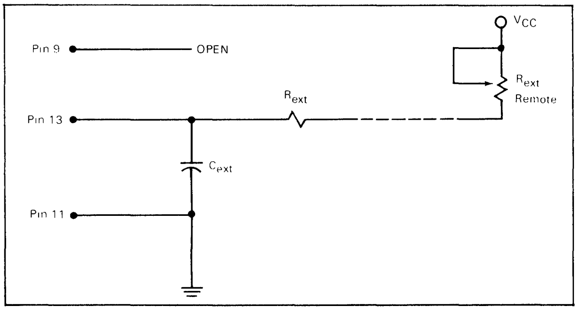

Pin 9
OPEN
Pin 13
Pin 11
R_{ext}
C_{ext}
V_{CC}
R_{ext}
Remote

Fig. 11—LS122 REMOTE TRIMMING CIRCUIT WITHOUT R_{ext}

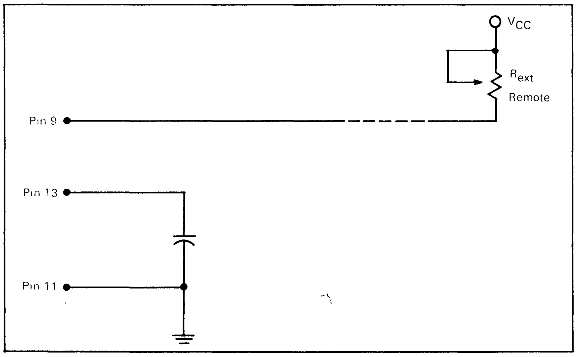

V_{CC}
R_{ext}
Remote
Pin 9
Pin 13
Pin 11

Fig. 12—LS122 REMOTE TRIMMING CIRCUIT WITH R_{int}

MOTOROLA

SN54/74LS125A
SN54/74LS126A

QUAD 3-STATE BUFFERS

LOW POWER SCHOTTKY

TRUTH TABLES

LS125A

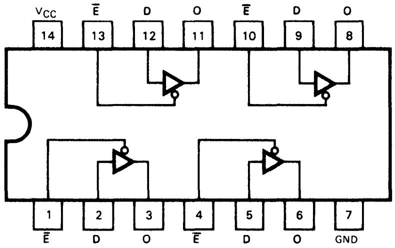
INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS126A

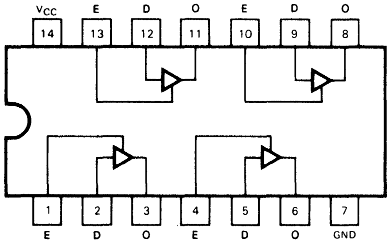
INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)



LS125A



LS126A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4			V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4			V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.4 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4V	
I_{OS}	Short Circuit Current		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current	LS125A			20	mA	V_{CC} = MAX,	V_{IN} = 0 V, V_E = 4.5 V
		LS126A			22			V_{IN} = 0 V, V_E = 0 V

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
t_{PLH}	Propagation Delay, Data to Output	LS125A		9.0	15	ns	Fig. 2	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH}		LS126A		9.0	15			
t_{PHL}		LS125A		7.0	18			
t_{PHL}		LS126A		8.0	18			
t_{PZH}	Output Enable Time to HIGH Level	LS125A		12	20	ns	Figs. 4, 5	
		LS126A		16	25			
t_{PZL}	Output Enable Time to LOW Level	LS125A		15	25	ns	Figs. 3, 5	
		LS126A		21	35			
t_{PHZ}	Output Disable Time from HIGH Level	LS125A			20	ns	Figs. 4, 5	$V_{CC} = 5.0$ V $C_L = 5.0$ pF $R_L = 667\ \Omega$
		LS126A			25			
t_{PLZ}	Output Disable Time from LOW Level	LS125A			20	ns	Figs. 3, 5	
		LS126A			25			

Fig. 1

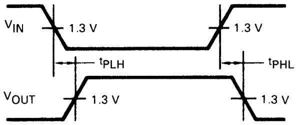

VIN
1.3 V
1.3 V
tPLH
tPHL
VOUT
1.3 V
1.3 V

Fig. 2

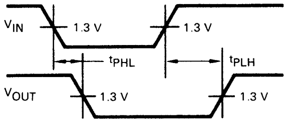

VIN
1.3 V
1.3 V
tPHL
tPLH
VOUT
1.3 V
1.3 V

Fig. 3

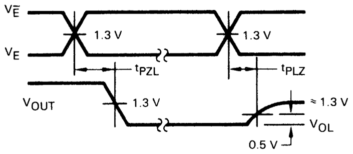

VĒ
VE
1.3 V
1.3 V
tPZL
tPLZ
VOUT
1.3 V
≈ 1.3 V
VOL
0.5 V

Fig. 4

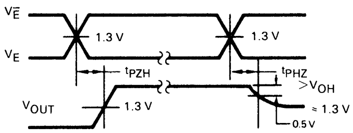
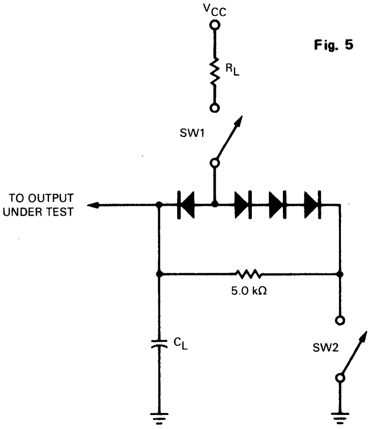

VĒ
VE
1.3 V
1.3 V
tPZH
tPHZ
>VOH
VOUT
1.3 V
≈ 1.3 V
0.5V

Fig. 5


VCC
RL
SW1
TO OUTPUT UNDER TEST
5.0 kΩ
CL
SW2

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SN54/74LS132

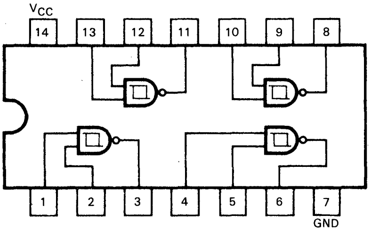
QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

V_{IN} VERSUS V_{OUT} TRANSFER FUNCTION

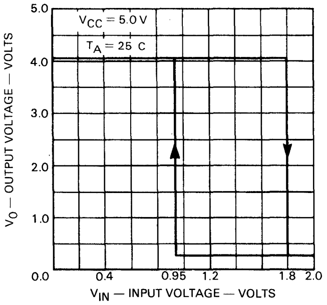


Fig. 1

GUARANTEED OPERATING RANGES

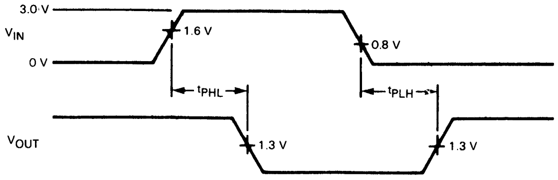
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{T+}	Positive-Going Threshold Voltage		1.5		2.0	V	$V_{CC} = 5.0$ V
V_{T-}	Negative-Going Threshold Voltage		0.6		1.1	V	$V_{CC} = 5.0$ V
V_{T+}-V_{T-}	Hysteresis		0.4	0.8		V	$V_{CC} = 5.0$ V
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, $I_{OH} = -400\mu A$, $V_{IN} = V_{IL}$
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, $I_{OL} = 4.0$ mA, $V_{IN} = 2.0$ V
		74		0.35	0.5	V	V_{CC} = MIN, $I_{OL} = 8.0$ mA, $V_{IN} = 2.0$ V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T+}$
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T-}$
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX, $V_{OUT} = 0$ V
I_{CC}	Power Supply Current Total, Output HIGH			5.9	11	mA	V_{CC} = MAX, $V_{IN} = 0$ V
	Total, Output LOW			8.2	14	mA	V_{CC} = MAX, $V_{IN} = 4.5$ V

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output			22	ns	$V_{CC} = 5.0$ V
t_{PHL}	Turn On Delay, Input to Output			22	ns	$C_L = 15$ pF



THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

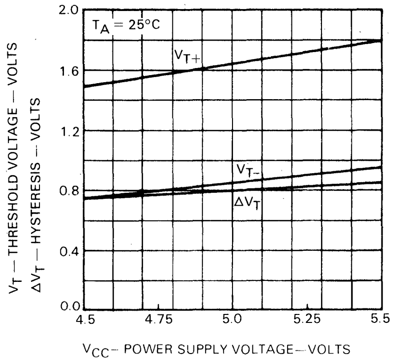


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS TEMPERATURE

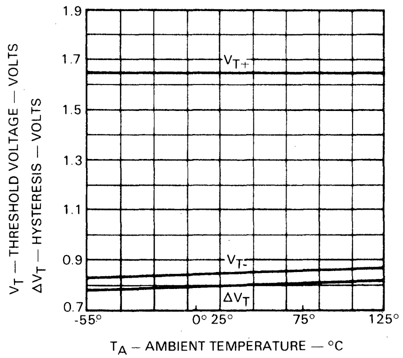
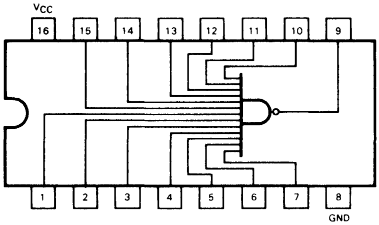


Fig. 3

MOTOROLA

SN54/74LS133



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

13-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				0.5	mA	V_{CC} = MAX
	Total, Output LOW				1.1		

AC CHARACTERISTICS: T_A = 25°C

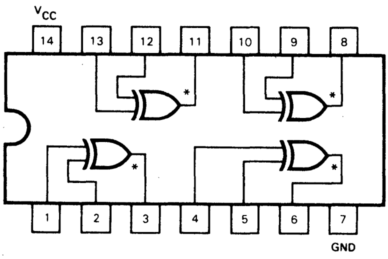
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		40	59	ns	C_L = 15 pF

MOTOROLA

SN74LS136

QUAD 2-INPUT EXCLUSIVE OR GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
V_{OH}	Output Voltage — High			5.5	V
I_{OL}	Output Current — Low			8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			−0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

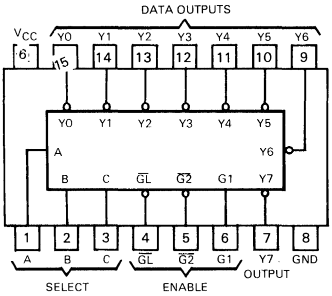
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		18 18	30 30	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		18 18	30 30	ns	

MOTOROLA

SN54/74LS137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

LOW POWER SCHOTTKY


DATA OUTPUTS
VCC
Y0
Y1
Y2
Y3
Y4
Y5
Y6
16
15
14
13
12
11
10
9
Y0
Y1
Y2
Y3
Y4
Y5
A
Y6
B
C
GL
G2
G1
Y7
1
2
3
4
5
6
7
8
A
B
C
GL
G2
G1
Y7
GND
OUTPUT
SELECT
ENABLE

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

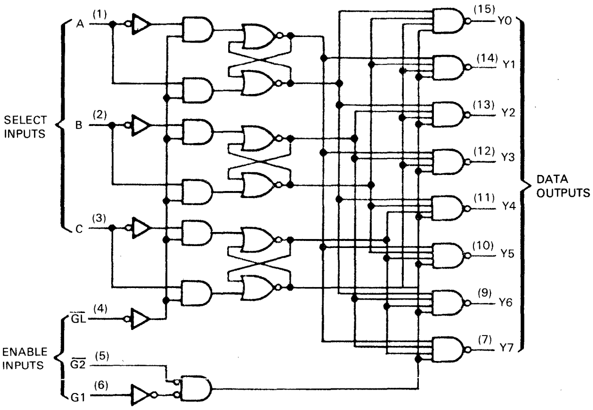
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				18	mA	V_{CC} = MAX	

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant


SELECT INPUTS
A (1)
B (2)
C (3)
ENABLE INPUTS
$\overline{GL}$ (4)
$\overline{G2}$ (5)
G1 (6)
(15) Y0
(14) Y1
(13) Y2
(12) Y3
(11) Y4
(10) Y5
(9) Y6
(7) Y7
DATA OUTPUTS

AC CHARACTERISTICS: $V_{CC} = 5.0$ V, $T_A = 25°C$

SYMBOL	PARAMETER	LEVELS OF DELAY	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay Time, A,B,C to Y	2 4		11 25	17 38	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay Time, A,B,C to Y	3 3		16 19	24 29	ns	
t_{PLH} t_{PHL}	Propagation Delay Time, Enable $\overline{G2}$ to Y	2 2		13 16	21 27	ns	
t_{PLH} t_{PHL}	Propagation Delay Time, Enable G1 to Y	3 3		14 18	21 27	ns	
t_{PLH} t_{PHL}	Propagation Delay Time, Enable $\overline{GL}$ to Y	3 4		18 25	27 38	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Pulse Width — Enable at $\overline{GL}$	15			ns	$V_{CC} = 5.0$ V
t_s	Setup Time, A,B,C	10			ns	
t_h	Hold Time, A,B,C	10			ns	

MOTOROLA

SN54/74LS138

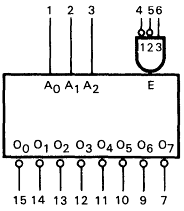
1-OF-8-DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- DEMULTIPLEXING CAPABILITY
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- TYPICAL POWER DISSIPATION OF 32 mW
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

LOGIC SYMBOL


1 2 3
4 5 6
1 2 3
A_0 A_1 A_2
E
O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7
15 14 13 12 11 10 9 7

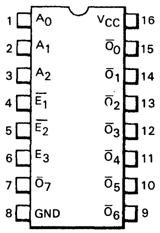
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOADING (Note a) LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1$, $\overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

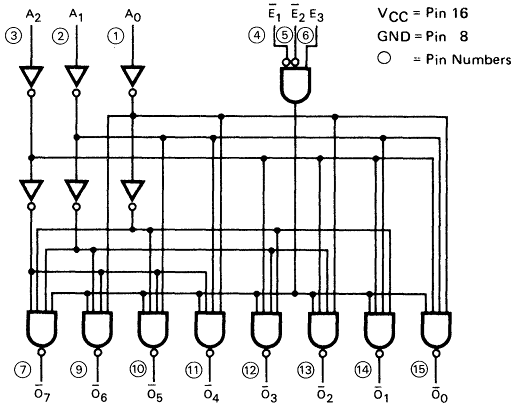
CONNECTION DIAGRAM
DIP (TOP VIEW)


1 A_0
2 A_1
3 A_2
4 $\overline{E}_1$
5 $\overline{E}_2$
6 E_3
7 $\overline{O}_7$
8 GND
16 V_{CC}
15 $\overline{O}_0$
14 $\overline{O}_1$
13 $\overline{O}_2$
12 $\overline{O}_3$
11 $\overline{O}_4$
10 $\overline{O}_5$
9 $\overline{O}_6$

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


A_2 A_1 A_0
③ ② ①
$\overline{E}_1$ $\overline{E}_2$ E_3
④ ⑤ ⑥
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers
⑦ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭ ⑮
$\overline{O}_7$ $\overline{O}_6$ $\overline{O}_5$ $\overline{O}_4$ $\overline{O}_3$ $\overline{O}_2$ $\overline{O}_1$ $\overline{O}_0$

FUNCTIONAL DESCRIPTION – The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

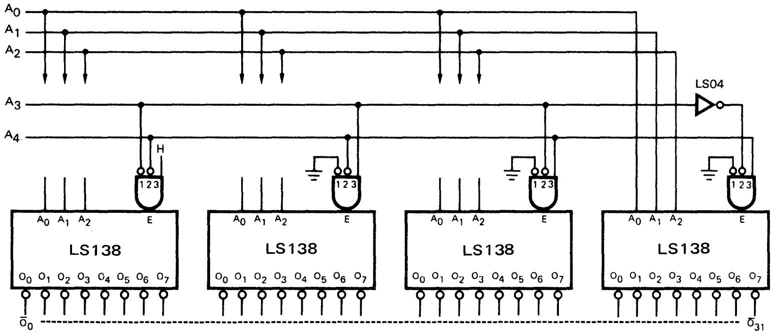


Fig. a.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LEVEL OF DELAY	LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay Address to Output	2 2		13 27	20 41	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Address to Output	3 3		18 26	27 39	ns	
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ Enable to Output	2 2		12 21	18 32	ns	
t_{PLH} t_{PHL}	Propagation Delay E_3 Enable to Output	3 3		17 25	26 38	ns	

AC WAVEFORMS

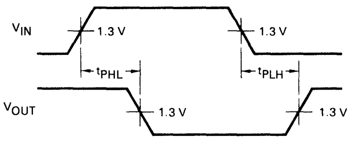


Fig. 1

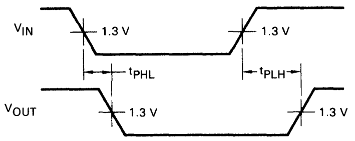


Fig. 2

MOTOROLA

SN54/74LS139

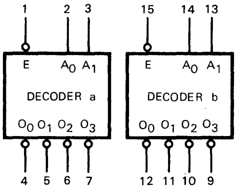
DUAL 1-OF-4 -DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY

DESCRIPTION —The LSTTL/MSI SN54LS/74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF- 4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL


1 2 3
15 14 13
E A0 A1
DECODER a
O0 O1 O2 O3
E A0 A1
DECODER b
O0 O1 O2 O3
4 5 6 7
12 11 10 9

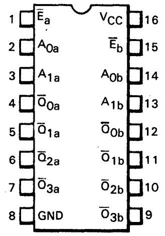
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

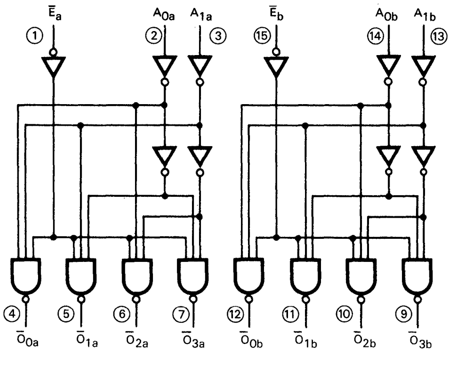
CONNECTION DIAGRAM DIP (TOP VIEW)


1 $\overline{E}_a$
2 A_{0a}
3 A_{1a}
4 $\overline{O}_{0a}$
5 $\overline{O}_{1a}$
6 $\overline{O}_{2a}$
7 $\overline{O}_{3a}$
8 GND
16 V_{CC}
15 $\overline{E}_b$
14 A_{0b}
13 A_{1b}
12 $\overline{O}_{0b}$
11 $\overline{O}_{1b}$
10 $\overline{O}_{2b}$
9 $\overline{O}_{3b}$

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


$\overline{E}_a$
A_{0a}
A_{1a}
$\overline{E}_b$
A_{0b}
A_{1b}
①
②
③
⑮
⑭
⑬
④
⑤
⑥
⑦
⑫
⑪
⑩
⑨
$\overline{O}_{0a}$
$\overline{O}_{1a}$
$\overline{O}_{2a}$
$\overline{O}_{3a}$
$\overline{O}_{0b}$
$\overline{O}_{1b}$
$\overline{O}_{2b}$
$\overline{O}_{3b}$

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

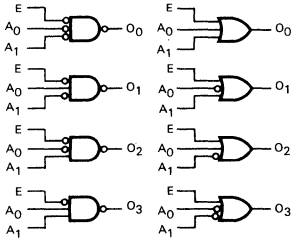


Fig. a

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				11	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LEVEL OF DELAY	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Address to Output	2 2		13 22	20 33	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Address to Output	3 3		18 25	29 38	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	2 2		16 21	24 32	ns	

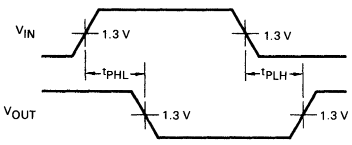


Fig. 1

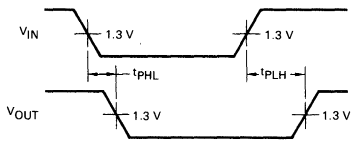


Fig. 2

MOTOROLA

SN54/74LS145

1-OF-10 DECODER/DRIVER OPEN-COLLECTOR

LOW POWER SCHOTTKY

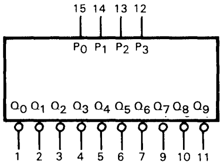
DESCRIPTION — The SN54LS/74LS145, 1-of-10 Decoder/Driver, is designed to accept BCD inputs and provide appropriate outputs to drive 10-digit incandescent displays. All outputs remain off for all invalid binary input conditions. It is designed for use as indicator/relay drivers or as an open-collector logic circuit driver. Each of the high breakdown output transistors will sink up to 80 mA of current. Typical power dissipation is 35 mW. This device is fully compatible with all TTL families.

- **LOW POWER VERSION OF 54/74145**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a) HIGH	**LOADING** (Note a) LOW
P_0, P_1, P_2, P_3	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{Q}_0$ to $\overline{Q}_9$	Outputs (Note b)	Open Collector	15 (7.5) U.L.

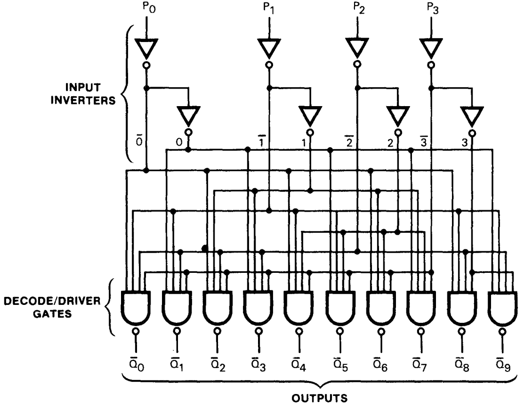
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges

LOGIC SYMBOL

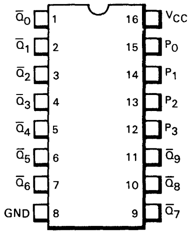

15 14 13 12
P0 P1 P2 P3
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
1 2 3 4 5 6 7 9 10 11

V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM


INPUTS
P0
P1
P2
P3
INPUT INVERTERS
0
0
1
1
2
2
3
3
DECODE/DRIVER GATES
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
OUTPUTS

CONNECTION DIAGRAM
DIP (TOP VIEW)


Q0 1
Q1 2
Q2 3
Q3 4
Q4 5
Q5 6
Q6 7
GND 8
16 VCC
15 P0
14 P1
13 P2
12 P3
11 Q9
10 Q8
9 Q7

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

TRUTH TABLE

INPUTS				OUTPUTS									
P_3	P_2	P_1	P_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			15	V
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			250	μA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
		54,74		2.3	3.0	V	I_{OL} = 80 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current				13	mA	V_{CC} = MAX, V_{IN} = GND	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL} t_{PLH}	Propagation Delay P_n Input to Q_n Output			50 50	ns	V_{CC} = 5.0 V C_L = 45 pF

AC WAVEFORMS

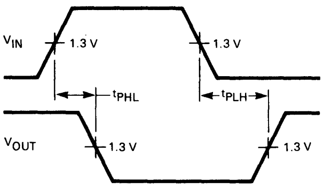


Fig. 1

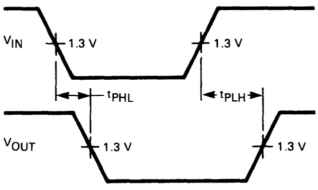


Fig. 2

MOTOROLA

SN54/74LS147
SN54/74LS148
SN54/74LS748

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS147 and the SN54LS/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

The SN54LS/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the EI input when data inputs 0-7 are at logical ones.

The only dc parameter differences between the LS148 and the LS748 are that (1) Pin 10 (input 0) has a fan-in of 2 on the LS748 versus a fan-in of 1 on the LS148; (2) Pins 1, 2, 3, 4, 11, 12 and 13 (inputs 1, 2, 3, 4, 5, 6, 7) have a fan-in of 3 on the LS748 versus a fan-in of 2 on the LS148.

The only ac difference is that t_{PHL} from EI to EO is changed from 40 to 45 ns.

SN54LS/74LS147
FUNCTION TABLE

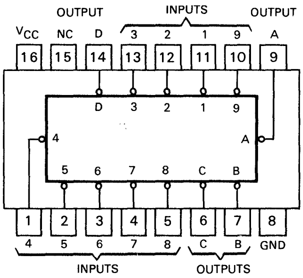
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

SN54LS/74LS148
SN54LS/74LS748
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

SN54LS/74LS147
(TOP VIEW)


OUTPUT
INPUTS
OUTPUT
VCC
NC
D
3
2
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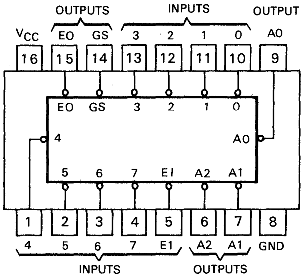
9
A
16
15
14
13
12
11
10
9
D
3
2
1
9
4
A
5
6
7
8
C
B
1
2
3
4
5
6
7
8
4
5
6
7
8
C
B
GND
INPUTS
OUTPUTS

SN54LS/74LS148
SN54LS/74LS748
(TOP VIEW)


OUTPUTS
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OUTPUT
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GS
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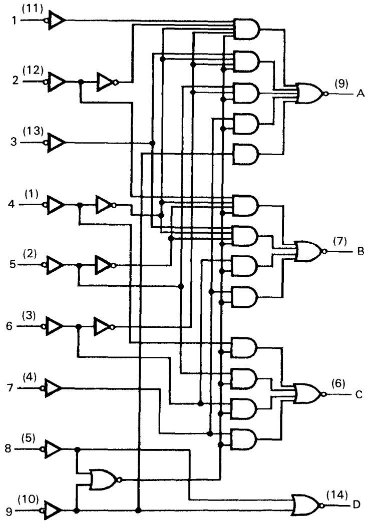
11
10
9
EO
GS
3
2
1
0
4
A0
5
6
7
EI
A2
A1
1
2
3
4
5
6
7
8
4
5
6
7
E1
A2
A1
GND
INPUTS
OUTPUTS

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

FUNCTIONAL BLOCK DIAGRAMS


(11)
1
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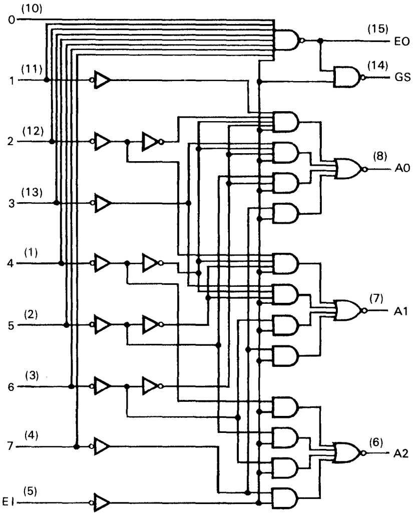
9
(9)
A
(7)
B
(6)
C
(14)
D

SN54LS/74LS147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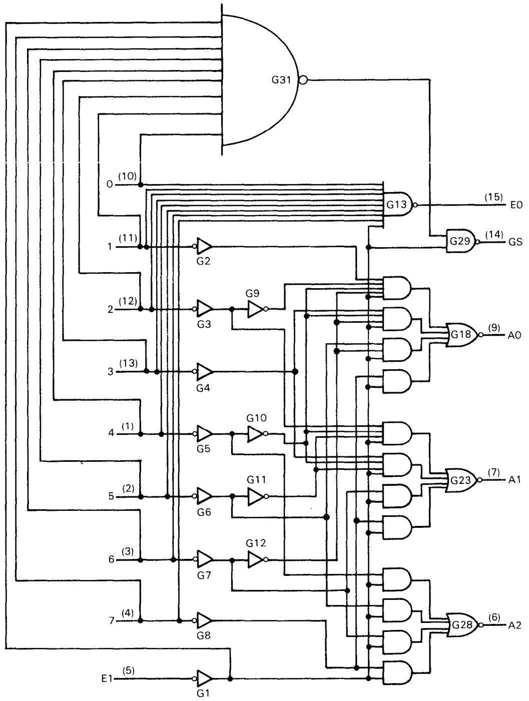
(4)
7
(5)
EI
(15)
EO
(14)
GS
(8)
A0
(7)
A1
(6)
A2

SN54LS/74LS148


G31
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(11)
1
G2
(12)
2
G3
G9
(13)
3
G4
(1)
4
G5
G10
(2)
5
G6
G11
(3)
6
G7
G12
(4)
7
G8
(5)
E1
G1
G13
(15)
EO
G29
(14)
GS
G18
(9)
A0
G23
(7)
A1
G28
(6)
A2

SN54LS/74LS748

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current							
	All Others				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input 0 (LS748)				40			
	Inputs 1–7 (LS148)				40			
	Inputs 1–7 (LS748)				60			
	All Others				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
	Input 0 (LS748)				0.2			
	Inputs 1–7 (LS148)				0.2			
	Inputs 1–7 (LS748)				0.3			
I_{IL}	Input LOW Current							
	All Others				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	Input 0 (LS748)				−0.8			
	Inputs 1–7 (LS148)				−0.8			
	Inputs 1–7 (LS748)				−1.2			
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CCH}	Power Supply Current Output High				17	mA	V_{CC} = MAX, All Inputs = 4.5 V	
I_{CCL}	Output Low				20	mA	V_{CC} = MAX, Inputs 7 & E1 = GND All Other Inputs = 4.5 V	

AC CHARACTERISTICS: $V_{CC} = 5.0$ V, $T_A = 25°C$

SN54LS/74LS147

SYMBOL	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	LIMITS			UNIT	TEST CONDITIONS
				MIN	TYP	MAX		
t_{PLH}	Any	Any	In-phase output		12	18	ns	CL = 15 pF, R_L = 2 kΩ
t_{PHL}					12	18		
t_{PLH}	Any	Any	Out-of-phase output		21	33	ns	
t_{PHL}					15	23		

SN54LS/74LS148
SN54LS/74LS748

SYMBOL	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	LIMITS			UNIT	TEST CONDITIONS
				MIN	TYP	MAX		
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output		14	18	ns	C_L = 15 pF, R_L = 2 kΩ,
t_{PHL}					15	25		
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output		20	36	ns	
t_{PHL}					16	29		
t_{PLH}	0 thru 7	EO	Out-of-phase output		7.0	18	ns	
t_{PHL}					25	40		
t_{PLH}	0 thru 7	GS	In-phase output		35	55	ns	
t_{PHL}					9.0	21		
t_{PLH}	EI	A0, A1, or A2	In-phase output		16	25	ns	
t_{PHL}					12	25		
t_{PLH}	EI	GS	In-phase output		12	17	ns	
t_{PHL}					14	36		
t_{PLH}	EI	EO	In-phase output		12	21	ns	
t_{PHL}					28 30	40 45		(LS148) (LS748)

MOTOROLA

SN54/74LS151

8-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN54LS/74LS151 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

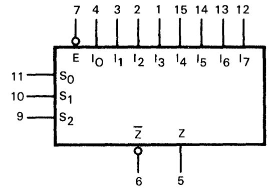
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

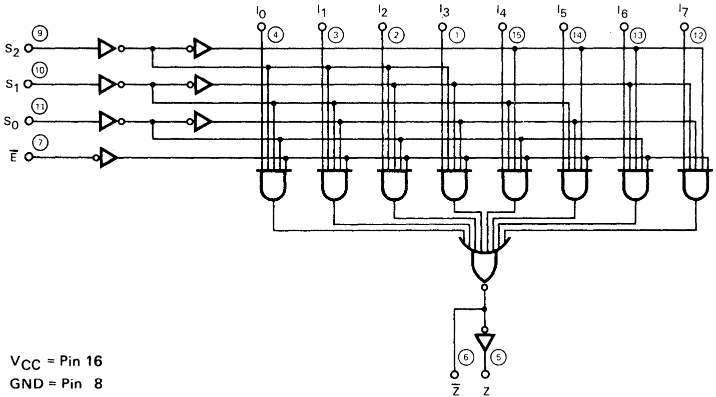
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


7 4 3 2 1 15 14 13 12
E I0 I1 I2 I3 I4 I5 I6 I7
11 S0
10 S1
9 S2
Z̄ Z
6 5

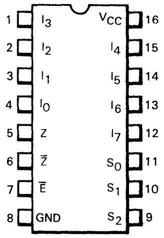
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM


S2 9
S1 10
S0 11
Ē 7
I0 4
I1 3
I2 2
I3 1
I4 15
I5 14
I6 13
I7 12
6 5
Z̄ Z

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)


1 I3
2 I2
3 I1
4 I0
5 Z
6 Z̄
7 Ē
8 GND
16 VCC
15 I4
14 I5
13 I6
12 I7
11 S0
10 S1
9 S2

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

FUNCTIONAL DESCRIPTION – The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E}\cdot(I_0\cdot\overline{S}_0\cdot\overline{S}_1\cdot\overline{S}_2 + I_1\cdot S_0\cdot\overline{S}_1\cdot\overline{S}_2 + I_2\cdot\overline{S}_0\cdot S_1\cdot\overline{S}_2 + I_3\cdot S_0\cdot S_1\cdot\overline{S}_2 +$$
$$I_4\cdot\overline{S}_0\cdot\overline{S}_1\cdot S_2 + I_5\cdot S_0\cdot\overline{S}_1\cdot S_2 + I_6\cdot\overline{S}_0\cdot S_1\cdot S_2 + I_7\cdot S_0\cdot S_1\cdot S_2).$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay Select to Output Z		27 18	43 30	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Select to Output $\overline{Z}$		14 20	23 32	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output Z		26 20	42 32	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output $\overline{Z}$		15 18	24 30	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to Output Z		20 16	32 26	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to Output $\overline{Z}$		13 12	21 20	ns	

AC WAVEFORMS

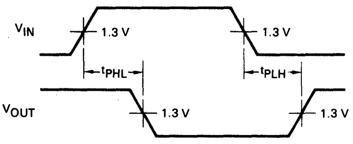


Fig. 1

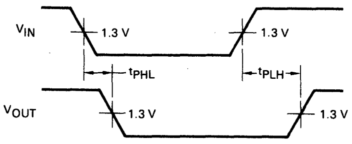


Fig. 2

MOTOROLA

SN54/74LS153

DUAL 4-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

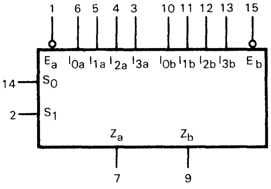
DESCRIPTION — The LSTTL/MSI SN54LS/74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **SEPARATE ENABLE FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

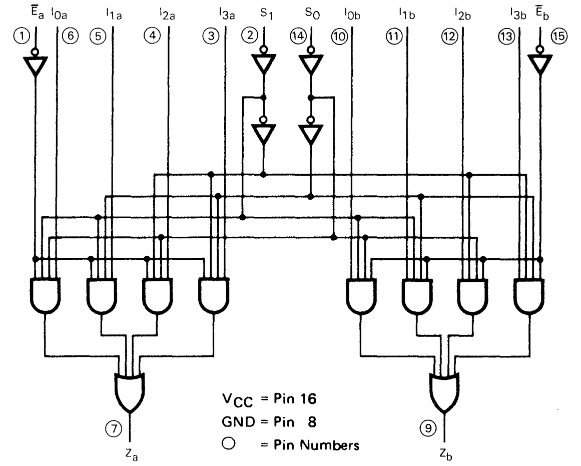
LOGIC SYMBOL



1 6 5 4 3 10 11 12 13 15
$\overline{E}_a$ I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b} $\overline{E}_b$
14 S_0
2 S_1
Z_a Z_b
7 9

V_{CC} = Pin 16
GND = Pin 8

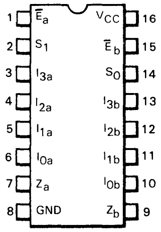
LOGIC DIAGRAM



$\overline{E}_a$ I_{0a} I_{1a} I_{2a} I_{3a} S_1 S_0 I_{0b} I_{1b} I_{2b} I_{3b} $\overline{E}_b$
① ⑥ ⑤ ④ ③ ② ⑭ ⑩ ⑪ ⑫ ⑬ ⑮
⑦ Z_a
⑨ Z_b

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



1 $\overline{E}_a$
2 S_1
3 I_{3a}
4 I_{2a}
5 I_{1a}
6 I_{0a}
7 Z_a
8 GND
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Z_b

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS153 is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay Data to Output		10 17	15 26	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Select to Output		19 25	29 38	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output		16 21	24 32	ns	Fig. 2	

AC WAVEFORMS

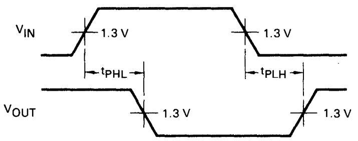


Fig. 1

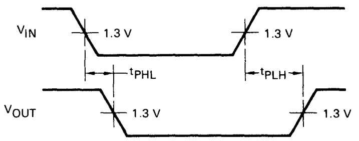


Fig. 2

MOTOROLA

SN54/74LS155
SN54/74LS156

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

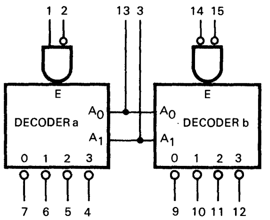
LS156-OPEN-COLLECTOR
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS155 and SN54LS/ 74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **COMMON ADDRESS INPUTS**
- **TRUE OR COMPLEMENT DATA DEMULTIPLEXING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL



1 2
13 3
14 15
E
DECODER a
A0
A1
0 1 2 3
7 6 5 4
E
A0
DECODER b
A1
0 1 2 3
9 10 11 12

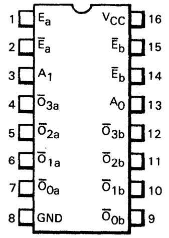
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_a, \overline{E}_b$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

CONNECTION DIAGRAM
DIP (TOP VIEW)

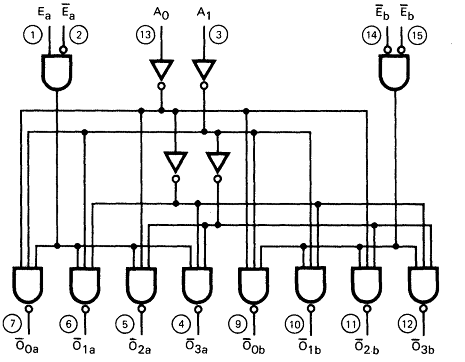


1 Ea
2 Ēa
3 A1
4 Ō3a
5 Ō2a
6 Ō1a
7 Ō0a
8 GND
16 VCC
15 Ēb
14 Ēb
13 A0
12 Ō3b
11 Ō2b
10 Ō1b
9 Ō0b

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



Ea Ēa
1 2
A0
13
A1
3
Ēb Ēb
14 15
7 Ō0a
6 Ō1a
5 Ō2a
4 Ō3a
9 Ō0b
10 Ō1b
11 Ō2b
12 Ō3b

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$—$\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \bullet \overline{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \bullet \overline{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection as (A_2). The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)$$

$$\text{where } E = E_a + \overline{E}_a;\ E = E_b + E_b$$

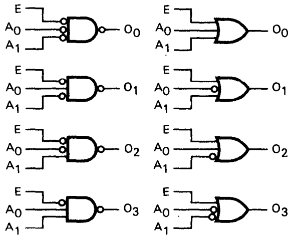


Fig. a

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS	
		TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay Address, $\overline{E}_a$ or $\overline{E}_b$ to Output	10 19	15 30	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Address to Output	17 19	26 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output	18 18	27 27	ns	Fig. 1	

AC WAVEFORMS

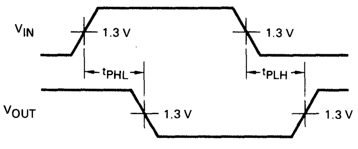


Fig. 1

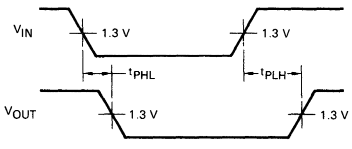


Fig. 2

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS T_A = 25°C

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS	
		TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay Address, $\overline{E}_a$ or $\overline{E}_b$ to Output	25 34	40 51	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 kΩ
t_{PLH} t_{PHL}	Propagation Delay Address to Output	31 34	46 51	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output	32 32	48 48	ns	Fig. 1	

AC WAVEFORMS

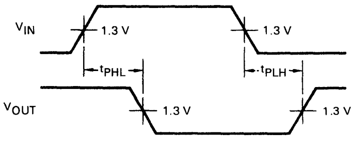


Fig. 1

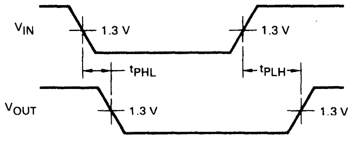


Fig. 2

MOTOROLA

SN54/74LS157

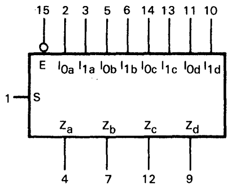
QUAD 2-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL


15 2 3 5 6 14 13 11 10
E
I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d}
1
S
Z_a Z_b Z_c Z_d
4 7 12 9

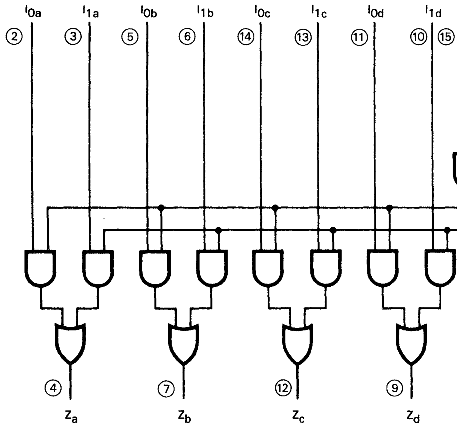
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	10 U.L.	5 (2.5) U.L.

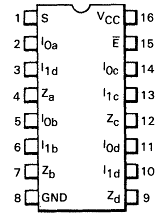
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM


I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d} $\overline{E}$ S
② ③ ⑤ ⑥ ⑭ ⑬ ⑪ ⑩ ⑮ ①
④ ⑦ ⑫ ⑨
Z_a Z_b Z_c Z_d

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)


1 S
2 I_{0a}
3 I_{1d}
4 Z_a
5 I_{0b}
6 I_{1b}
7 Z_b
8 GND
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current I_0,I_1 $\overline{E}$,S				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	I_0,I_1 $\overline{E}$,S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current I_0,I_1 $\overline{E}$,S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				16	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay Data to Output		9.0 9.0	14 14	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Enable to Output		13 14	20 21	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		15 18	23 27	ns	Fig. 2	

AC WAVEFORMS

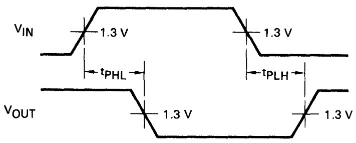


Fig. 1

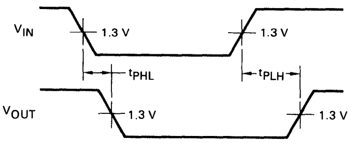


Fig. 2

MOTOROLA

SN54/74LS158

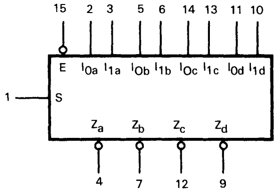
QUAD 2-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS158 is a high speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The LS158 can also generate any four of the 16 different functions of two variables. The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INVERTED OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL


15
2
3
5
6
14
13
11
10
E
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
1
S
Za
Zb
Zc
Zd
4
7
12
9

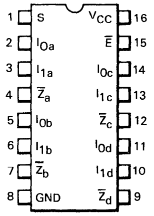
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOADING (Note a) LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

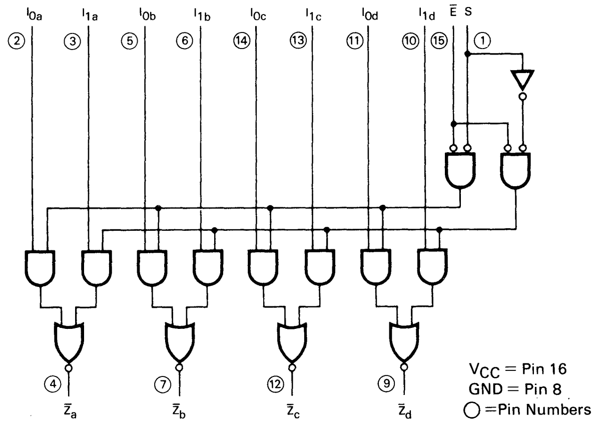
CONNECTION DIAGRAM DIP (TOP VIEW)


1
S
VCC
16
2
I0a
E
15
3
I1a
I0c
14
4
Za
I1c
13
5
I0b
Zc
12
6
I1b
I0d
11
7
Zb
I1d
10
8
GND
Zd
9

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
E
S
②
③
⑤
⑥
⑭
⑬
⑪
⑩
⑮
①
④
⑦
⑫
⑨
Za
Zb
Zc
Zd
VCC = Pin 16
GND = Pin 8
○ = Pin Numbers

5

FUNCTIONAL DESCRIPTION – The LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current I_0, I_1 $\overline{E}$, S				 20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	I_0, I_1 $\overline{E}$, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current I_0, I_1 $\overline{E}$, S				 −0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				8.0	mA	V_{CC} = MAX	All inputs at 4.5 V. All outputs open.
I_{CC}	Power Supply Current				11	mA	V_{CC} = MAX	All other input combinations. All outputs open.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay Data to Output		7.0 10	12 15	ns	Figure 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Enable to Output		11 18	17 24	ns	Figure 1	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		13 16	20 24	ns	Figure 2	

AC WAVEFORMS

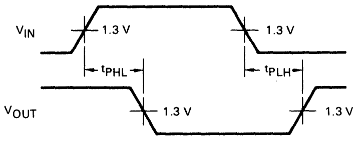


Fig. 1

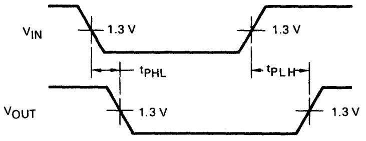


Fig. 2

MOTOROLA

SN54/74LS160A
SN54/74LS161A
SN54/74LS162A
SN54/74LS163A

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

LOW POWER SCHOTTKY

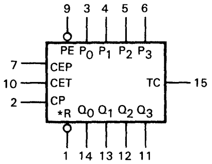
DESCRIPTION — The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary.)

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

- **SYNCHRONOUS COUNTING AND LOADING**
- **TWO COUNT ENABLE INPUTS FOR HIGH SPEED SYNCHRONOUS EXPANSION**
- **TERMINAL COUNT FULLY DECODED**
- **EDGE-TRIGGERED OPERATION**
- **TYPICAL COUNT RATE OF 35 MHz**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

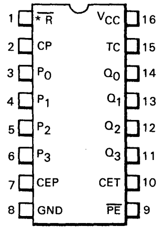
*MR for LS160A and LS161A
*SR for LS162A and LS163A

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{SR}$	Synchronous Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commerical (74) Temperature Ranges.

CONNECTION DIAGRAMS
DIP (TOP VIEW)

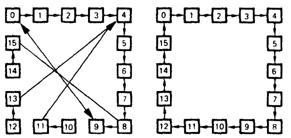


*MR for LS160A and LS161A
*SR for LS162A and LS163A

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAM



LS160A • LS162A **LS161A • LS163A**

LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for LS160A & LS162A = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160A & LS161A)
Reset = $\overline{SR}$ • CP + (rising clock edge)
(LS162A & LS163A)

NOTE:
The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION – The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs – Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH. When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the $\overline{PE}$ held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (_⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

LS160A and LS161A
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current $\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	$\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V_{CC} = MAX	

LS162A and LS163A
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

AC SETUP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Clock Pulse Width Low	25			ns	V_{CC} = 5.0 V
t_W	$\overline{MR}$ or $\overline{SR}$ Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time $\overline{PE}$ or $\overline{SR}$	25			ns	
t_h	Hold Time, Any Input	0			ns	
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			ns	

*CEP, CET or DATA

DEFINITION OF TERMS:

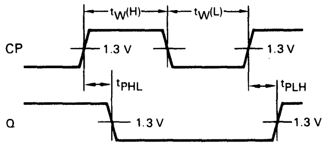
SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

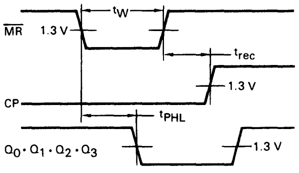
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ ($\overline{SR}$) = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

AC WAVEFORMS (Cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the $(Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3)$ state for the LS160 and LS162 and the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the LS161 and LS163.

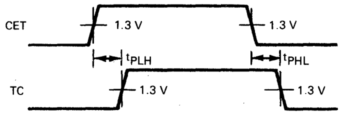

CET
1.3 V
1.3 V
tPLH
tPHL
TC
1.3 V
1.3 V

Fig. 3

Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state $(Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3)$ for the LS161 and LS163 and $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ for the LS161 and LS163.

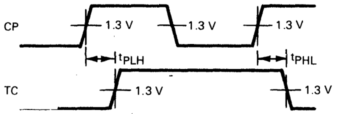

CP
1.3 V
1.3 V
1.3 V
tPLH
tPHL
TC
1.3 V
1.3 V

Fig. 4

Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

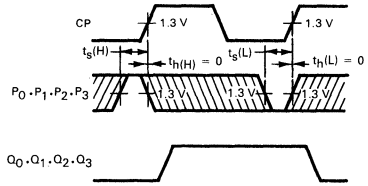

CP
1.3 V
1.3 V
ts(H)
th(H) = 0
ts(L)
th(L) = 0
P0 • P1 • P2 • P3
1.3 V
1.3 V
1.3 V
Q0 • Q1 • Q2 • Q3

Fig. 5

Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

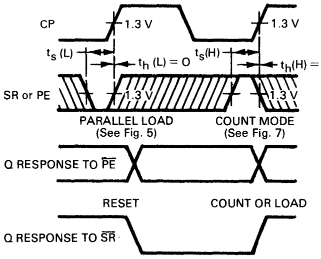
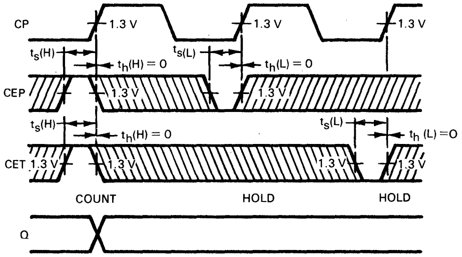

CP
1.3 V
1.3 V
ts (L)
th (L) = 0
ts(H)
th(H) = 0
SR or PE
1.3 V
1.3 V
PARALLEL LOAD
(See Fig. 5)
COUNT MODE
(See Fig. 7)
Q RESPONSE TO PE
RESET
COUNT OR LOAD
Q RESPONSE TO SR

Fig. 6


CP
1.3 V
1.3 V
1.3 V
ts(H)
th(H) = 0
ts(L)
th(L) = 0
CEP
1.3 V
1.3 V
ts(H)
th(H) = 0
ts(L)
th (L) = 0
CET
1.3 V
1.3 V
1.3 V
1.3 V
COUNT
HOLD
HOLD
Q

Other Conditions: $\overline{PE}$ = H, $\overline{MR}$ = H

Fig. 7

MOTOROLA

SN54/74LS164

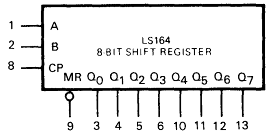
DESCRIPTION — The SN54LS/74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

LOW POWER SCHOTTKY

- **TYPICAL SHIFT FREQUENCY OF 35 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **GATED SERIAL DATA INPUT**
- **FULLY SYNCHRONOUS DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL


1
2
8
A
B
CP
LS164
8-BIT SHIFT REGISTER
MR Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
9 3 4 5 6 10 11 12 13

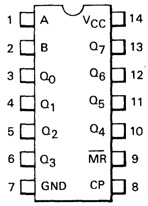
V_{CC} = Pin 14
GND = Pin 7

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (**54**) and 5 U.L. for Commercial (**74**) Temperature Ranges.

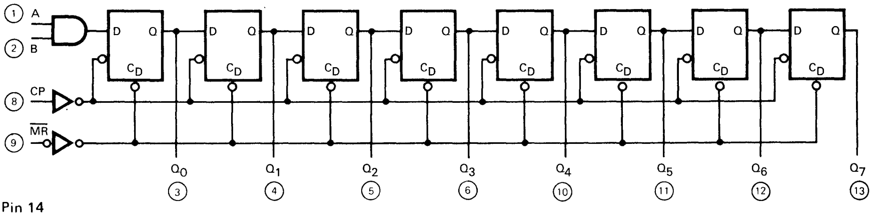
CONNECTION DIAGRAM DIP (TOP VIEW)


1 A
2 B
3 Q0
4 Q1
5 Q2
6 Q3
7 GND
14 VCC
13 Q7
12 Q6
11 Q5
10 Q4
9 MR
8 CP

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


1 A
2 B
8 CP
9 MR
D Q
CD
Q0 3
Q1 4
Q2 5
Q3 6
Q4 10
Q5 11
Q6 12
Q7 13

V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	36		MHz	$V_{CC} = 5$ V $C_L = 15$ pF
t_{PHL}	Propagation Delay $\overline{MR}$ to Output Q		24	36	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output Q		17 21	27 32	ns	

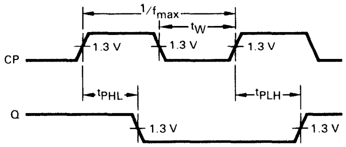
AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	CP, $\overline{MR}$ Pulse Width	20			ns	$V_{CC} = 5$ V
t_s	Data Setup Time	15			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	$\overline{MR}$ to Clock Recovery Time	20			ns	

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH


1/fmax
tW
CP
1.3 V
1.3 V
1.3 V
tPHL
tPLH
Q
1.3 V
1.3 V

CONDITIONS: $\overline{MR}$ = H

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

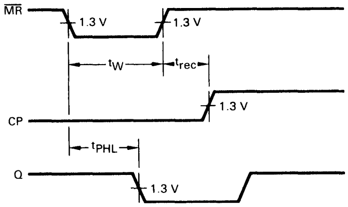

MR
1.3 V
1.3 V
tW
trec
CP
1.3 V
tPHL
Q
1.3 V

Fig. 2

DATA SETUP AND HOLD TIMES

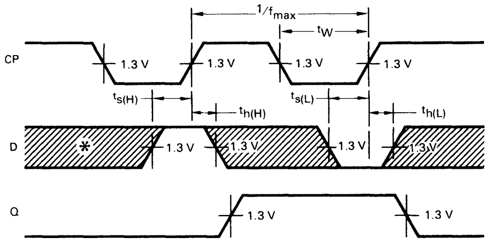

1/fmax
tW
CP
1.3 V
1.3 V
1.3 V
1.3 V
ts(H)
th(H)
ts(L)
th(L)
D
*
1.3 V
1.3 V
1.3 V
1.3 V
Q
1.3 V
1.3 V

Fig. 3

MOTOROLA

SN54/74LS165

8-BIT PARALLEL-TO-SERIAL CONVERTER

LOW POWER SCHOTTKY

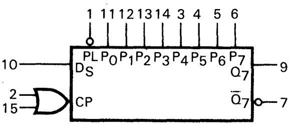
DESCRIPTION — The SN54LS/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

PIN NAMES

		LOADING (Note a) HIGH	LOADING (Note a) LOW
CP_1, CP_2	Clock (LOW-to-HIGH Going Edge) Inputs	0.5 U.L.	0.25 U.L.
DS	Serial Data Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	1.5 U.L.	0.75 U.L.
P_0-P_7	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_7	Serial Output from Last State (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_7$	Complementary Output (Note b)	10 U.L.	5 (2.5) U.L.

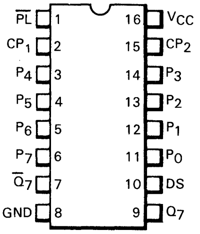
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


1 11 12 13 14 3 4 5 6
PL P0 P1 P2 P3 P4 P5 P6 P7
DS
Q7
CP
Q̄7
10
9
2
15
7

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)


P̄L 1
CP1 2
P4 3
P5 4
P6 5
P7 6
Q̄7 7
GND 8
16 VCC
15 CP2
14 P3
13 P2
12 P1
11 P0
10 DS
9 Q7

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

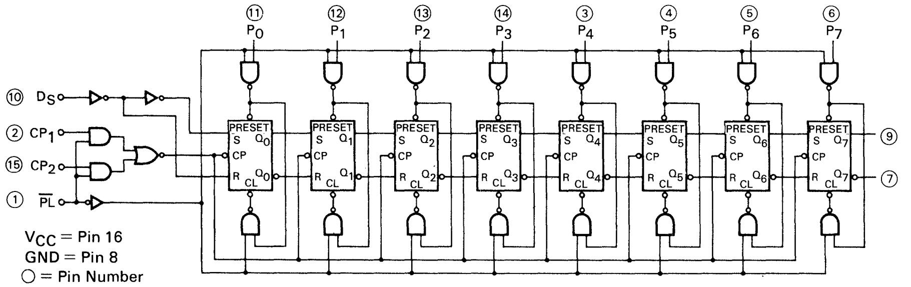
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

$\overline{PL}$	CP 1	CP 2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	RESPONSE
L	X	X	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Parallel Entry
H	L	↑	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	↑	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	↑	L	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	↑	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM


⑪ P0
⑫ P1
⑬ P2
⑭ P3
③ P4
④ P5
⑤ P6
⑥ P7
⑩ DS
② CP1
⑮ CP2
① P̄L
PRESET S Q0 CP R CL Q̄0
PRESET S Q1 CP R CL Q̄1
PRESET S Q2 CP R CL Q̄2
PRESET S Q3 CP R CL Q̄3
PRESET S Q4 CP R CL Q̄4
PRESET S Q5 CP R CL Q̄5
PRESET S Q6 CP R CL Q̄6
PRESET S Q7 CP R CL Q̄7
⑨
⑦

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION — The SN54LS/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW, provided that the recommended setup and hold times are observed.

For clock operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Other Inputs $\overline{PL}$ Input				20 60	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Other Inputs $\overline{PL}$ Input				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Other Inputs $\overline{PL}$ Input				−0.4 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				36	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Input Clock Frequency	25	35		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Output		22 22	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output		27 28	40 40	ns	
t_{PLH} t_{PHL}	Propagation Delay P_7 to Q_7		14 21	25 30	ns	
t_{PLH} t_{PHL}	Propagation Delay P_7 to $\overline{Q}_7$		21 16	30 25	ns	

AC SETUP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	CP Clock Pulse Width	25			ns	V_{CC} = 5.0 V
t_W	$\overline{PL}$ Pulse Width	15			ns	
t_s	Parallel Data Setup Time	10			ns	
t_s	Serial Data Setup Time	20			ns	
t_s	CP_1 to CP_2 Setup Time[1]	30			ns	
t_h	Hold Time	0			ns	
t_{rec}	Recovery Time, $\overline{PL}$ to CP	45			ns	

① The role of CP_1, and CP_2 in an application may be interchanged

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the $\overline{PL}$ pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

AC WAVEFORMS

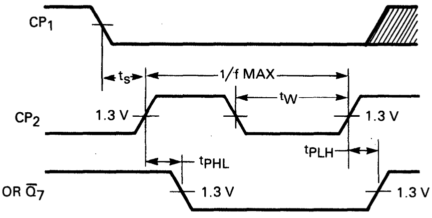


Fig.1

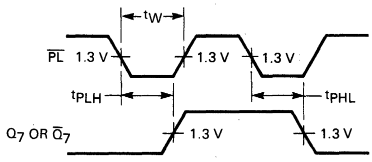


Fig. 2

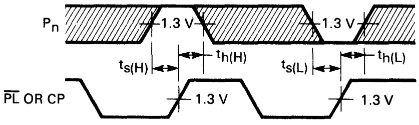


Fig. 3

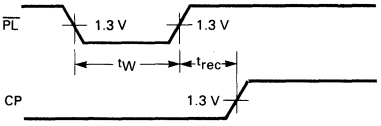


Fig. 4

MOTOROLA

SN54/74LS166

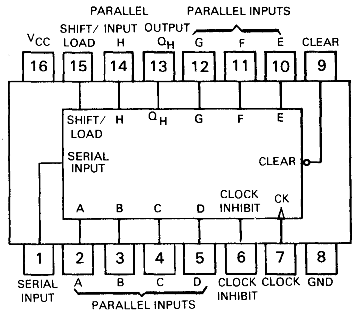
8-BIT SHIFT REGISTERS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 54LS/74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- **SYNCHRONOUS LOAD**
- **DIRECT OVERRIDING CLEAR**
- **PARALLEL TO SERIAL CONVERSION**

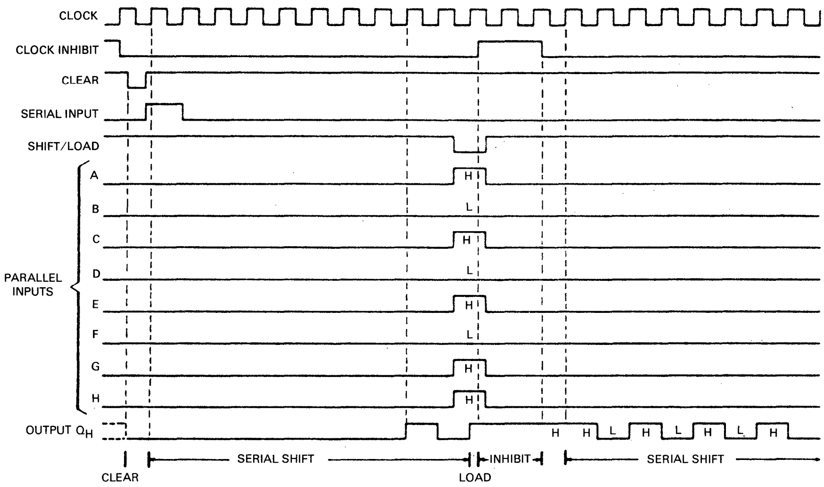


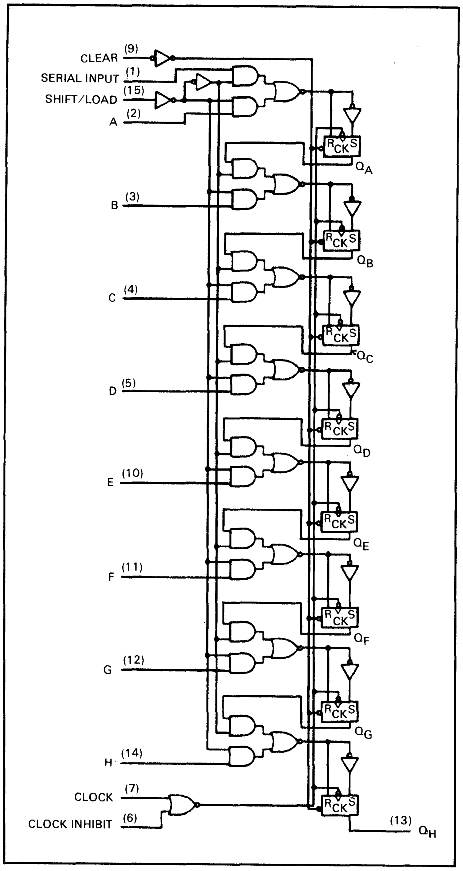
J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Typical Clear, Shift, Load, Inhibit, and Shift Sequences




CLEAR (9)
SERIAL INPUT (1)
SHIFT/LOAD (15)
A (2)
B (3)
C (4)
D (5)
E (10)
F (11)
G (12)
H (14)
CLOCK (7)
CLOCK INHIBIT (6)
R CK S
QA
QB
QC
QD
QE
QF
QG
(13) QH

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

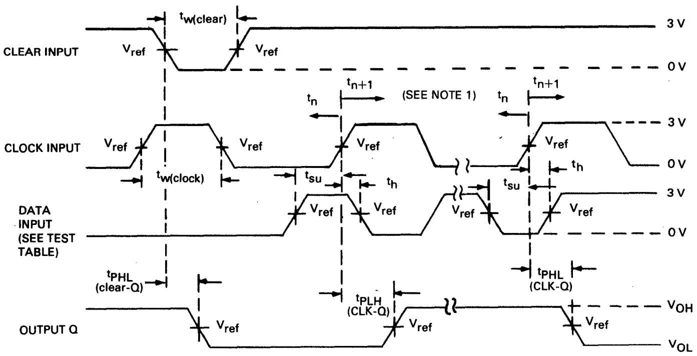
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				38	mA	V_{CC} = MAX	

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}

AC WAVEFORMS


CLEAR INPUT
CLOCK INPUT
DATA INPUT (SEE TEST TABLE)
OUTPUT Q
$t_{w(clear)}$
$t_{w(clock)}$
V_{ref}
3 V
0 V
t_n
t_{n+1}
(SEE NOTE 1)
t_{su}
t_h
t_{PHL} (clear-Q)
t_{PLH} (CLK-Q)
t_{PHL} (CLK-Q)
V_{OH}
V_{OL}

Note 1. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions
LS166 $V_{ref} = 1.3$ V.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PHL}	Clear to Output		19	30	ns	
t_{PLH} t_{PHL}	Clock to Output		23 24	35 35	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Clear Pulse Width	30			ns	$V_{CC} = 5.0$ V
t_s	Mode Control Setup Time	30			ns	
t_s	Data Setup Time	20			ns	
t_h	Hold Time, Any Input	15			ns	

MOTOROLA

SN54/74LS168
SN54/74LS169

BCD DECADE/MODULO 16 BINARY SYNCHRONOUS BI-DIRECTIONAL COUNTERS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS168 and SN54LS/74LS169 are fully synchronous 4-stage up/down counters featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. The SN54LS/74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the SN54LS/74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to HIGH transition of the clock.

- LOW POWER DISSIPATION 100mW TYPICAL
- HIGH-SPEED COUNT FREQUENCY 30 MHz TYPICAL
- FULLY SYNCHRONOUS OPERATION
- FULL CARRY LOOKAHEAD FOR EASY CASCADING
- SINGLE UP/DOWN CONTROL INPUT
- POSITIVE EDGE-TRIGGER OPERATION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

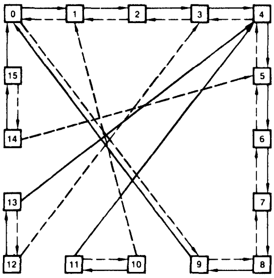
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CEP}$	Count Enable Parallel (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{CET}$	Count Enable Trickle (Active LOW) Input	1.0 U.L.	0.5 U.L.
CP	Clock Pulse (Active positive going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$U/\overline{D}$	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Flip-Flop Outputs	10 U.L.	5 (2.5) U.L.
$\overline{TC}$	Terminal Count (Active LOW) Output	10 U.L.	5 (2.5) U.L.

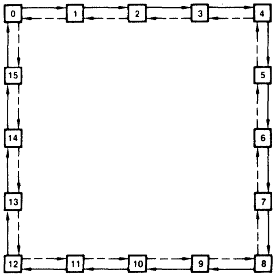
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

STATE DIAGRAMS

SN54LS/74LS168
UP/DOWN DECADE COUNTER



SN54LS/74LS169



SN54LS/74LS168

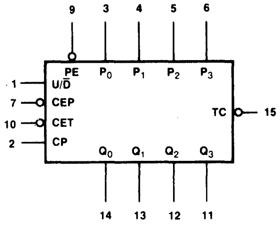
UP: $TC = Q_0 \cdot Q_3 \cdot (U/\overline{D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/\overline{D}})$

——→ Count Up
– – → Count Down

SN54LS/74LS169

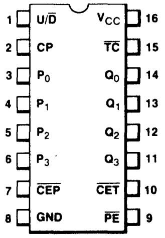
UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/\overline{D}})$

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

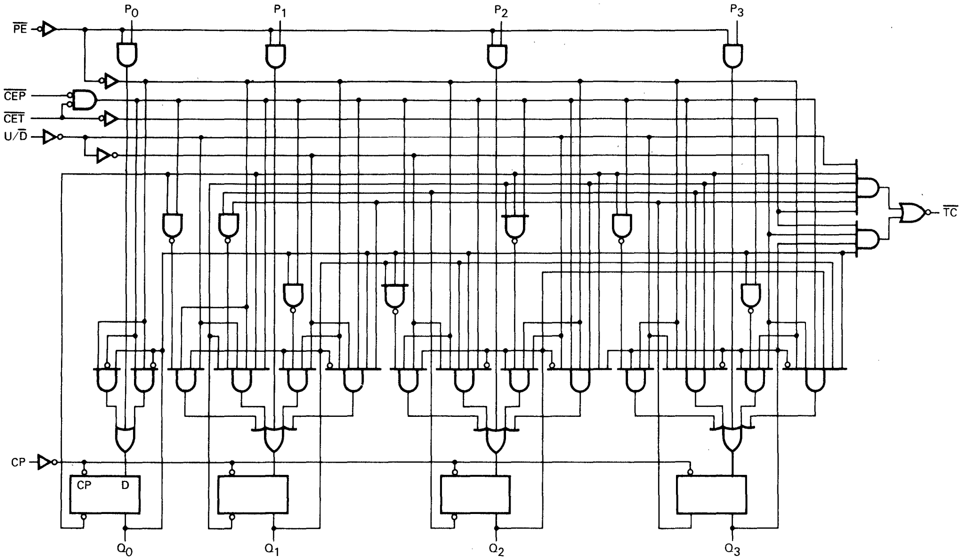


J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

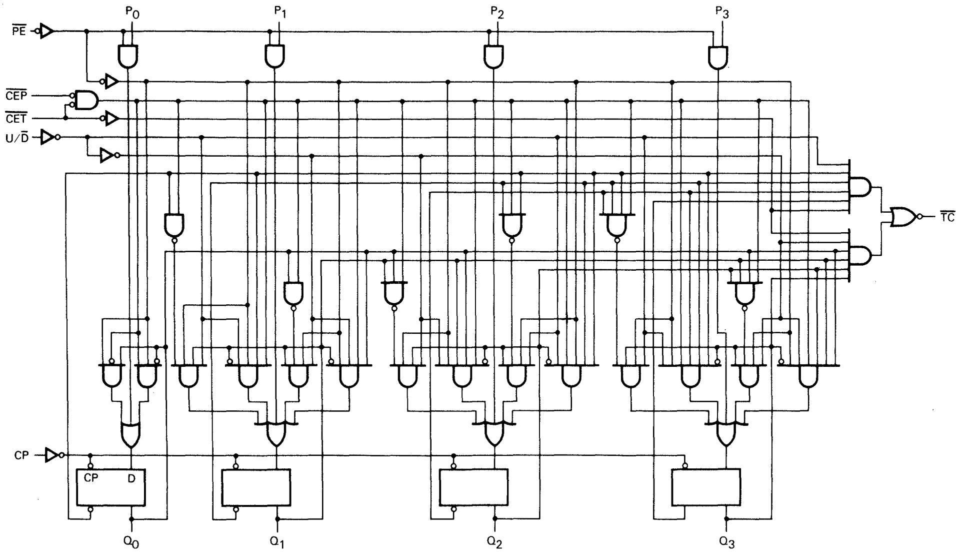
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS

SN54LS/74LS168


P0
P1
P2
P3
PE
CEP
CET
U/D
TC
CP
CP
D
Q0
Q1
Q2
Q3

SN54LS/74LS169


P0
P1
P2
P3
PE
CEP
CET
U/D
TC
CP
CP
D
Q0
Q1
Q2
Q3

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Other Inputs $\overline{\text{CET}}$ Input				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Other Input $\overline{\text{CET}}$ Input				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Other Input $\overline{\text{CET}}$ Input				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX	

FUNCTIONAL DESCRIPTION — The SN54LS74LS168 and SN54LS74LS169 use edge-triggered D-type flip-flops andthat have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting.

The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the SN54LS74LS168) in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the SN54LS74LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If illegal state occurs, the SN54LS74LS168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended.

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (Pn→Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = immaterial

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to $\overline{TC}$		23 23	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to any Q		13 15	20 23	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CET}$ to $\overline{TC}$		15 15	20 20	ns	
t_{PLH} t_{PHL}	Propagation Delay, U/$\overline{D}$ to $\overline{TC}$		17 19	25 29	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$,

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	25			ns	$V_{CC} = 5.0$ V
t_s	Setup Time, Data or Enable	20			ns	
t_s	Setup Time $\overline{PE}$	25			ns	
t_s	Setup Time U/$\overline{D}$	30			ns	
t_h	Hold Time Any Input	0			ns	

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.

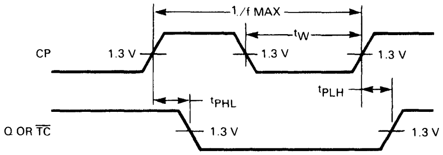

1/f MAX
tW
CP
1.3 V
1.3 V
1.3 V
tPHL
tPLH
Q OR TC
1.3 V
1.3 V

Fig. 1

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

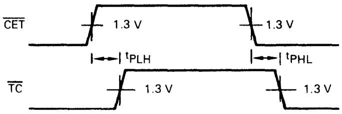

CET
1.3 V
1.3 V
tPLH
tPHL
TC
1.3 V
1.3 V

Fig. 2

CLOCK TO TERMINAL DELAYS

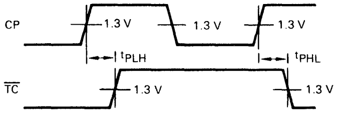

CP
1.3 V
1.3 V
1.3 V
tPLH
tPHL
TC
1.3 V
1.3 V

Fig. 3

SETUP TIME (t_s) AND HOLD (t_h) FOR PARALLEL DATA INPUTS.

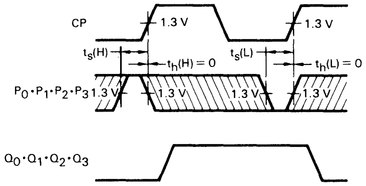
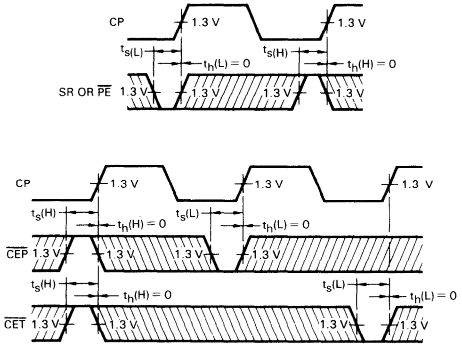

CP
1.3 V
1.3 V
ts(H)
th(H) = 0
ts(L)
th(L) = 0
P0•P1•P2•P3
1.3 V
1.3 V
1.3 V
1.3 V
Q0•Q1•Q2•Q3

Fig. 4

SETUP TIME AND HOLD TIME FOR COUNT ENABLE AND PARALLEL ENABLE INPUTS, AND UP-DOWN CONTROL INPUTS


CP
1.3 V
1.3 V
ts(L)
th(L) = 0
ts(H)
th(H) = 0
SR OR PE
1.3 V
1.3 V
1.3 V
1.3 V
CP
1.3 V
1.3 V
1.3 V
ts(H)
th(H) = 0
ts(L)
th(L) = 0
CEP
1.3 V
1.3 V
1.3 V
1.3 V
ts(H)
th(H) = 0
ts(L)
th(L) = 0
CET
1.3 V
1.3 V
1.3 V
1.3 V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

UP-DOWN INPUT TO TERMINAL COUNT OUTPUT DELAYS

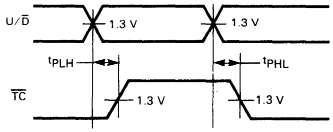

U/D
1.3 V
1.3 V
tPLH
tPHL
TC
1.3 V
1.3 V

Fig. 6

MOTOROLA

SN54/74LS170

4 x 4 REGISTER FILE OPEN-COLLECTOR

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN54LS/74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54LS/74LS670 provides a similar function to this device but it features 3-state outputs.

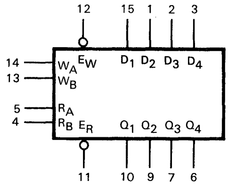
- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS OF n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

PIN NAMES **LOADING** (Note a)

		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_1-Q_4	Outputs (Note b)	Open-Collector	5(2.5)U.L.

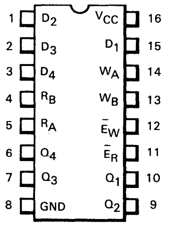
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5.0 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

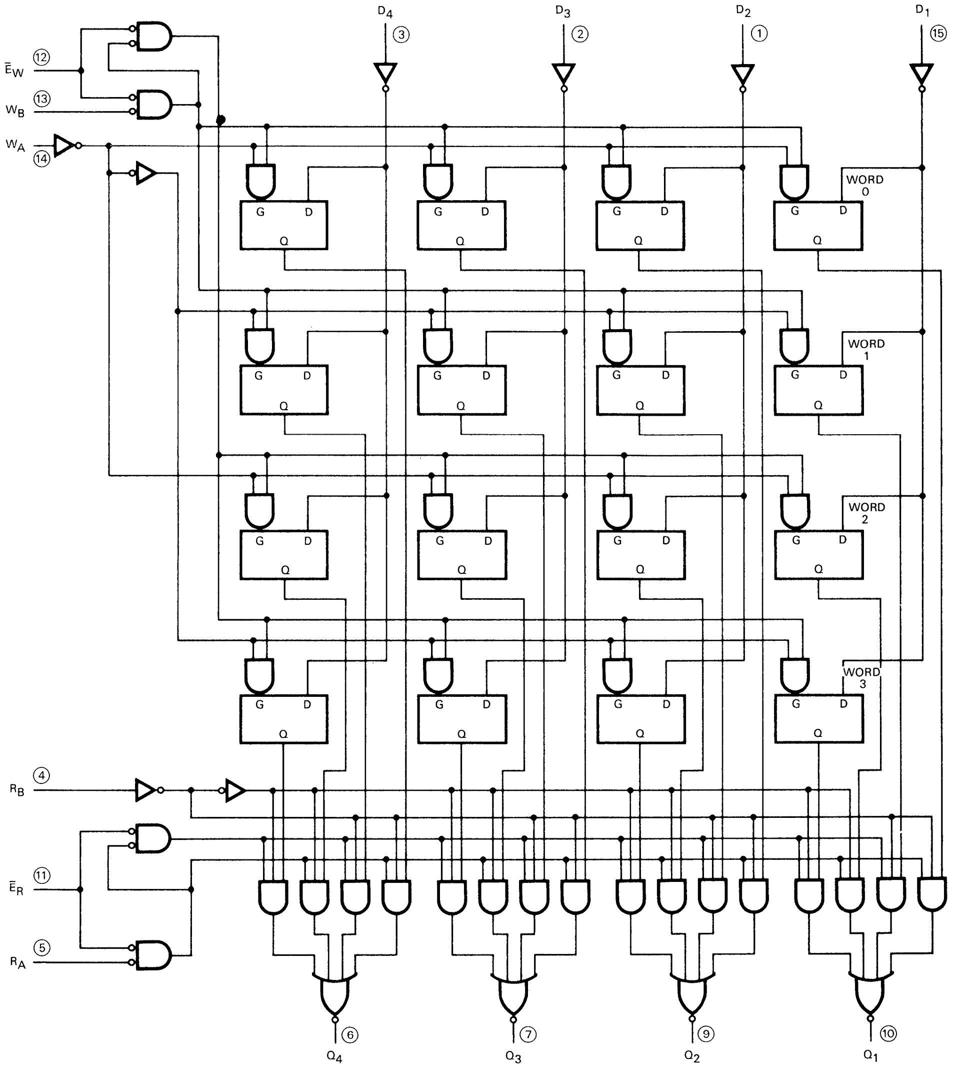
CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



D4
③
D3
②
D2
①
D1
⑮
$\bar{E}_W$
⑫
W_B
⑬
W_A
⑭
WORD 0
WORD 1
WORD 2
WORD 3
G
D
Q
R_B
④
$\bar{E}_R$
⑪
R_A
⑤
⑥
Q_4
⑦
Q_3
⑨
Q_2
⑩
Q_1

V_{CC} = Pin 16
GND = Pin 8
○=Pin Numbers

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	$\bar{E}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	$\bar{E}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level. L = low level, X = irreleveant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output High Current	54,74			100	μA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC}MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Any D, R, W $\bar{E}_R$, $\bar{E}_W$				20 40	μA	V_{CC} = MAX, V_{IN} = 2.4 V	
	Any D, R, W $\bar{E}_R$, $\bar{E}_W$				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Any D, R, W $\bar{E}_R$, $\bar{E}_W$				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current				40	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_R$ to Q Outputs		20 20	30 30	ns	Fig. 1	$V_{CC} = 5$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs		25 24	40 40	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_W$ to Q Outputs		30 26	45 40	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	ns	Fig. 1	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Pulse Width, $\overline{E}_R$, $\overline{E}_W$	25			ns	$V_{CC} = 5$ V $R_L = 2$ kΩ
t_s	Setup Time, Data to $\overline{E}_W$	10			ns	
t_s	Setup Time, W_A, W_B to $\overline{E}_W$	15			ns	
t_h	Hold Time, Data to $\overline{E}_W$	15			ns	
t_h	Hold Time, W_A, W_B to $\overline{E}_W$	5.0			ns	
t_{LATCH}	Latch Time	25			ns	

VOLTAGE WAVEFORMS

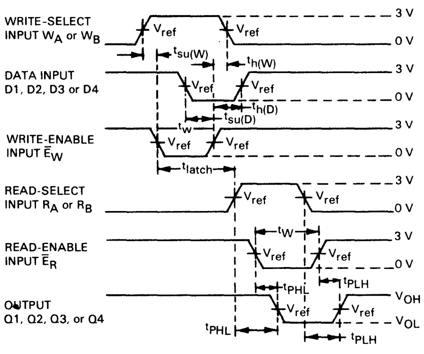

WRITE-SELECT INPUT W_A or W_B
DATA INPUT D1, D2, D3 or D4
WRITE-ENABLE INPUT $\overline{E}_W$
READ-SELECT INPUT R_A or R_B
READ-ENABLE INPUT $\overline{E}_R$
OUTPUT Q1, Q2, Q3, or Q4
V_{ref}
3 V
0 V
$t_{su(W)}$
$t_{h(W)}$
$t_{h(D)}$
$t_{su(D)}$
t_w
t_{latch}
t_W
t_{PHL}
t_{PLH}
V_{OH}
V_{OL}

Fig. 1

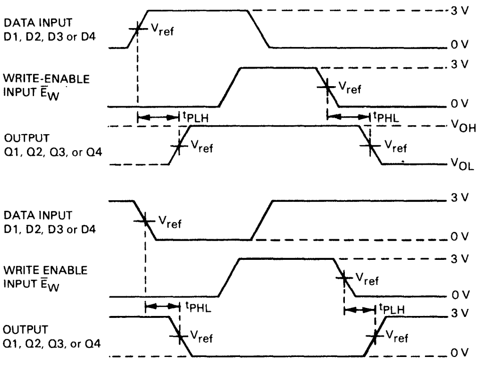

DATA INPUT D1, D2, D3 or D4
WRITE-ENABLE INPUT $\overline{E}_W$
OUTPUT Q1, Q2, Q3, or Q4
DATA INPUT D1, D2, D3 or D4
WRITE ENABLE INPUT $\overline{E}_W$
OUTPUT Q1, Q2, Q3, or Q4
V_{ref}
3 V
0 V
t_{PLH}
t_{PHL}
V_{OH}
V_{OL}

Fig. 2

MOTOROLA

SN54/74LS173A

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) brings the output to a high impedence state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

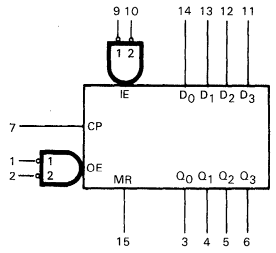
- **FULLY EDGE-TRIGGERED**
- **3-STATE OUTPUTS**
- **GATED INPUT AND OUTPUT ENABLES**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{IE}_1$-$\overline{IE}_2$	Input Enable (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{OE}_1$-$\overline{OE}_2$	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
CP	Clock Pulse (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset input (Active HIGH)	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Note b)	65(25)U.L.	15(7.5)U.L.

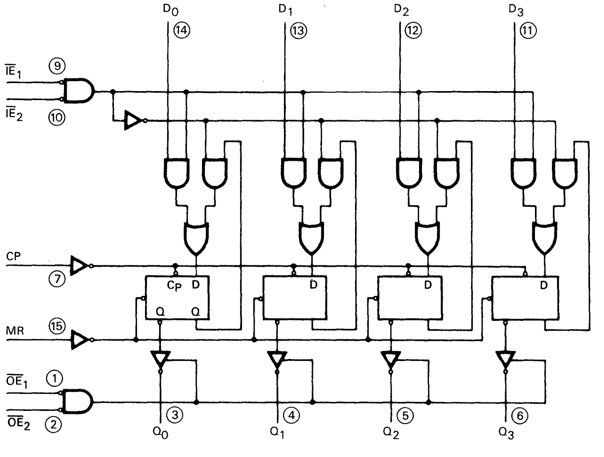
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


9 10
14 13 12 11
1 2
IE
D0 D1 D2 D3
7
CP
1
2
OE
MR
Q0 Q1 Q2 Q3
15
3 4 5 6

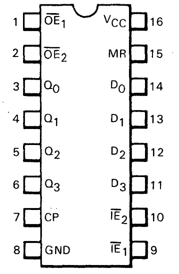
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM


D0
D1
D2
D3
⑭
⑬
⑫
⑪
IE1 ⑨
IE2 ⑩
CP
⑦
Cp D
Q Q
D
D
D
MR ⑮
OE1 ①
OE2 ②
③
④
⑤
⑥
Q0
Q1
Q2
Q3

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 OE1
2 OE2
3 Q0
4 Q1
5 Q2
6 Q3
7 CP
8 GND
VCC 16
MR 15
D0 14
D1 13
D2 12
D3 11
IE2 10
IE1 9

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

TRUTH TABLE

MR	CP	$\overline{IE}_1$	$\overline{IE}_2$	D_n	Q_n
H	x	x	x	x	L
L	L	x	x	x	Q_n
L	↑	H	x	x	Q_n
L	↑	x	H	x	Q_n
L	↑	L	L	L	L
L	↑	L	L	H	H

When either $\overline{OE}_1$ or $\overline{OE}_2$ are HIGH, the output is in the off state (High Impedence); however this does not affect the contents or sequential operation of the register.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_O = 2.7 V
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_O = 0.4 V
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				30	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Input Clock Frequency	30	50		MHz	V_{CC} = 5.0 V C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 22	25 30	ns	
t_{PHL}	Propagation Delay, MR To Output		26	35	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 18	23 27	ns	
t_{PLZ} t_{PHZ}	Output Disable Time		11 11	17 17	ns	C_L = 5.0 pF R_L = 667 Ω

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock or MR Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Data Enable Setup Time,	35			ns	
t_s	Data Setup Time	17			ns	
t_h	Hold Time, Any Input	0			ns	
t_{rec}	Recovery Time	10			ns	

AC WAVEFORMS

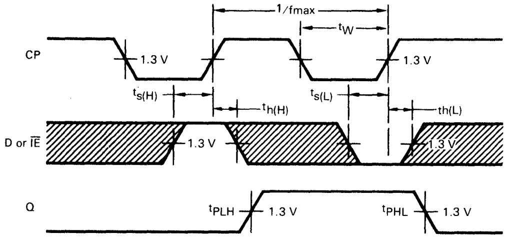

1/fmax
t_W
CP
1.3 V
1.3 V
$t_{s(H)}$
$t_{h(H)}$
$t_{s(L)}$
$t_{h(L)}$
D or $\overline{IE}$
1.3 V
1.3 V
Q
t_{PLH}
1.3 V
t_{PHL}
1.3 V

Fig. 1

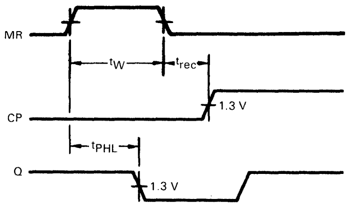

MR
t_W
t_{rec}
CP
1.3 V
t_{PHL}
Q
1.3 V

Fig. 2

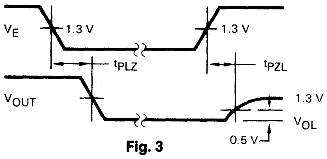

V_E
1.3 V
1.3 V
t_{PLZ}
t_{PZL}
V_{OUT}
1.3 V
V_{OL}
0.5 V

Fig. 3

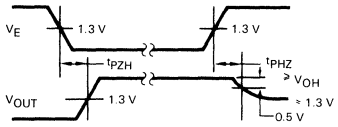
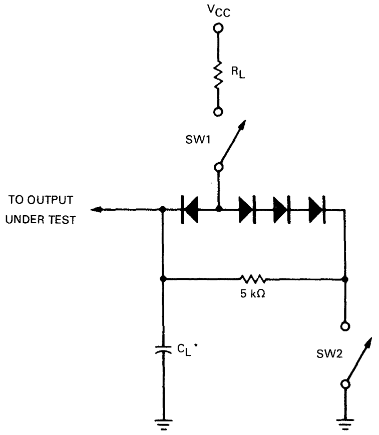

V_E
1.3 V
1.3 V
t_{PZH}
t_{PHZ}
$\geq V_{OH}$
V_{OUT}
1.3 V
≈ 1.3 V
0.5 V

Fig. 4

AC LOAD CIRCUIT

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed


V_{CC}
R_L
SW1
TO OUTPUT UNDER TEST
5 kΩ
C_L*
SW2

*Includes Jig and Probe Capacitance.

Fig. 5

MOTOROLA

SN54/74LS174

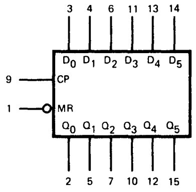
HEX D FLIP-FLOP

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL


3 4 6 11 13 14
D_0 D_1 D_2 D_3 D_4 D_5
9
CP
1
MR
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5
2 5 7 10 12 15

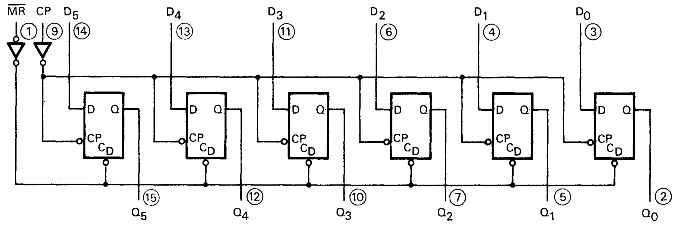
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_5$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_5$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

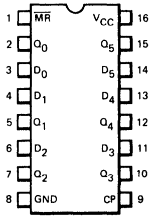
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM


$\overline{MR}$ CP D_5
①⑨⑭
D_4 ⑬
D_3 ⑪
D_2 ⑥
D_1 ④
D_0 ③
D Q
CP
C_D
⑮ Q_5
⑫ Q_4
⑩ Q_3
⑦ Q_2
⑤ Q_1
② Q_0

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)


1 $\overline{MR}$
2 Q_0
3 D_0
4 D_1
5 Q_1
6 D_2
7 Q_2
8 GND
16 V_{CC}
15 Q_5
14 D_5
13 D_4
12 Q_4
11 D_3
10 Q_3
9 CP

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				26	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

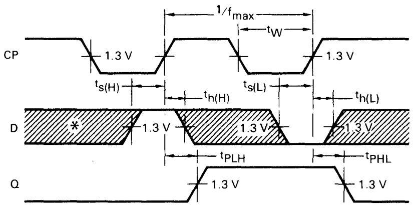
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Input Clock Frequency	30	40		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		23	35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 21	30 30	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock or $\overline{MR}$ Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	25			ns	

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

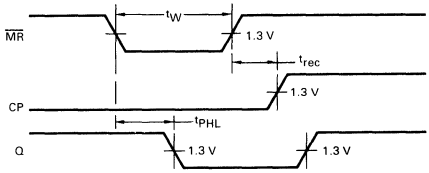


Fig. 2

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

MOTOROLA

SN54/74LS175

QUAD D FLIP-FLOP

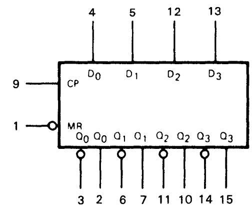
LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **CLOCK TO OUTPUT DELAYS OF 30 ns**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL


4
5
12
13
9
1
CP
D0
D1
D2
D3
MR
Q0
Q̄0
Q1
Q̄1
Q2
Q̄2
Q3
Q̄3
3
2
6
7
11
10
14
15

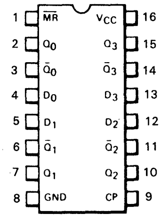
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

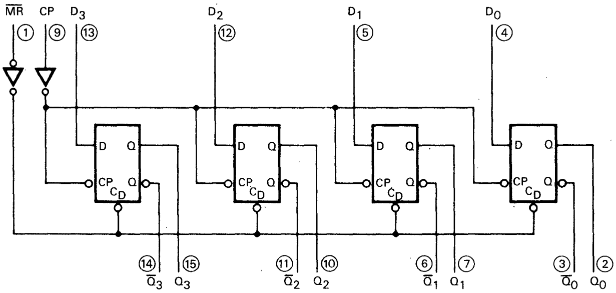
CONNECTION DIAGRAM DIP (TOP VIEW)


1
MR
2
Q0
3
Q̄0
4
D0
5
D1
6
Q̄1
7
Q1
8
GND
16
VCC
15
Q3
14
Q̄3
13
D3
12
D2
11
Q̄2
10
Q2
9
CP

J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


MR
CP
D3
D2
D1
D0
①
⑨
⑬
⑫
⑤
④
D
Q
CP
CD
Q̄
⑭
⑮
Q̄3
Q3
⑪
⑩
Q̄2
Q2
⑥
⑦
Q̄1
Q1
③
②
Q̄0
Q0

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				18	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

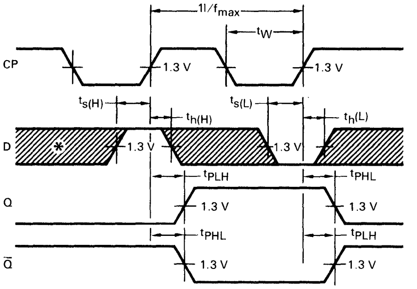
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Input Clock Frequency	30	40		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		20 20	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		13 16	25 25	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Clock or $\overline{MR}$ Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	25			ns	

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

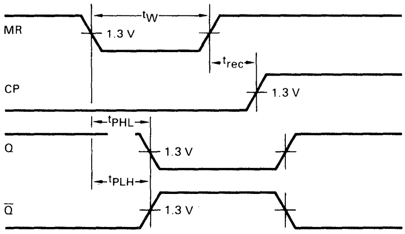


Fig. 2

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SN54/74LS181

4-BIT ARITHMETIC LOGIC UNIT

LOW POWER SCHOTTKY

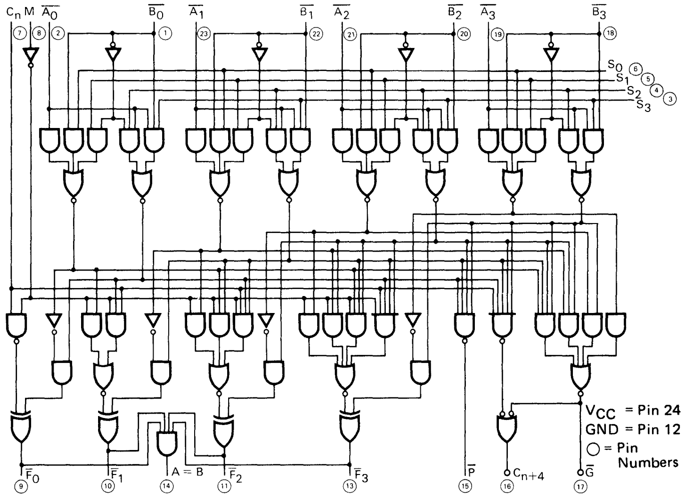
DESCRIPTION — The SN54LS/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- PROVIDES 16 ARITHMETIC OPERATIONS
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS
  TWELVE OTHER ARITHMETIC OPERATIONS
- PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES
  EXCLUSIVE—OR, COMPARE, AND, NAND, OR,
  NOR, PLUS TEN OTHER LOGIC OPERATIONS
- FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS
- INPUT CLAMP DIODES

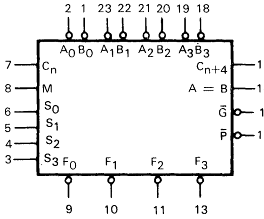
PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{A}_0$–$\overline{A}_3$, $\overline{B}_0$–$\overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L	0.75 U.L.
S_0–S_3	Function – Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
C_n	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0$–$\overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
A = B	Comparator Output	Open Collector	5 (2.5) U.L.
$\overline{G}$	Carry Generator (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

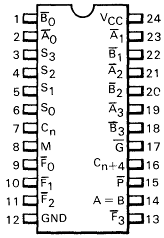

Cn M A0 B0 A1 B1 A2 B2 A3 B3
⑦ ⑧ ② ① ㉓ ㉒ ㉑ ⑳ ⑲ ⑱
S0 ⑥
S1 ⑤
S2 ④
S3 ③
F0 ⑨
F1 ⑩
A = B ⑭
F2 ⑪
F3 ⑬
P ⑮
Cn+4 ⑯
G ⑰
VCC = Pin 24
GND = Pin 12
○ = Pin Numbers

LOGIC SYMBOL


2 1 23 22 21 20 19 18
A0 B0 A1 B1 A2 B2 A3 B3
7 Cn
8 M
6 S0
5 S1
4 S2
3 S3
Cn+4 16
A = B 14
G 17
P 15
F0 F1 F2 F3
9 10 11 13

VCC = Pin 24
GND = Pin 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 B0
2 A0
3 S3
4 S2
5 S1
6 S0
7 Cn
8 M
9 F0
10 F1
11 F2
12 GND
24 VCC
23 A1
22 B1
21 A2
20 B2
19 A3
18 B3
17 G
16 Cn+4
15 P
14 A = B
13 F3

J Suffix — Case 623-05
(Ceramic)
N Suffix — Case 649-03
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs (S_0 . . . S_3) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate), $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of the four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A>B and A<B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L L H L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A + B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	$(A + \overline{B})$ plus A
H H H H	A	A	A	A minus 1

L = LOW Voltage Level

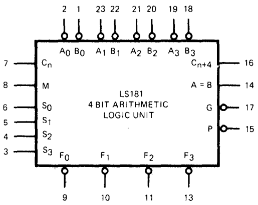
H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

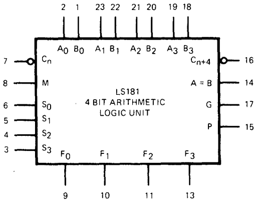
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	
V_{OH}	Output Voltage — High (A=B only)	54,74			5.5	V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
	Output $\overline{G}$	54,74			0.7	V	I_{OL} = 16 mA	
	Output $\overline{P}$	54			0.6	V	I_{OL} = 8.0 mA	
		74			0.5			
I_{OH}	Output HIGH Current	54,74			100	μA	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current							
	Mode Input				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Any $\overline{A}$ or $\overline{B}$ Input				60			
	Any S Input				80			
	C_n Input				100			
	Mode Input				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
	Any $\overline{A}$ or $\overline{B}$ Input				0.3			
	Any S Input				0.4			
	C_n Input				0.5			
I_{IL}	Input Low Current							
	Mode Input				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	Any $\overline{A}$ or $\overline{B}$ Input				−1.2			
	Any S Input				−1.6			
	C_n Input				−2.0			
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current See Note 1A	54			32	mA	V_{CC} = MAX	
		74			34			
	See Note 1B	54			35			
		74			37			

Note 1.
With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, Pin 12 = GND, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})	18 13	27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\bar{F}$ Outputs)	17 13	26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{G}$ Output)	19 15	29 23	ns	$M = S_1 = S_2 = 0$ V, $S_0 = S_3 = 4.5$ V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{G}$ Output)	21 21	32 32	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{P}$ Output)	20 20	30 30	ns	$M = S_1 = S_2 = 0$ V, $S_0 = S_3 = 4.5$ V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{P}$ Output)	20 22	30 33	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to any $\bar{F}$ Output)	21 13	32 20	ns	$M = S_1 = S_2 = 0$ V, $S_0 = S_3 = 4.5$ V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to any $\bar{F}$ Output)	21 21	32 32	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to $\bar{F}$ Outputs)	22 26	33 38	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to C_{n+4} Output)	25 25	38 38	ns	M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to C_{n+4} Output)	27 27	41 41	ns	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode)
t_{PLH} t_{PHL}	($\bar{A}$ or $\bar{B}$ Inputs to A = B Output)	33 41	50 62	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V $R_L = 2$ kΩ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

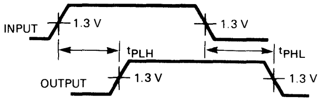


Fig. 4

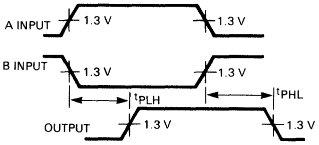


Fig. 5

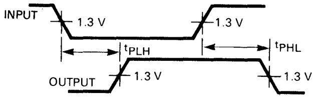


Fig. 6

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	None	$\overline{B}_I$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_I + 1$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_I + 1$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}_I$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_I$	$\overline{B}_I$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	$\overline{B}_I$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_I + 1$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_I + 1$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

MOTOROLA

SN54/74LS190
SN54/74LS191

PRESETTABLE BCD/DECADE UP/DOWN COUNTERS
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

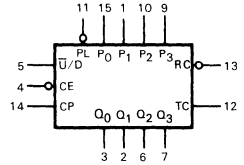
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54LS/74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}/D$) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

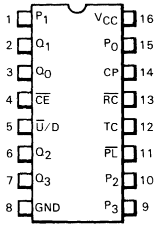
- **LOW POWER . . . 90 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 25 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **COUNT ENABLE AND UP/DOWN CONTROL INPUTS**
- **CASCADABLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

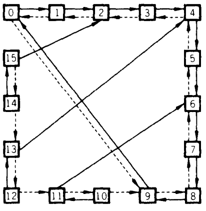
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CE}$	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{U}/D$	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{RC}$	Ripple Clock Output (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

STATE DIAGRAMS



190

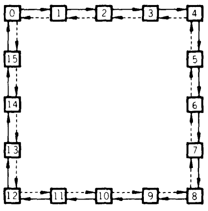
LS190

UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{\overline{U}/D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U}/D)$

LS191

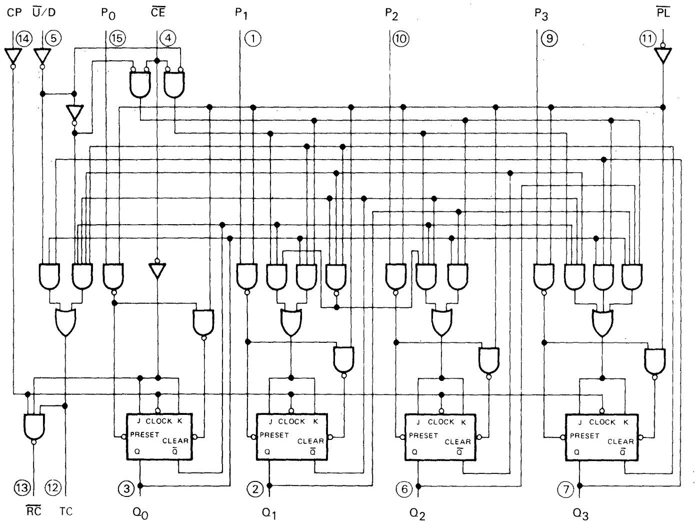
UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{\overline{U}/D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U}/D)$

Count Up ——
Count Down ------

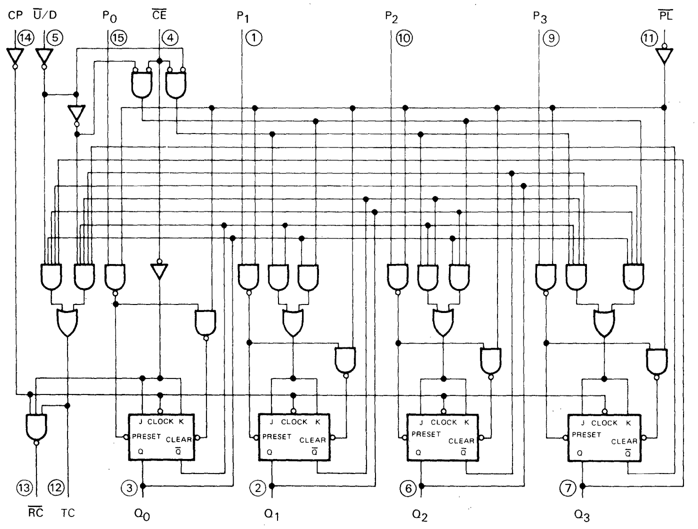


191

LOGIC DIAGRAMS


CP
Ū/D
P0
CE
P1
P2
P3
PL
⑭
⑤
⑮
④
①
⑩
⑨
⑪
J CLOCK K
PRESET
CLEAR
Q
Q̄
⑬
⑫
③
②
⑥
⑦
RC
TC
Q0
Q1
Q2
Q3

DECADE COUNTER
LS190


CP
Ū/D
P0
CE
P1
P2
P3
PL
⑭
⑤
⑮
④
①
⑩
⑨
⑪
J CLOCK K
PRESET
CLEAR
Q
Q̄
⑬
⑫
③
②
⑥
⑦
RC
TC
Q0
Q1
Q2
Q3

BINARY COUNTER
LS191

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{\text{PL}}$) input is LOW, information present on the Parallel Data inputs (P_0—P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{\text{CE}}$ input inhibits counting. When $\overline{\text{CE}}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{\text{U}}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{\text{CE}}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{\text{CE}}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{\text{U}}$/D signal should only be changed when either $\overline{\text{CE}}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{\text{U}}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{\text{RC}}$) output. The $\overline{\text{RC}}$ output is normally HIGH. When $\overline{\text{CE}}$ is LOW and TC is HIGH, the $\overline{\text{RC}}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each $\overline{\text{RC}}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{\text{CE}}$ inhibits the $\overline{\text{RC}}$ output pulse, as indicated in the $\overline{\text{RC}}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{\text{RC}}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{\text{RC}}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{\text{CE}}$ input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{\text{CE}}$.

MODE SELECT TABLE

INPUTS				MODE
$\overline{\text{PL}}$	$\overline{\text{CE}}$	$\overline{\text{U}}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			$\overline{\text{RC}}$
$\overline{\text{CE}}$	TC*	CP	OUTPUT
L	H	⊔	⊔
H	X	X	H
X	L	X	H

*TC is generated internally

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Clock Transition
⊔ = LOW Pulse

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0$ mA	
I_{IH}	Input HIGH Current Other Inputs $\overline{CE}$				20 60	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7$ V	
	Other Inputs $\overline{CE}$				0.1 0.3	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current Other Inputs $\overline{CE}$				−0.4 −1.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4$ V	
I_{OS}	Short Circuit Current		−20		−100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current				35	mA	$V_{CC} = \text{MAX}$	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	20	25		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ to Output Q		22 33	33 50	ns	
t_{PLH} t_{PHL}	Data to Output Q		20 27	32 40	ns	
t_{PLH} t_{PHL}	Clock to $\overline{RC}$		13 16	20 24	ns	
t_{PLH} t_{PHL}	Clock to Output Q		16 24	24 36	ns	
t_{PLH} t_{PHL}	Clock to TC		28 37	42 52	ns	
t_{PLH} t_{PHL}	$\overline{U}$/D to $\overline{RC}$		30 30	45 45	ns	
t_{PLH} t_{PHL}	$\overline{U}$/D to TC		21 22	33 33	ns	
t_{PLH} t_{PHL}	$\overline{CE}$ to $\overline{RC}$		21 22	33 33	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	CP Pulse Width	25			ns	$V_{CC} = 5.0$ V
t_W	$\overline{PL}$ Pulse Width	35			ns	
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	40			ns	

DEFINITIONS OF TERMS:

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

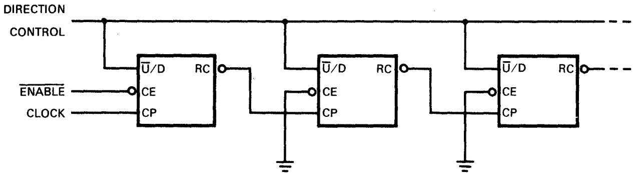

DIRECTION
CONTROL
ENABLE
CLOCK
U/D
RC
CE
CP

Fig. a) n-stage counter using ripple clock.

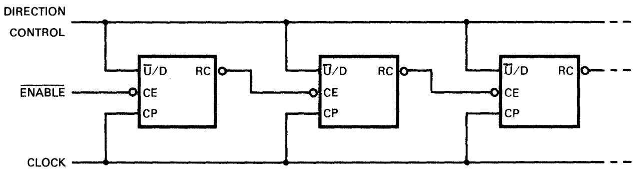

DIRECTION
CONTROL
ENABLE
CLOCK
U/D
RC
CE
CP

Fig. b) Synchronous n-stage counter using ripple carry/borrow.

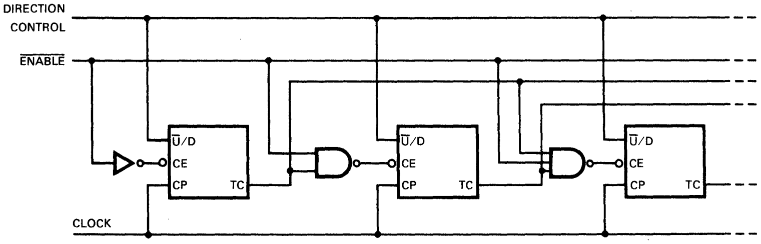

DIRECTION
CONTROL
ENABLE
CLOCK
U/D
CE
CP
TC

Fig. c) Synchronous n-stage counter with parallel gated carry/borrow.

AC WAVEFORMS

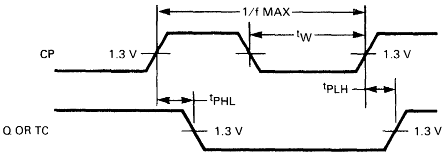

1/f MAX
tW
CP
1.3 V
1.3 V
tPHL
tPLH
Q OR TC
1.3 V
1.3 V

Fig. 1

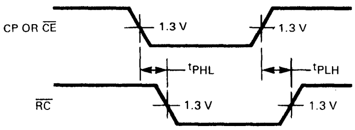
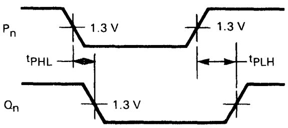

CP OR CE
1.3 V
1.3 V
tPHL
tPLH
RC
1.3 V
1.3 V

Fig. 2


Pn
1.3 V
1.3 V
tPHL
tPLH
Qn
1.3 V

NOTE: $\overline{PL}$ = LOW

Fig. 3

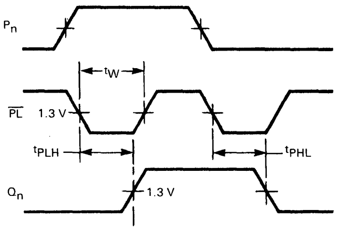

Pn
tW
PL
1.3 V
tPLH
tPHL
Qn
1.3 V

Fig. 4

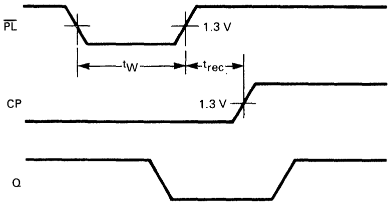
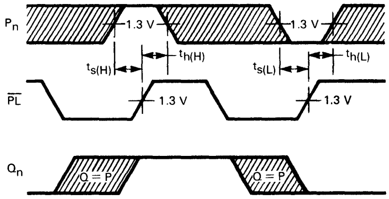

PL
1.3 V
tW
trec
CP
1.3 V
Q

Fig. 5


Pn
1.3 V
1.3 V
ts(H)
th(H)
ts(L)
th(L)
PL
1.3 V
1.3 V
Qn
Q = P
Q = P

*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

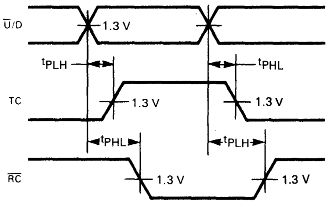

U/D
1.3 V
tPLH
tPHL
TC
1.3 V
1.3 V
tPHL
tPLH
RC
1.3 V
1.3 V

Fig. 7

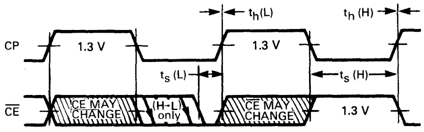

th(L)
th (H)
CP
1.3 V
1.3 V
ts (L)
ts (H)
CE
CE MAY CHANGE
(H-L) only
CE MAY CHANGE
1.3 V

Fig. 8

MOTOROLA

SN54/74LS192
SN54/74LS193

PRESETTABLE BCD/DECADE UP/DOWN COUNTER
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54LS/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

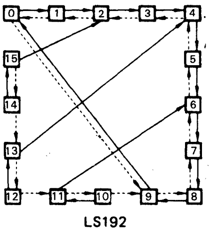
Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

- **LOW POWER . . . 95 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

STATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

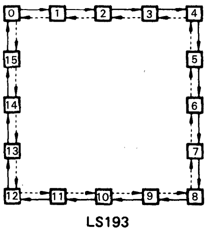
$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

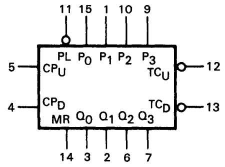
COUNT UP ——

COUNT DOWN ------



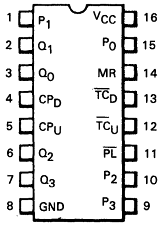
LS193

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

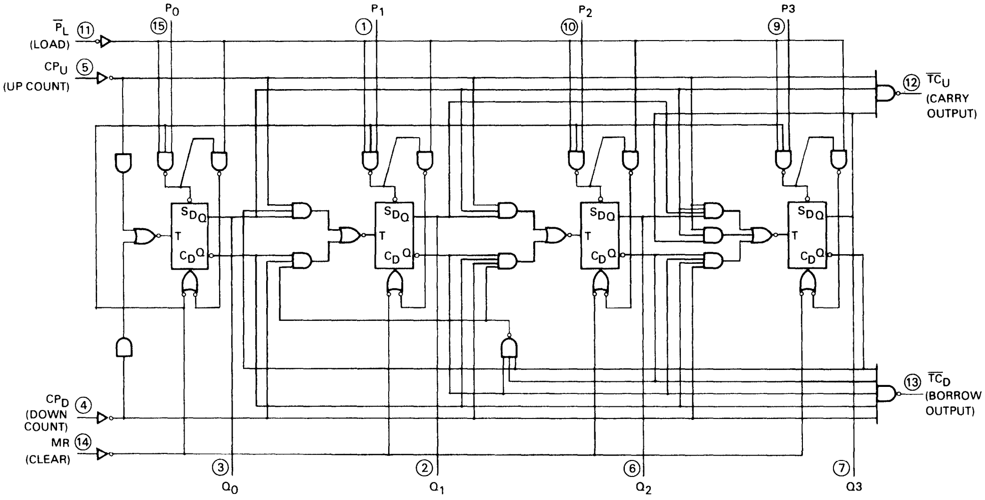
CONNECTION DIAGRAM
DIP (TOP VIEW)



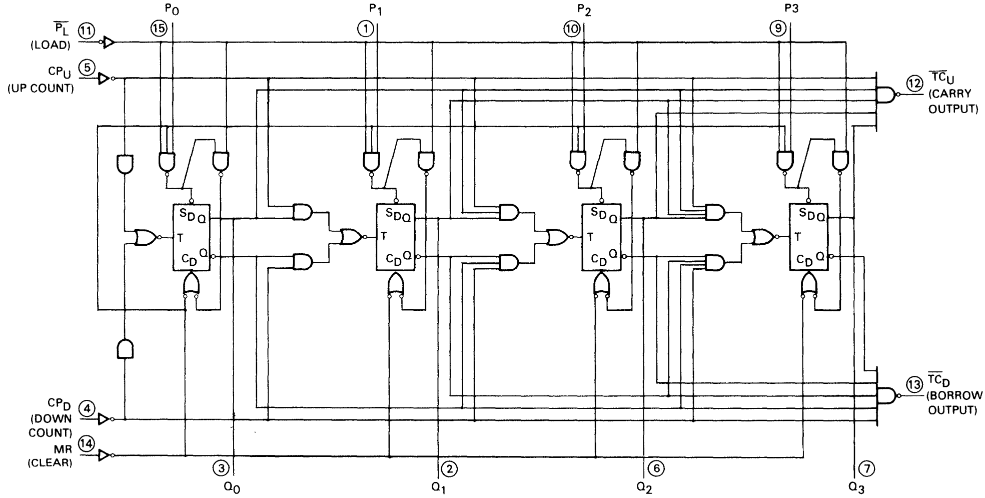
J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS


P0
P1
P2
P3
$\overline{P}_L$ ⑪
(LOAD)
CP_U ⑤
(UP COUNT)
⑮
①
⑩
⑨
⑫ $\overline{TC}_U$
(CARRY
OUTPUT)
S_D Q
T
C_D Q
CP_D ④
(DOWN
COUNT)
MR ⑭
(CLEAR)
⑬ $\overline{TC}_D$
(BORROW
OUTPUT)
③
②
⑥
⑦
Q0
Q1
Q2
Q3

LS192


P0
P1
P2
P3
$\overline{P}_L$ ⑪
(LOAD)
CP_U ⑤
(UP COUNT)
⑮
①
⑩
⑨
⑫ $\overline{TC}_U$
(CARRY
OUTPUT)
S_D Q
T
C_D Q
CP_D ④
(DOWN
COUNT)
MR ⑭
(CLEAR)
⑬ $\overline{TC}_D$
(BORROW
OUTPUT)
③
②
⑥
⑦
Q0
Q1
Q2
Q3

LS193

V_{CC} = Pin 16

GND = Pin 8

○ = Pin Number

FUNCTIONAL DESCRIPTION — The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	ʃ	H	Count Up
L	H	H	ʃ	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
ʃ = LOW-to-HIGH Clock Transition

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	CP_U Input to		17	26	ns	
t_{PHL}	$\overline{TC}_U$ Output		18	24		
t_{PLH}	CP_D Input to		16	24	ns	
t_{PHL}	$\overline{TC}_D$ Output		15	24		
t_{PLH}	Clock to Q		27	38	ns	
t_{PHL}			30	47		
t_{PLH}	$\overline{PL}$ to Q		24	40	ns	
t_{PHL}			25	40		
t_{PHL}	MR Input to Any Output		23	35	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Any Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	40			ns	

DEFINITIONS OF TERMS:

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{PL}$ transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

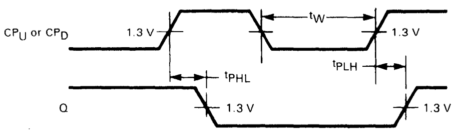

CP_U or CP_D
1.3 V
t_W
1.3 V
t_{PLH}
t_{PHL}
Q
1.3 V
1.3 V

Fig. 1

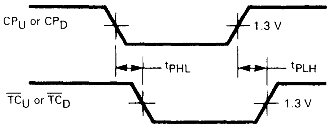
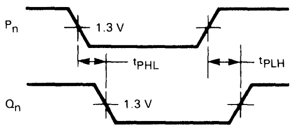

CP_U or CP_D
1.3 V
t_{PHL}
t_{PLH}
$\overline{TC}_U$ or $\overline{TC}_D$
1.3 V

Fig. 2


P_n
1.3 V
t_{PHL}
t_{PLH}
Q_n
1.3 V

NOTE: $\overline{PL}$ = LOW

Fig. 3

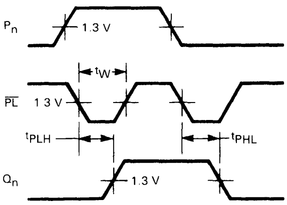

P_n
1.3 V
t_W
$\overline{PL}$
1.3 V
t_{PLH}
t_{PHL}
Q_n
1.3 V

Fig. 4

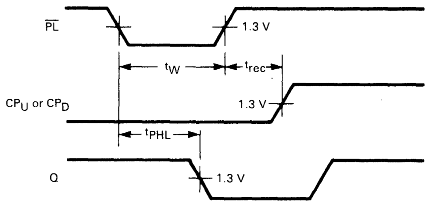
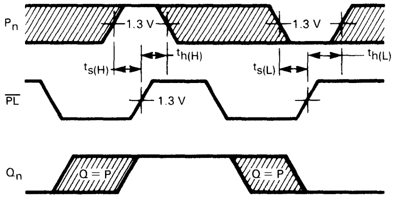

$\overline{PL}$
1.3 V
t_W
t_{rec}
CP_U or CP_D
1.3 V
t_{PHL}
Q
1.3 V

Fig. 5


P_n
1.3 V
1.3 V
$t_{s(H)}$
$t_{h(H)}$
$t_{s(L)}$
$t_{h(L)}$
$\overline{PL}$
1.3 V
Q_n
Q = P
Q = P

*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

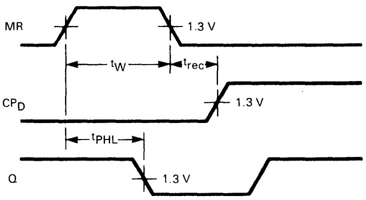

MR
1.3 V
t_W
t_{rec}
CP_U or CP_D
1.3 V
t_{PHL}
Q
1.3 V

Fig. 7

MOTOROLA

SN54/74LS194A

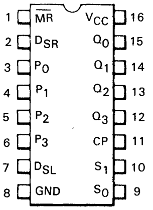
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

- **TYPICAL SHIFT FREQUENCY OF 36 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 $\overline{MR}$
2 D_{SR}
3 P_0
4 P_1
5 P_2
6 P_3
7 D_{SL}
8 GND
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 CP
10 S_1
9 S_0

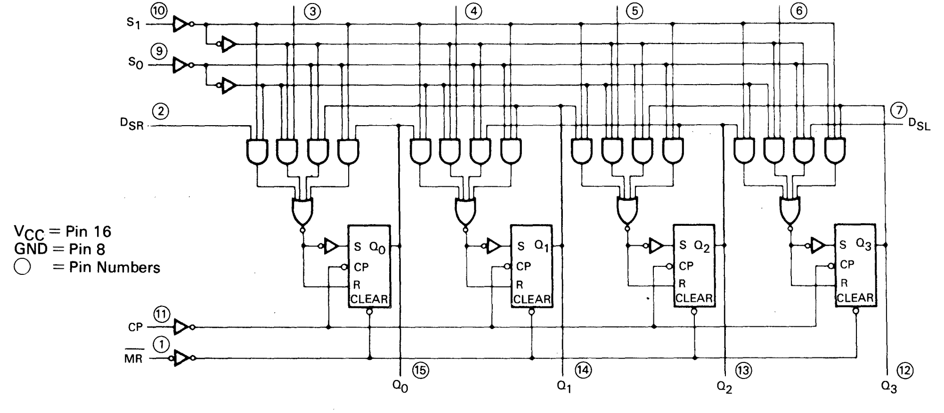
J Suffix — Case 620-09
Ceramic
N Suffix — Case 648-08
(Plastic)

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0, S_1	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
D_{SR}	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D_{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM


P_0 ③
P_1 ④
P_2 ⑤
P_3 ⑥
S_1 ⑩
S_0 ⑨
D_{SR} ②
⑦ D_{SL}
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers
S Q_0 CP R CLEAR
S Q_1 CP R CLEAR
S Q_2 CP R CLEAR
S Q_3 CP R CLEAR
CP ⑪
$\overline{MR}$ ①
⑮ Q_0
⑭ Q_1
⑬ Q_2
⑫ Q_3

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the Motorola LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1. All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2, and P_3 inputs is transferred to the Q_0, Q_1, Q_2, and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.

4. The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

2. D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	P_n	P_0	P_1	P_2	P_3

L = LOW Voltage Level
H= HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				23	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	36		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		14 17	22 26	ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		19	30	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock or $\overline{MR}$ Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Mode Control Setup Time	30			ns	
t_s	Data Setup Time	20			ns	
t_h	Hold Time, Any Input	0			ns	
t_{rec}	Recovery Time	25			ns	

DEFINITIONS OF TERMS:

SET UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

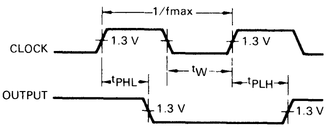
HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEVFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

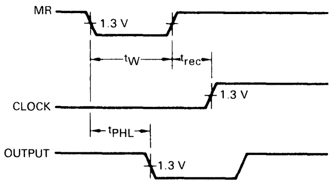
CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH AND f_{max}


1/fmax
CLOCK
1.3 V
1.3 V
t_{PHL}
t_W
t_{PLH}
OUTPUT
1.3 V
1.3 V

OTHER CONDITIONS: $S_1 = L$, $\overline{MR} = H$, $S_0 = H$

Fig. 1

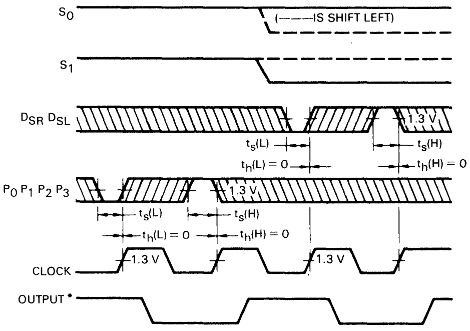
MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME


MR
1.3 V
t_W
t_{rec}
CLOCK
1.3 V
t_{PHL}
OUTPUT
1.3 V

OTHER CONDITIONS: $S_0, S_1 = H$
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 2

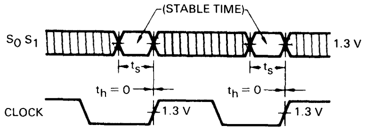
SETUP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)


S_0
(------IS SHIFT LEFT)
S_1
D_{SR} D_{SL}
1.3 V
$t_s(L)$
$t_s(H)$
$t_h(L) = 0$
$t_h(H) = 0$
P_0 P_1 P_2 P_3
1.3 V
$t_s(L)$
$t_s(H)$
$t_h(L) = 0$
$t_h(H) = 0$
CLOCK
1.3 V
1.3 V
OUTPUT *

OTHER CONDITIONS: $\overline{MR} = H$
*D_{SR} set-up time affects Q_0 only
D_{SL} set-up time affects Q_3 only

Fig. 3

SETUP (t_s) AND HOLD (t_h) TIME FOR S INPUT


(STABLE TIME)
S_0 S_1
1.3 V
t_s
t_s
$t_h = 0$
$t_h = 0$
CLOCK
1.3 V
1.3 V

OTHER CONDITIONS: $\overline{MR} = H$

Fig. 4

MOTOROLA

SN54/74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

LOW POWER SCHOTTKY

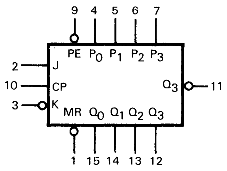
DESCRIPTION — The SN54LS/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- **TYPICAL SHIFT RIGHT FREQUENCY OF 39 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 — P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 — Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

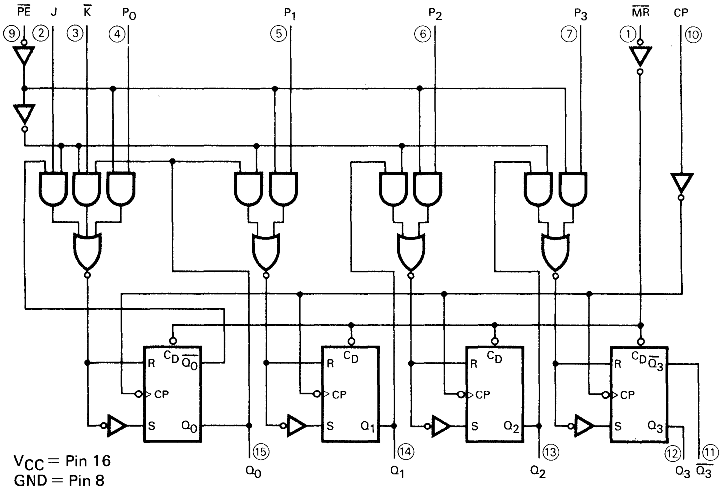
LOGIC SYMBOL



9 4 5 6 7
PE P0 P1 P2 P3
2 J
10 CP
3 K
Q3 11
MR Q0 Q1 Q2 Q3
1 15 14 13 12

V_{CC} = Pin 16
GND = Pin 8

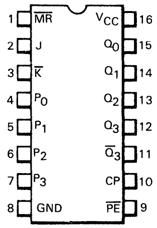
LOGIC DIAGRAM



PE J K P0 P1 P2 P3 MR CP
9 2 3 4 5 6 7 1 10
R CD Q0 CP S Q0
R CD CP S Q1
R CD CP S Q2
R CD Q3 CP S Q3
15 14 13 12 11
Q0 Q1 Q2 Q3 Q3

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



1 MR
2 J
3 K
4 P0
5 P1
6 P2
7 P3
8 GND
VCC 16
Q0 15
Q1 14
Q2 13
Q3 12
Q3 11
CP 10
PE 9

J Suffix — Case 620-09 Ceramic
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	P_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				21	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	39		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to Output		14 17	22 26	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Output		19	30	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	CP Clock Pulse Width	16			ns	V_{CC} = 5.0 V
t_W	$\overline{MR}$ Pulse Width	12			ns	
t_s	$\overline{PE}$ Setup Time	25			ns	
t_s	Data Setup Time	15			ns	
t_{rec}	Recovery Time	25			ns	
t_{rel}	$\overline{PE}$ Release Time			10	ns	
t_h	Data Hold Time	0			ns	

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

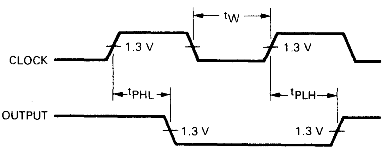
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

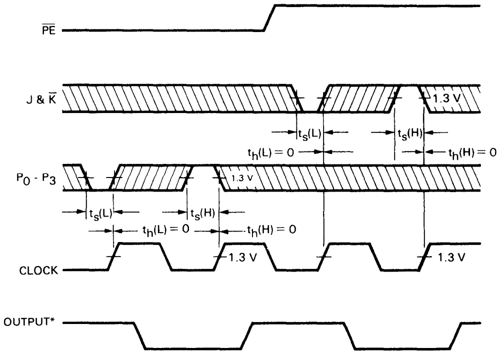


tW
CLOCK
1.3 V
1.3 V
tPHL
tPLH
OUTPUT
1.3 V
1.3 V

CONDITIONS: J = $\overline{\text{PE}}$ = $\overline{\text{MR}}$ = H
$\overline{\text{K}}$ = L

Fig. 1

SETUP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{\text{K}}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)

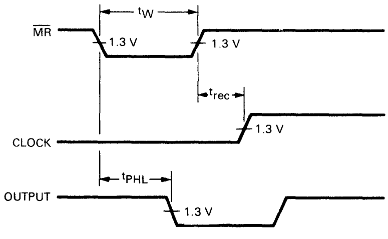


PE
J & K
1.3 V
ts(L)
ts(H)
th(L) = 0
th(H) = 0
P0 - P3
1.3 V
ts(L)
ts(H)
th(L) = 0
th(H) = 0
CLOCK
1.3 V
1.3 V
OUTPUT*

CONDITIONS: $\overline{\text{MR}}$ = H
*J and $\overline{\text{K}}$ set-up time affects Q_0 only

Fig. 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

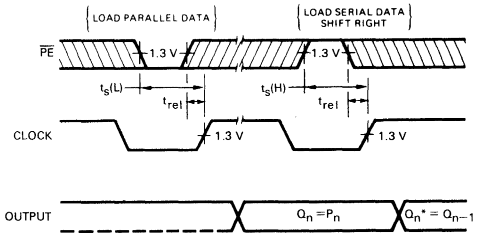


tW
MR
1.3 V
1.3 V
trec
CLOCK
1.3 V
tPHL
OUTPUT
1.3 V

CONDITIONS: $\overline{\text{PE}}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 3

SETUP (t_s) AND HOLD (t_h) TIME FOR $\overline{\text{PE}}$ INPUT



LOAD PARALLEL DATA
LOAD SERIAL DATA SHIFT RIGHT
PE
1.3 V
1.3 V
ts(L)
trel
ts(H)
trel
CLOCK
1.3 V
1.3 V
OUTPUT
Qn = Pn
Qn* = Qn−1

CONDITIONS: $\overline{\text{MR}}$ = H
*Q_0 state will be determined by J and $\overline{\text{K}}$ inputs

Fig. 4

MOTOROLA

SN54/74LS196
SN54/74LS197

4-STAGE PRESETTABLE RIPPLE COUNTERS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8,4,2,1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54LS/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

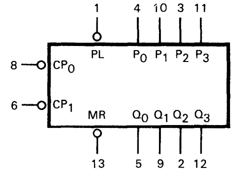
- **LOW POWER CONSUMPTION — TYPICALLY 80 mW**
- **HIGH COUNTING RATES — TYPICALLY 70 MHz**
- **CHOICE OF COUNTING MODES — BCD, BI-QUINARY, BINARY**
- **ASYNCHRONOUS PRESETTABLE**
- **ASYNCHRONOUS MASTER RESET**
- **EASY MULTISTAGE CASCADING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES **LOADING** (Note a)

		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section	1.0 U.L.	1.5 U.L.
$\overline{CP}_1$ (LS196)	Clock (Active LOW Going Edge) Input to Divide-by-Five Section	2.0 U.L.	1.75 U.L.
$\overline{CP}_1$ (LS197)	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	0.8 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{PL}$	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Notes b, c)	10 U.L.	5(2.5) U.L.

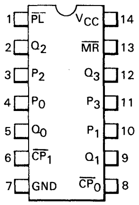
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. In addition to loading shown, Q_0 can also drive $\overline{CP}_1$.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

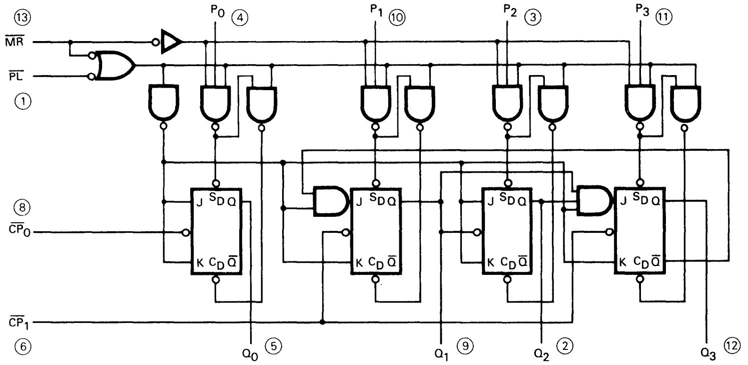
CONNECTION DIAGRAM
DIP (TOP VIEW)



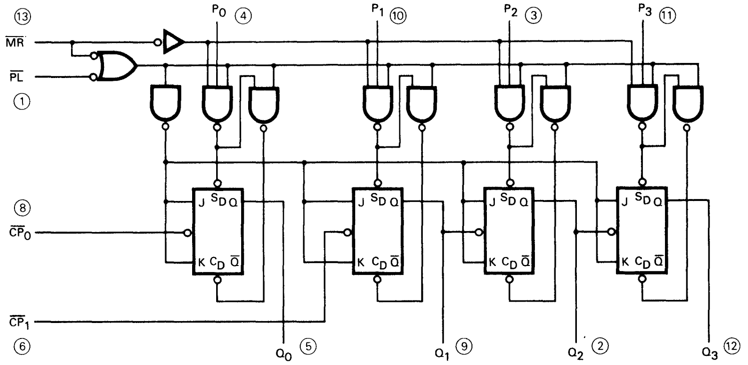
J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


⑬
MR
PL
①
P0 ④
P1 ⑩
P2 ③
P3 ⑪
J SD Q
K CD Q̄
⑧
CP0
CP1
⑥
Q0 ⑤
Q1 ⑨
Q2 ②
Q3 ⑫

LS196


⑬
MR
PL
①
P0 ④
P1 ⑩
P2 ③
P3 ⑪
J SD Q
K CD Q̄
⑧
CP0
CP1
⑥
Q0 ⑤
Q1 ⑨
Q2 ②
Q3 ⑫

LS197

V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP_0}$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP_1}$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP_1}$ input. With the input frequency connected to $\overline{CP_0}$ and Q_0 driving $\overline{CP_1}$, the LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to $\overline{CP_1}$ and Q_3 driving $\overline{CP_0}$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P_0—P_3) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

Figure 2: LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:
1. Signal applied to CP_0, Q_0 connected to CP_1.
2. Signal applied to CP_1, Q_3 connected to CP_0.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⎺⎽	Count

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⎺⎽ = HIGH to Low Clock Transition

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Data, $\overline{PL}$ $\overline{MR}$, $\overline{CP}_0$ (LS196) $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)				20 40 40 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, $\overline{PL}$ $\overline{MR}$, $\overline{CP}_0$ (LS196) $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)				0.1 0.2 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, $\overline{PL}$ $\overline{MR}$ $\overline{CP}_0$ $\overline{CP}_1$ (LS196) $\overline{CP}_1$ (LS197)				−0.4 −0.8 −2.4 −2.8 −1.3	mA	V_{CC} = MAX = V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS196			LS197				
		MIN	TYP	MAX	MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	40		30	40		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_0 Output		8.0 13	15 20		8.0 14	15 21	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		16 22	24 33		12 23	19 35	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		38 41	57 62		34 42	51 63	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		12 30	18 45		55 63	78 95	ns	
t_{PLH} t_{PHL}	Data to Output		20 29	30 44		18 29	27 44	ns	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		27 30	41 45		26 30	39 45	ns	
t_{PHL}	$\overline{MR}$ Input to Any Output		34	51		34	51	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS196			LS197				
		MIN	TYP	MAX	MIN	TYP	MAX		
t_W	$\overline{CP}_0$ Pulse Width	20			20			ns	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_1$ Pulse Width	30			30			ns	
t_W	$\overline{PL}$ Pulse Width	20			20			ns	
t_W	$\overline{MR}$ Pulse Width	15			15			ns	
t_s	Data Input Setup Time — HIGH	10			10			ns	
t_s	Data Input Setup Time — LOW	15			15			ns	
t_h	Data Hold Time — HIGH	10			10			ns	
t_h	Data Hold Time — LOW	10			10			ns	
t_{rec}	Recovery Time	30			30			ns	

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

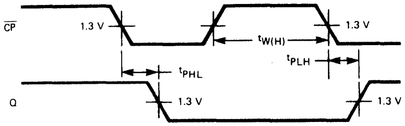
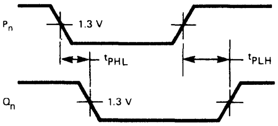

CP
1.3 V
1.3 V
tW(H)
tPLH
tPHL
Q
1.3 V
1.3 V

Fig. 1


Pn
1.3 V
tPHL
tPLH
Qn
1.3 V

NOTE: $\overline{PL}$ = LOW

Fig. 2

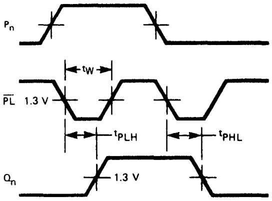

Pn
tW
PL 1.3 V
tPLH
tPHL
Qn
1.3 V

Fig. 3

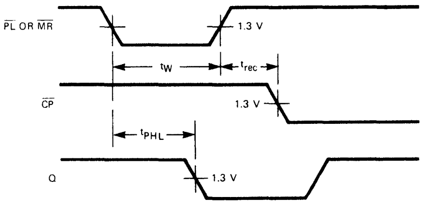
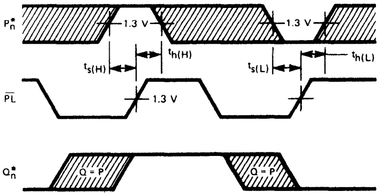

PL OR MR
1.3 V
tW
trec
CP
1.3 V
tPHL
Q
1.3 V

Fig. 4


Pn*
1.3 V
1.3 V
th(H)
ts(H)
ts(L)
th(L)
PL
1.3 V
Qn*
Q = P
Q = P

*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

MOTOROLA

SN54/74LS221

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

LOW POWER SCHOTTKY

DESCRIPTION — Each multivibrator of the LS221 features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1 volt/second, providing the circuit with excellent noise immunity. A high immunity to V_{CC} noise is also provided by internal latching circuitry.

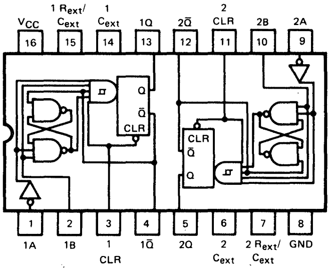
Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With $R_{ext} = 2\ k\Omega$ and $C_{ext} = 0$, a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for greater than six decades of timing capacitance (10pF to 10 μF), and greater than one decade of timing resistance (2 to 70 kΩ for the SN54LS221, and 2 to 100 kΩ for the SN74LS221). Pulse width is defined by the relationship: $t_W(out) = C_{ext}R_{ext} \ln 2 \approx 0.7\ C_{ext}R_{ext}$. If pulse cutoff is not critical, capacitance up to 1000 μF and resistance as low as 1.4 kΩ may be used. The range of jitter-free pulse widths is extended if V_{CC} is 5 V and 25°C temperature.

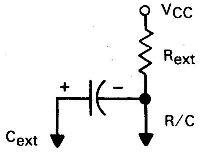
- **SN54LS221 and SN74LS221 IS A DUAL HIGHLY STABLE ONE-SHOT**
- **OVERRIDING CLEAR TERMINATES OUTPUT PULSE**
- **PIN OUT IS IDENTICAL TO SN54LS/74LS123**

(TOP VIEW)



positive logic: Low input to clear resets Q low and Q̄ high regardless of d-c levels at A or B inputs.

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)



FUNCTION TABLE

(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

Once in the pulse trigger mode, the output pulse width is determined by $t_W = R_{ext}C_{ext}\ln 2$, as long as R_{ext} and C_{ext} are within their minimum and maximum valves and the duty cycle is less than 50%. This pulse width is essentially independent of V_{CC} and temperature variations. Output pulse widths varies typically no more than ±0.5% from device to device.

If the duty cycle, defined as being $100 \bullet \frac{t_W}{T}$ where T is the period of the input pulse, rises above 50%, the output pulse width will become shorter. If the duty cycle varies between low and high valves, this causes the output pulse width to vary in length, or jitter. To reduce jitter to a minimum, R_{ext} should be as large as possible. (Jitter is independent of C_{ext}). With $R_{ext} = 100K$, jitter is not appreciable until the duty cycle approaches 90%.

Although the LS221 is pin-for-pin compatible with the LS123, it should be remembered that they are not functionally identical. The LS123 is retriggerable so that the output is dependent upon the input transitions once it is high. This is not the case for the LS221. Also note that it is recommended to externally ground the LS123 C_{ext} pin. However, this cannot be done on the LS221.

The SN54LS/74LS221 is a dual, monolithic, non-retriggerable, high-stability one shot. The output pulse width, t_W can be varied over 9 decades of timing by proper selection of the external timing components, R_{ext} and C_{ext}.

Pulse triggering occurs at a voltage level and is, therefore, independent of the input slew rate. Although all three inputs have this Schmitt-trigger effect, only the B input should be used for very long transition triggers ($\geqslant 1.0\,\mu V/s$). High immunity to V_{CC} noise (typically 1.5 V) is achieved by internal latching circuitry. However, standard V_{CC} bypassing is strongly recommended.

The LS221 has four basic modes of operation.

Clear Mode: If the clear input is held low, irregardless of the previous output state and other input states, the Q output is low.

Inhibit Mode: If either the A input is high or the B input is low, once the Q output goes low, it cannot be retriggered by other inputs.

Pulse Trigger Mode: This occurs when none of the other modes are in effect and the Q output is low. A proper transition by either the CLR, A or B input, as shown in the truth table, will cause the Q output to go high and remain high for the pulse time t_W.

Once triggered, as long as the output remains high, all input transitions (except for Clear, see Note 4) are ignored.

Overriding Clear Mode: If the Q output is high, it may be forced low by bringing the clear input low.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{T+}	Positive-Going Threshold Voltage at A Input			1.0	2.0	V	V_{CC} = MIN
V_{T-}	Negative-Going Threshold Voltage at A Input	54	0.7	1.0		V	V_{CC} = MIN
		74	0.8	1.0		V	
V_{T+}	Positive-Going Threshold Voltage at B Input			1.0	2.0	V	V_{CC} = MIN
V_{T-}	Negative-Going Threshold Voltage at B Input	54	0.7	0.9		V	V_{CC} = MIN
		74	0.8	0.9		V	
V_{IK}	Input Clamp Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX
		74	2.7	3.4		V	
V_{OL}	Output LOW Voltage	54		0.25	0.4	V	I_{OL} = 4.0 mA, V_{CC} = MIN
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current Input A Input B Clear				 −0.4 −0.8 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Quiescent			4.7	11	mA	V_{CC} = MAX
	Triggered			19	27		

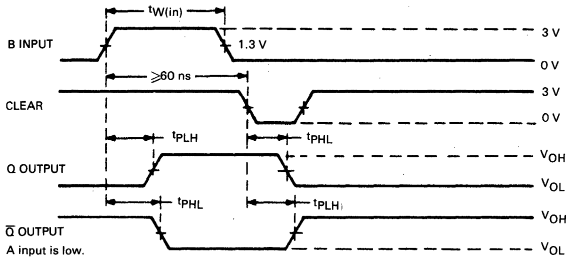
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX			
t_{PLH}	A	Q		45	70	ns	C_L=15 pF, See Figure 1	C_{ext} = 80 pF, R_{ext} = 2 kΩ
	B	Q		35	55			
t_{PHL}	A	$\overline{Q}$		50	80	ns		
	B	$\overline{Q}$		40	65			
t_{PHL}	Clear	Q		35	55	ns		
t_{PLH}	Clear	$\overline{Q}$		44	65	ns		
$t_{W(out)}$	A or B	Q or $\overline{Q}$	70	120	150	ns		C_{ext} = 80 pF, R_{ext} = 2 Ω
			20	47	70			C_{ext} = 0, R_{ext} = 2 kΩ
			600	670	750			C_{ext} = 100 pF, R_{ext} = 10 kΩ
			6	6.9	7.5	ms		C_{ext} = 1 µF, R_{ext} = 10 kΩ

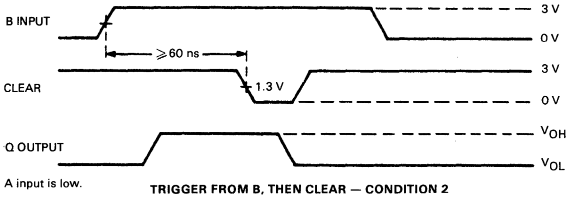
AC SETUP REQUIREMENTS V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER		LIMITS			UNITS
			MIN	TYP	MAX	
dv/dt	Rate of Rise or Fall of Input Pulse					
	Schmitt, B		1.0			V/s
	Logic Input, A		1.0			V/µs
t_W	Input Pulse Width					
	A or B, $t_{W(in)}$		40			ns
	Clear, t_W (clear)		40			
t_s	Clear-Inactive-State Setup Time		15			ns
R_{ext}	External Timing Resistance	54	1.4		70	kΩ
		74	1.4		100	
C_{ext}	External Timing Capacitance		0		1000	µF
	Output Duty Cycle					
	RT = 2.0 kΩ				50	%
	R_T = MAX R_{ext}				90	

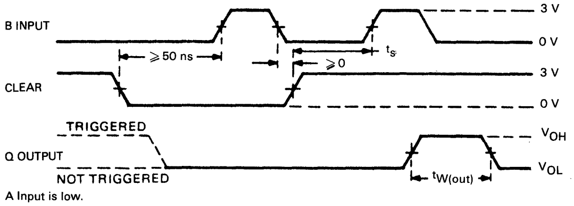
AC WAVEFORMS


tW(in)
B INPUT
1.3 V
3 V
0 V
≥60 ns
CLEAR
3 V
0 V
tPLH
tPHL
Q OUTPUT
VOH
VOL
tPHL
tPLH
Q̄ OUTPUT
VOH
VOL
A input is low.

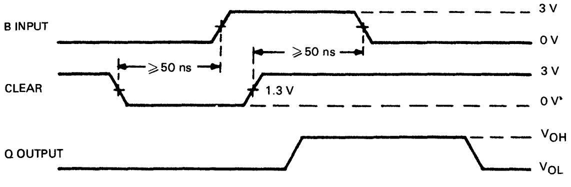
TRIGGER FROM B, THEN CLEAR — CONDITION 1


B INPUT
3 V
0 V
≥60 ns
CLEAR
1.3 V
3 V
0 V
Q OUTPUT
VOH
VOL
A input is low.

TRIGGER FROM B, THEN CLEAR — CONDITION 2


B INPUT
3 V
0 V
≥50 ns
ts
≥0
CLEAR
3 V
0 V
TRIGGERED
Q OUTPUT
NOT TRIGGERED
VOH
VOL
tW(out)
A Input is low.

CLEAR OVERRIDING B, THEN TRIGGER FROM B


B INPUT
3 V
0 V
≥50 ns
≥50 ns
CLEAR
1.3 V
3 V
0 V*
Q OUTPUT
VOH
VOL
A input is low.

TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

Fig. 1

MOTOROLA

SN54/74LS240
SN54/74LS241
SN54/74LS244

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

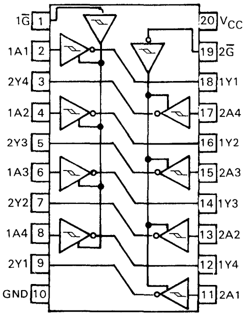
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS240, 241 and 244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

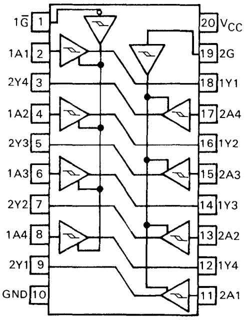
- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS
- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

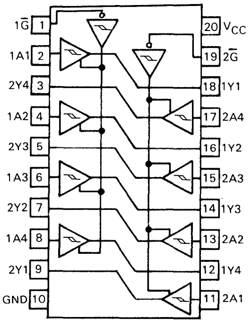
SN54LS/74LS240


1G̅ 1
1A1 2
2Y4 3
1A2 4
2Y3 5
1A3 6
2Y2 7
1A4 8
2Y1 9
GND 10
20 VCC
19 2G̅
18 1Y1
17 2A4
16 1Y2
15 2A3
14 1Y3
13 2A2
12 1Y4
11 2A1

SN54LS/74LS241


1G̅ 1
1A1 2
2Y4 3
1A2 4
2Y3 5
1A3 6
2Y2 7
1A4 8
2Y1 9
GND 10
20 VCC
19 2G
18 1Y1
17 2A4
16 1Y2
15 2A3
14 1Y3
13 2A2
12 1Y4
11 2A1

SN54LS/74LS244


1G̅ 1
1A1 2
2Y4 3
1A2 4
2Y3 5
1A3 6
2Y2 7
1A4 8
2Y1 9
GND 10
20 VCC
19 2G̅
18 1Y1
17 2A4
16 1Y2
15 2A3
14 1Y3
13 2A2
12 1Y4
11 2A1

TRUTH TABLES

SN54LS/74LS240

INPUTS		OUTPUT
$\overline{1G}$,$\overline{2G}$	D	
L	L	H
L	H	L
H	X	(Z)

SN54LS/74LS244

INPUTS		OUTPUT
$\overline{1G}$,$\overline{2G}$	D	
L	L	L
L	H	H
H	X	(Z)

SN54LS/74LS241

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{1G}$	D		2G	D	
L	L	L	H	L	L
L	H	H	H	H	H
H	X	(Z)	L	X	(Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−3.0	mA
		54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
$V_{T+} - V_{T-}$	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA	
		54,74	2.0			V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				27	mA	V_{CC} = MAX	
	Total, Output LOW	LS240			44			
		LS241/244			46			
	Total at HIGH Z	LS240			50			
		LS241/244			54			

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS240		9.0 12	14 18	ns	$C_L = 45$ pF, $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS241/244		12 12	18 18	ns	
t_{PZH}	Output Enable Time to HIGH Level		15	23	ns	
t_{PZL}	Output Enable Time to LOW Level		20	30	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25	ns	$C_L = 5.0$ pF $R_L = 667\ \Omega$
t_{PHZ}	Output Disable Time from HIGH Level		10	18	ns	

AC WAVEFORMS

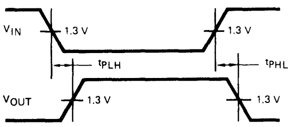

V_{IN}
1.3 V
1.3 V
t_{PLH}
t_{PHL}
V_{OUT}
1.3 V
1.3 V

Fig.1

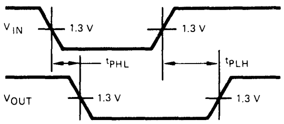

V_{IN}
1.3 V
1.3 V
t_{PHL}
t_{PLH}
V_{OUT}
1.3 V
1.3 V

Fig. 2

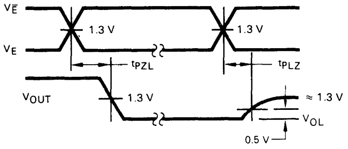

$V_{\bar{E}}$
V_E
1.3 V
1.3 V
t_{PZL}
t_{PLZ}
V_{OUT}
1.3 V
≈ 1.3 V
V_{OL}
0.5 V

Fig. 3

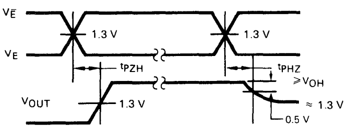
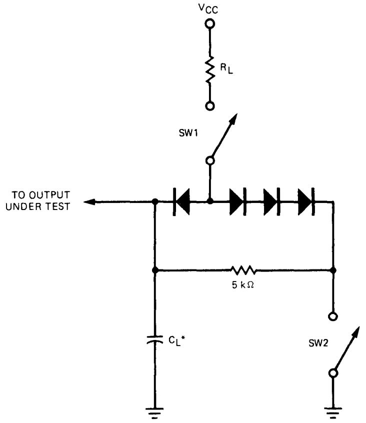

$V_{\bar{E}}$
V_E
1.3 V
1.3 V
t_{PZH}
t_{PHZ}
$\geq V_{OH}$
V_{OUT}
1.3 V
≈ 1.3 V
0.5 V

Fig. 4


V_{CC}
R_L
SW1
TO OUTPUT UNDER TEST
5 kΩ
C_L*
SW2

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

SN54/74LS242
SN54/74LS243

DESCRIPTION — The SN54LS/74LS242 and SN54LS/74LS243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

- **HYSTERISIS AT INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

QUAD BUS TRANSCEIVER

LOW POWER SCHOTTKY

TRUTH TABLES

SN54LS/74LS242

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{\text{GAB}}$	D		GAB	D	
L	L	H	L	X	(Z)
L	H	L	H	L	H
H	X	(Z)	H	H	L

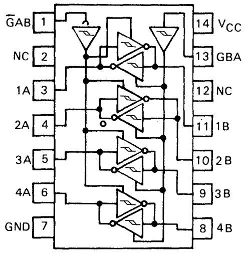
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedence

SN54LS/74LS243

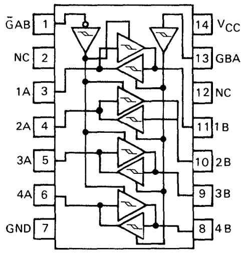
INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{\text{GAB}}$	D		GAB	D	
L	L	L	L	X	(Z)
L	H	H	H	L	L
H	X	(Z)	H	H	H

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

SN54LS/74LS242


$\overline{\text{GAB}}$ 1
NC 2
1A 3
2A 4
3A 5
4A 6
GND 7
14 VCC
13 GBA
12 NC
11 1B
10 2B
9 3B
8 4B

SN54LS/74LS243


$\overline{\text{GAB}}$ 1
NC 2
1A 3
2A 4
3A 5
4A 6
GND 7
14 VCC
13 GBA
12 NC
11 1B
10 2B
9 3B
8 4B

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−3.0	mA
		54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
$V_{T+} - V_{T-}$	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	V_{CC} = MIN I_{OH} = −3.0 mA	
		54,74	2.0			V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				40	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−200	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	D, $\overline{E}_1$, E_2			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		$\overline{E}_1$, E_2			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		D Input			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				38	mA	V_{CC} = MAX	
	Total, Output LOW				50			
	Total at HIGH Z	LS242			50			
		LS243			54			

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS242			LS243				
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		9.0 12	14 18		12 12	18 18	ns	$C_L = 45$ pF $R_L = 667\ \Omega$
t_{PZH}	Output Enable Time to HIGH Level		15	23		15	23	ns	
t_{PZL}	Output Enable Time to LOW Level		20	30		20	30	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25		15	25	ns	$C_L = 5.0$ pF $R_L = 667\ \Omega$
t_{PHZ}	Output Disable Time from HIGH Level		10	18		10	18	ns	

AC WAVEFORMS

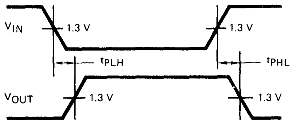

VIN
1.3 V
1.3 V
tPLH
tPHL
VOUT
1.3 V
1.3 V

Fig.1

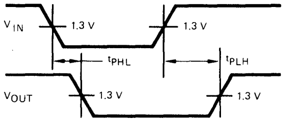

VIN
1.3 V
1.3 V
tPHL
tPLH
VOUT
1.3 V
1.3 V

Fig. 2

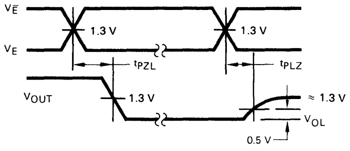

VĒ
VE
1.3 V
1.3 V
tPZL
tPLZ
VOUT
1.3 V
≈ 1.3 V
VOL
0.5 V

Fig. 3

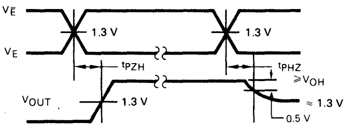
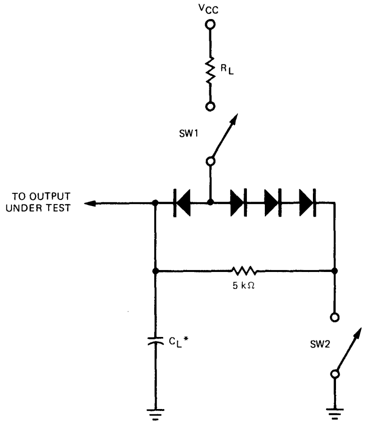

VE
VĒ
1.3 V
1.3 V
tPZH
tPHZ
≥VOH
VOUT
1.3 V
≈ 1.3 V
0.5 V

Fig. 4


VCC
RL
SW1
TO OUTPUT UNDER TEST
5 kΩ
CL*
SW2

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

MOTOROLA

SN54/74LS245

OCTAL BUS TRANSCEIVER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the buses.

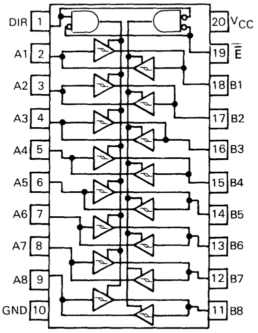
- **HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)


DIR 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 V_{CC}
19 $\overline{E}$
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−3.0	mA
		54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
$V_{T+}-V_{T-}$	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA	
		54,74	2.0			V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−200	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	A or B, DR or $\bar{E}$			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		DR or $\bar{E}$			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		A or B			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				70	mA	V_{CC} = MAX	
	Total, Output LOW				90			
	Total at HIGH Z				95			

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	C_L = 45 pF R_L = 667 Ω
t_{PZH}	Output Enable Time to HIGH Level		25	40	ns	
t_{PZL}	Output Enable Time to LOW Level		27	40	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25	ns	C_L = 5.0 pF R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level		15	25	ns	

MOTOROLA

SN54/74LS247
SN54/74LS248
SN54/74LS249

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS247 thru SN54LS/74LS249 are BCD-to-Seven-Segment Decoder/Drivers.

The LS247 and LS248 are functionally and electrically identical to the LS47 and LS48 with the same pinout configuration. The LS249 is a 16-pin version of the 14-pin LS49 and includes full functional capability for lamp test and ripple blanking which was not available in the LS49.

The composition of all characters, except the 6 and 9 are identical between the LS247, 248, 249 and the LS47, 48 and 49. The LS47 thru 49 compose the 6 and 9 without tails, the LS247 thru 249 compose the 6 and 9 with the tails. The LS247 has active-low outputs for direct drive of indicators. The LS248 and 249 have active-high outputs for driving lamp buffers.

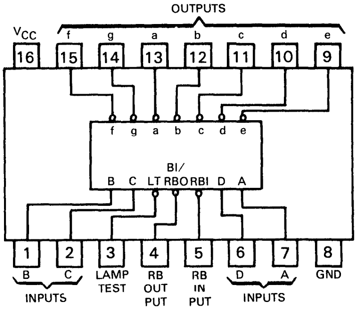
All types feature a lamp test input and have full ripple-blanking input/output controls. On all types an automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level. Segment identification and resultant displays are shown below. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

LS247
- OPEN-COLLECTOR OUTPUTS DRIVE INDICATORS DIRECTLY
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION

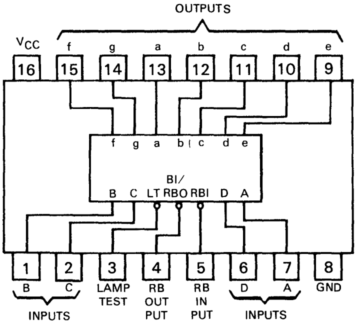
LS248
- INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION

LS249
- OPEN-COLLECTOR OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION

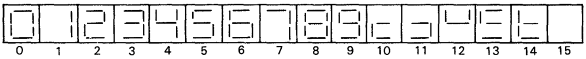
SN54LS/74LS247
(TOP VIEW)


OUTPUTS
VCC
f
g
a
b
c
d
e
16
15
14
13
12
11
10
9
f g a b c d e
BI/
B C LT RBO RBI D A
1
2
3
4
5
6
7
8
B
C
LAMP TEST
RB OUT PUT
RB IN PUT
D
A
GND
INPUTS
INPUTS

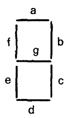
SN54LS/74LS248
SN54LS/74LS249
(TOP VIEW)


OUTPUTS
VCC
f
g
a
b
c
d
e
16
15
14
13
12
11
10
9
f g a b c d e
BI/
B C LT RBO RBI D A
1
2
3
4
5
6
7
8
B
C
LAMP TEST
RB OUT PUT
RB IN PUT
D
A
GND
INPUTS
INPUTS

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

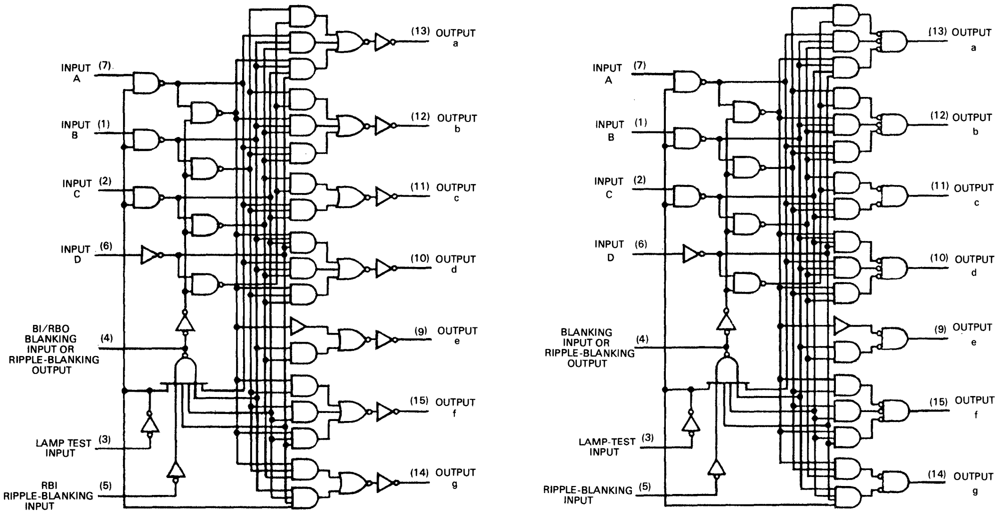


SEGMENT IDENTIFICATION

ALL CIRCUIT TYPES FEATURE LAMP INTENSITY MODULATION CAPABILITY

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	
SN54LS247	low	open-collector	12 mA	15 V	35 mW
SN54LS248	high	2-kΩ pull-up	2.0 mA	5.5 V	125 mW
SN54LS249	high	open-collector	4.0 mA	5.5 V	40 mW
SN74LS247	low	open-collector	24 mA	15 V	35 mW
SN74LS248	high	2-kΩ pull-up	6.0 mA	5.5 V	125 mW
SN74LS249	high	open-collector	8.0 mA	5.5 V	40 mW

LOGIC DIAGRAM



LS247

LS248, LS249

INPUT (7) A
INPUT (1) B
INPUT (2) C
INPUT (6) D
BI/RBO BLANKING INPUT OR RIPPLE-BLANKING OUTPUT (4)
LAMP TEST INPUT (3)
RBI RIPPLE-BLANKING INPUT (5)
(13) OUTPUT a
(12) OUTPUT b
(11) OUTPUT c
(10) OUTPUT d
(9) OUTPUT e
(15) OUTPUT f
(14) OUTPUT g
INPUT (7) A
INPUT (1) B
INPUT (2) C
INPUT (6) D
BLANKING INPUT OR RIPPLE-BLANKING OUTPUT (4)
LAMP-TEST INPUT (3)
RIPPLE-BLANKING INPUT (5)
(13) OUTPUT a
(12) OUTPUT b
(11) OUTPUT c
(10) OUTPUT d
(9) OUTPUT e
(15) OUTPUT f
(14) OUTPUT g

LS247
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

LS248, LS249
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	1
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High BI/RBO	54,74			−50	μA
I_{OL}	Output Current — Low BI/RBO	54 74			1.6 3.2	mA
$V_{O(off)}$	Off-State Output Voltage a—g	54,74			15	V
$I_{O(on)}$	On-State Output Current a—g a—g	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage BI/RBO	54	2.4	4.2		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.4	4.2		V		
V_{OL}	Output LOW Voltage BI/RBO	54,74		0.25	0.4	V	$I_{OL} = 1.6$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 3.2$ mA	
$I_{O(off)}$	Off-State Output Current a—g	54,74			250	μA	V_{CC} = MAX, $V_{IH} = 2.0$ V, $V_{O(off)} = 15$ V, V_{IL} = MAX	
$V_{O(on)}$	On-State Output Voltage a—g	54,74		0.25	0.4	V	$I_{O(on)} = 12$ mA	V_{CC} = MIN, $V_{IH} = 2.0$ V, V_{IL} per Truth Table
		74		0.35	0.5	V	$I_{O(on)} = 24$ mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
					0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current Any Input, except BI/RBO				−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
	BI/RBO				−1.2			
I_{OS}	Short Circuit Current BI/RBO		−0.3		−2.0	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			7.0	13	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $V_{CC} = 5.0$ V, $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Turn-Off Time from A Input Turn-On Time from A Input			100 100	ns	$C_L = 15$ pF, $R_L = 665\ \Omega$
t_{PHL} t_{PLH}	Turn-Off Time from RBI Input Turn-On Time from RBI Input			100 100	ns	

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High BI/RBO	54,74			−50	μA
	a–g	54,74			−100	
I_{OL}	Output Current — Low BI/RBO	54			1.6	mA
	BI/RBO	74			3.2	
	a–g	54			2.0	
	a–g	74			6.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	4.2		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
	a—g and BI/RBO	74	2.4	4.2		V	
I_O	Output Current a—g	54,74	−1.3	−2.0		mA	V_{CC} = MIN, V_O = 0.85 V, Input Conditions as for V_{OH}
V_{OL}	Output LOW Voltage a—g	54,74		0.25	0.4	V	I_{OL} = 2.0 mA V_{CC} = MIN, V_{IH} = 2.0 V, V_{IL} = per Truth Table
		74		0.35	0.5		I_{OL} = 6.0 mA
	BI/RBO	54,74		0.25	0.4	V	I_{OL} = 1.6 mA
		74		0.35	0.5		I_{OL} = 3.2 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Any Input, except BI/RBO				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current Any Input, except BI/RBO				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	BI/RBO				−1.2		
I_{OS}	Short Circuit Current BI/RBO		−0.3		−2.0	mA	V_{CC} = MAX
I_{CC}	Power Supply Current			25	38	mA	V_{CC} = MAX

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output from A Input			100	ns	C_L = 15 pF, R_L = 4.0 kΩ
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output from A Input			100		
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output from RBI Input			100	ns	C_L = 15 pF, R_L = 6.0 kΩ
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output from RBI Input			100		

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High BI/RBO	54,74			−50	µA
I_{OL}	Output Current — Low BI/RBO BI/RBO	54 74			1.6 3.2	mA
V_{OH}	Output Voltage — High a—g	54,74			5.5	V
I_{OL}	Output Current — Low a—g a—g	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54	2.4	4.2		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
	BI/RBO	74	2.4	4.2		V		
I_{OH}	Output HIGH Current a—g	54,74			250	µA	V_{CC} = MIN, $V_{IH} = 2.0$ V, $V_{OH} = 5.5$ V, V_{IL} = MAX	
V_{OL}	Output LOW Voltage BI/RBO	54,74		0.25	0.4	V	$I_{OL} = 1.6$ mA	V_{CC} = MIN, $V_{IH} = 2.0$ V, V_{IL} = per Truth Table
		74		0.35	0.5		$I_{OL} = 3.2$ mA	
	a—g	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA	
		74		0.35	0.5		$I_{OL} = 8.0$ mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
	Any Input, except BI/RBO				0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current Any Input, except BI/RBO				−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
	BI/RBO				−1.2			
I_{OS}	Short Circuit Current BI/RBO		−0.3		−2.0	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			8.0	15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $V_{CC} = 5.0$ V, $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHL} t_{PLH}	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	$C_L = 15$ pF, $R_L = 2.0$ kΩ
t_{PHL} t_{PLH}	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	$C_L = 15$ pF, $R_L = 6.0$ kΩ

MOTOROLA

SN74LS251

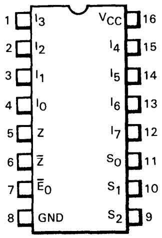
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

CONNECTION DIAGRAM
DIP (TOP VIEW)



1
I_3
V_{CC}
16
2
I_2
I_4
15
3
I_1
I_5
14
4
I_0
I_6
13
5
Z
I_7
12
6
$\overline{Z}$
S_0
11
7
$\overline{E}_0$
S_1
10
8
GND
S_2
9

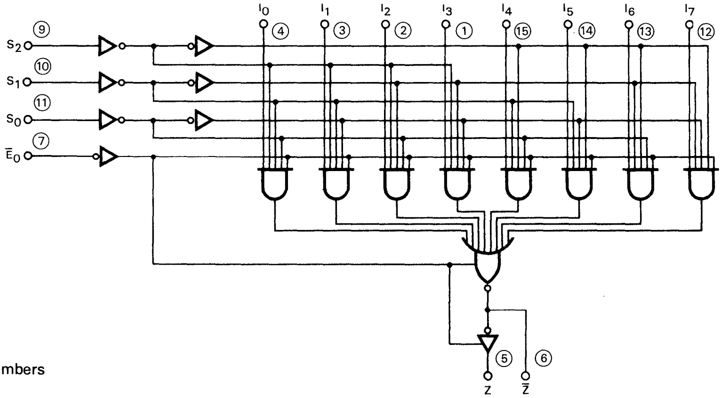
J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_0$	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output	65 U.L.	15 U.L.
$\overline{Z}$	Complementary Multiplexer Output	65 U.L.	15 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
④
③
②
①
⑮
⑭
⑬
⑫
⑨
S_2
⑩
S_1
⑪
S_0
⑦
$\overline{E}_0$
⑤
⑥
Z
$\overline{Z}$

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{E}_O$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{E}_O \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

$\overline{E}_0$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			−2.6	mA
I_{OL}	Output Current — Low			24	mA

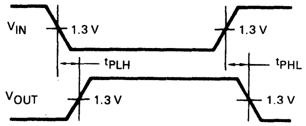
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	2.4	3.1		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH			20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW			−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current	−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			10	mA	V_{CC} = MAX, $V_{\bar{E}}$ = 0.0 V	
				12	mA	V_{CC} = MAX, $V_{\bar{E}}$ = 4.5 V	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

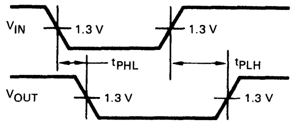
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Select to $\bar{Z}$ Output		20 21	33 33	ns	Fig. 1	C_L = 15 pF, R_L = 2K Ω
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		29 28	45 45	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\bar{Z}$ Output		10 9.0	15 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		17 18	28 28	ns	Fig. 2	
t_{PZH} t_{PZL}	Output Enable Time to $\bar{Z}$ Output		17 24	27 40	ns	Figs. 4, 5	
t_{PZH} t_{PZL}	Output Enable Time to Z Output		30 26	45 40	ns	Figs. 3, 5	
t_{PHZ} t_{PLZ}	Output Disable Time to $\bar{Z}$ Output		37 15	55 25	ns	Figs. 3, 5	C_L = 5 pF R_L = 667 Ω
t_{PHZ} t_{PLZ}	Output Disable Time to Z Output		30 15	45 25	ns	Figs. 4, 5	

3-STATE AC WAVEFORMS



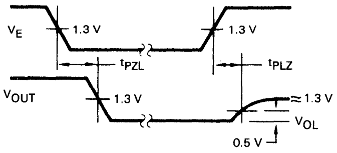
VIN
1.3 V
1.3 V
tPLH
tPHL
VOUT
1.3 V
1.3 V

Fig. 1



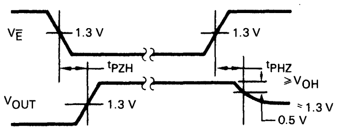
VIN
1.3 V
1.3 V
tPHL
tPLH
VOUT
1.3 V
1.3 V

Fig. 2



VE
1.3 V
1.3 V
tPZL
tPLZ
VOUT
1.3 V
≈1.3 V
VOL
0.5 V

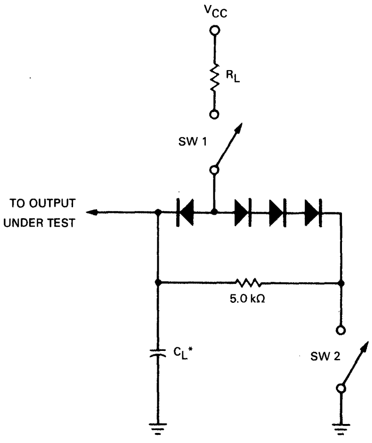
Fig. 3



VE
1.3 V
1.3 V
tPZH
tPHZ
≥VOH
VOUT
1.3 V
≈1.3 V
0.5 V

Fig. 4

AC LOAD CIRCUIT



VCC
RL
SW 1
TO OUTPUT UNDER TEST
5.0 kΩ
CL*
SW 2

*Includes Jig and Probe Capacitance.

Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

MOTOROLA

SN54/74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{E}_O$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

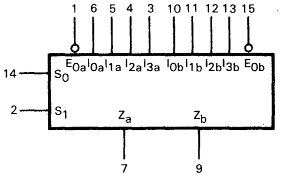
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_{0a} — I_{3a}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output (Note b)	65(25) U.L.	15(7.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_{0b} — I_{3b}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Mutiplexer Output (Note b)	65(25) U.L.	15(7.5) U.L.

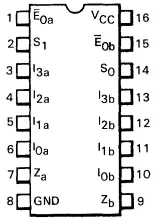
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


1 6 5 4 3 10 11 12 13 15
14
2
S_0
$\overline{E}_{0a}$ I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b} $\overline{E}_{0b}$
S_1
Z_a
Z_b
7
9

V_{CC} = Pin 16
GND = Pin 8

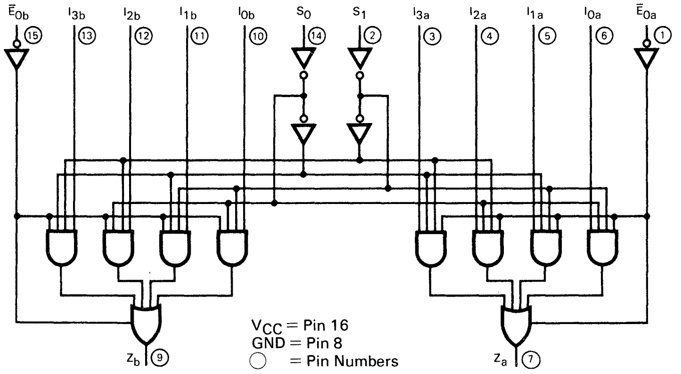
CONNECTION DIAGRAM
DIP (TOP VIEW)


1 $\overline{E}_{0a}$
2 S_1
3 I_{3a}
4 I_{2a}
5 I_{1a}
6 I_{0a}
7 Z_a
8 GND
16 V_{CC}
15 $\overline{E}_{0b}$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Z_b

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


$\overline{E}_{0b}$ ⑮
I_{3b} ⑬
I_{2b} ⑫
I_{1b} ⑪
I_{0b} ⑩
S_0 ⑭
S_1 ②
I_{3a} ③
I_{2a} ④
I_{1a} ⑤
I_{0a} ⑥
$\overline{E}_{0a}$ ①
Z_b ⑨
Z_a ⑦

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Irrelevant
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				12	mA	V_{CC} = MAX, $V_{\overline{E}}$ = 0.0 V	
					14	mA	V_{CC} = MAX, $V_{\overline{E}}$ = 4.5 V	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See SN54LS251 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		17 13	25 20	ns	Fig. 1	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		30 21	45 32	ns	Fig. 1	
t_{PZH} t_{PZL}	Output Enable Time		15 15	28 23	ns	Figs. 4, 5	
t_{PHZ} t_{PLZ}	Output Disable Time		27 18	41 27	ns	Figs. 3, 5	C_L = 5.0 pF R_L = 667 Ω

MOTOROLA

SN54/74LS256

DUAL 4-BIT ADDRESSABLE LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input (E) and an active LOW Clear input (CL). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{CL}$) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the ($\overline{CL}$) and $\overline{E}$ are both LOW. When $\overline{CL}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q_0-Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$=LOW, $\overline{CL}$=HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$=$\overline{CL}$=HIGH).

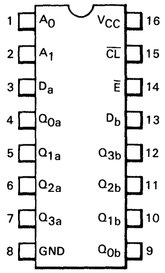
- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **EASILY EXPANDABLE**
- **ACTIVE LOW COMMON CLEAR**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
D_a, D_b	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable Input (Active LOW)	1.0 U.L.	0.5 U.L.
$\overline{CL}$	Clear Input (Active LOW)	0.5 U.L.	0.25 U.L.
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

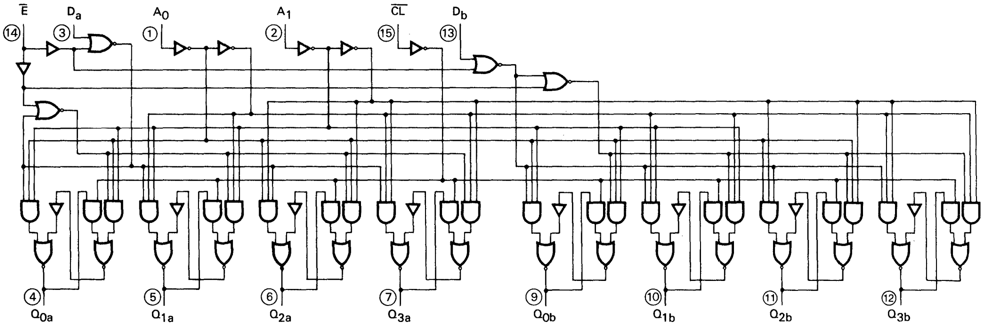
CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

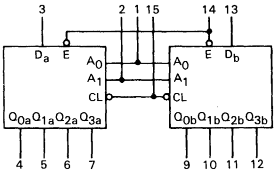
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL


3
2
1
15
14
13
D_a
E
A_0
A_1
CL
Q_{0a} Q_{1a} Q_{2a} Q_{3a}
A_0
A_1
CL
E
D_b
Q_{0b} Q_{1b} Q_{2b} Q_{3b}
4
5
6
7
9
10
11
12

V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE

$\overline{CL}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
H	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable Latch
H	L	H	L	L	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	
H	L	L	H	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
H	L	H	H	L	Q_{N-1}	H	Q_{N-1}	Q_{N-1}	
H	L	L	L	H	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
H	L	H	L	H	Q_{N-1}	Q_{N-1}	H	Q_{N-1}	
H	L	L	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
H	L	H	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	H	

H = High Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECTION

$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Others $\overline{E}$ Input				 20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Others $\overline{E}$ Input				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Others $\overline{E}$ Input				 −0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				25	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

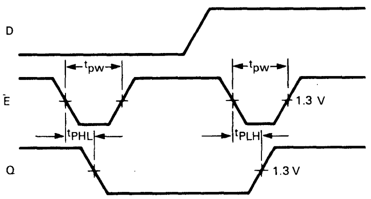
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		20 16	27 24	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 1
t_{PLH} t_{PHL}	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	30 20	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 2
t_{PLH} t_{PHL}	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		20 14	30 24	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 3
t_{PHL}	Turn-On Delay, Clear to Output		12	23	ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_s	Data Setup Time	20			ns	$V_{CC} = 5.0$ V Fig. 4
t_s	Address Setup Time	0			ns	Fig. 6
t_h	Data Hold Time	0			ns	$V_{CC} = 5.0$ V Fig. 4
t_h	Address Hold Time	15			ns	$V_{CC} = 5$V Fig. 6
t_W	Enable Pulse Width	15			ns	$V_{CC} = 5.0$ V Fig. 1

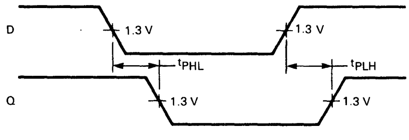
AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH


D
$\overline{E}$
t_{pw}
t_{pw}
1.3 V
t_{PHL}
t_{PLH}
Q
1.3 V

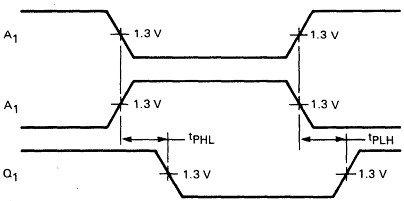
OTHER CONDITIONS: $\overline{CL}$ = H, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT


D
1.3 V
1.3 V
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V

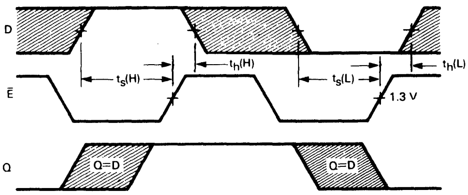
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{CL}$ = H, A = STABLE

Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT


A_1
1.3 V
1.3 V
A_1
1.3 V
1.3 V
t_{PHL}
t_{PLH}
Q_1
1.3 V
1.3 V

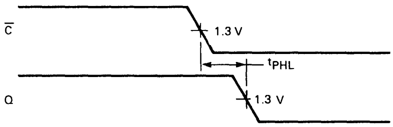
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{CL}$ = L, D = H

Fig. 4 SETUP AND HOLD TIME, DATA TO ENABLE


D
$t_h(H)$
$t_h(L)$
$t_s(H)$
$t_s(L)$
$\overline{E}$
1.3 V
Q
Q=D
Q=D

OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

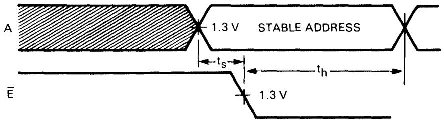
Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT


$\overline{C}$
1.3 V
t_{PHL}
Q
1.3 V

OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SETUP TIME, ADDRESS TO ENABLE

(SEE NOTES 1 AND 2)


A
1.3 V
STABLE ADDRESS
t_s
t_h
$\overline{E}$
1.3 V

OTHER CONDITIONS: $\overline{CL}$ = H

NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

MOTOROLA

SN54/74LS257A
SN54/74LS258A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

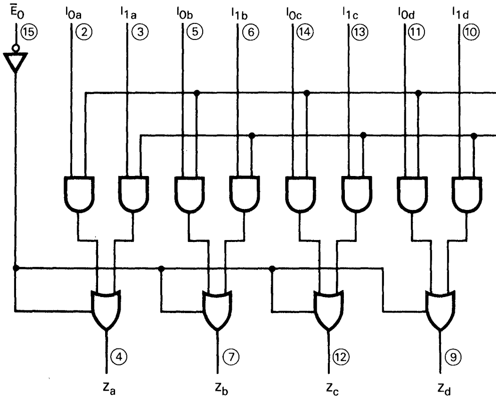
LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS257A and the SN54LS/74LS258A are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (E_O) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

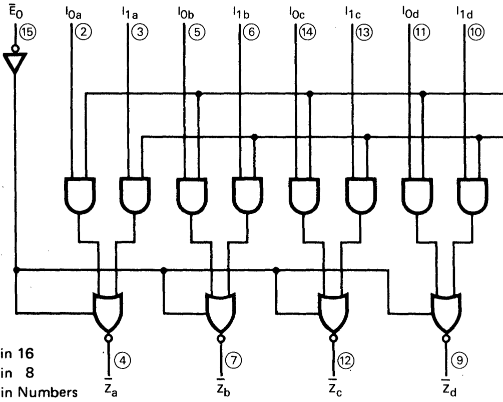
LOGIC DIAGRAMS

SN54LS/74LS257A



Ē0 ⑮
I0a ②
I1a ③
I0b ⑤
I1b ⑥
I0c ⑭
I1c ⑬
I0d ⑪
I1d ⑩
S ①
④ Za
⑦ Zb
⑫ Zc
⑨ Zd

SN54LS/74LS258A

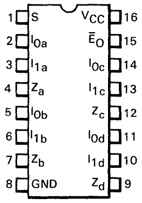


Ē0 ⑮
I0a ②
I1a ③
I0b ⑤
I1b ⑥
I0c ⑭
I1c ⑬
I0d ⑪
I1d ⑩
S ①
④ Z̄a
⑦ Z̄b
⑫ Z̄c
⑨ Z̄d

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)

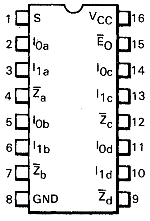
SN54LS/74LS257A



1 S
2 I0a
3 I1a
4 Za
5 I0b
6 I1b
7 Zb
8 GND
16 VCC
15 Ē0
14 I0c
13 I1c
12 Zc
11 I0d
10 I1d
9 Zd

V_{CC} = Pin 16
GND = Pin 8

SN54LS/74LS258A



1 S
2 I0a
3 I1a
4 Z̄a
5 I0b
6 I1b
7 Z̄b
8 GND
16 VCC
15 Ē0
14 I0c
13 I1c
12 Z̄c
11 I0d
10 I1d
9 Z̄d

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS257A and LS258A are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257A and in the inverted form for the LS258A.

The LS257A and LS258A are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

LS257A

$Z_a = \overline{E}_O \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$ $\quad Z_b = \overline{E}_O \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

$Z_c = \overline{E}_O \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$ $\quad Z_d = \overline{E}_O \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

LS258A

$\overline{Z}_a = \overline{E}_O \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$ $\quad \overline{Z}_b = \overline{E}_O \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

$\overline{Z}_c = \overline{E}_O \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$ $\quad \overline{Z}_d = \overline{E}_O \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257A	OUTPUTS LS258A
$\overline{E}_O$	S	I_0	I_1	Z	$\overline{Z}$
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current — HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current — LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	Other Inputs			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		S Inputs			40	µA		
		Other Inputs			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		S Inputs			0.2	mA		
I_{IL}	Input LOW Current	Other Inputs			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		S Inputs			−0.8	mA		
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current						V_{CC} = MAX	
	Total, Output HIGH	LS257A			10	mA		
		LS258A			7.0	mA		
	Total, Output LOW	LS257A			16	mA		
		LS258A			14	mA		
	Total, Output 3-State				19	mA		

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See SN54LS251 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH}	Propagation Delay, Data to Output		12	18	ns	Fig. 1, 2	C_L = 45 pF
t_{PHL}			12	18			
t_{PLH}	Propagation Delay, Select to Output		14	21	ns	Fig. 1, 2	C_L = 45 pF
t_{PHL}			14	21			
t_{PZH}	Output Enable Time to HIGH Level		20	30	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level		20	30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time to LOW Level		16	25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level		18	30	ns	Figs. 4, 5	R_L = 667 Ω

MOTOROLA

SN54/74LS259

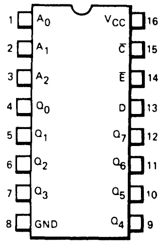
8-BIT ADDRESSABLE LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- **SERIAL-TO-PARALLEL CONVERSION**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABIILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**

CONNECTION DIAGRAM
DIP (TOP VIEW)



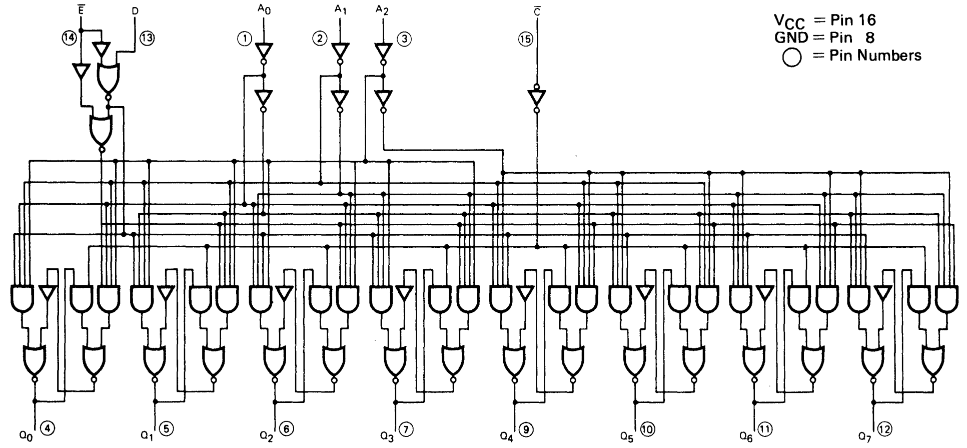
1 A0
2 A1
3 A2
4 Q0
5 Q1
6 Q2
7 Q3
8 GND
16 VCC
15 C̄
14 Ē
13 D
12 Q7
11 Q6
10 Q5
9 Q4

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
A_0, A_1, A_2	Address Inputs	0.5 U.L.	0.25 U.L.
D	Data Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



Ē
D
A0
A1
A2
C̄
⑭
⑬
①
②
③
⑮
VCC = Pin 16
GND = Pin 8
○ = Pin Numbers
Q0 ④
Q1 ⑤
Q2 ⑥
Q3 ⑦
Q4 ⑨
Q5 ⑩
Q6 ⑪
Q7 ⑫

FUNCTIONAL DESCRIPTION — The SN54LS/74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN54LS/74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

TRUTH TABLE

PRESENT OUTPUT STATES

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}	→							Memory
H	I	I	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	→				Addressable Latch
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}	→					
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}	→					
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}	→					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
H	L	L	H	H	H	Q_{N-1}	→					Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}	→					Q_{N-1}	H	

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				36	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

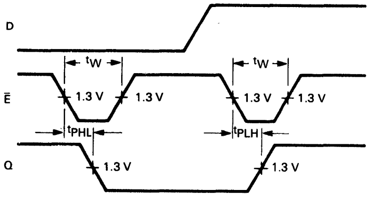
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn-Off Delay, Enable to Output		22	35	ns	C_L = 15 pF
t_{PHL}	Turn-On Delay, Enable to Output		15	24	ns	
t_{PLH}	Turn-Off Delay, Data to Output		20	32	ns	
t_{PHL}	Turn-On Delay, Data to Output		13	21	ns	
t_{PLH}	Turn-Off Delay, Address to Output		24	38	ns	
t_{PHL}	Turn-On Delay, Address to Output		18	29	ns	
t_{PHL}	Turn-On Delay, Clear to Output		17	27	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C, V_{CC} = 5.0\text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
t_s	Input Setup Time	20			ns
t_W	Pulse Width, Clear or Enable	15			ns
t_h	Hold Time, Data	5.0			ns
t_h	Hold Time, Address	20			ns

AC WAVEFORMS

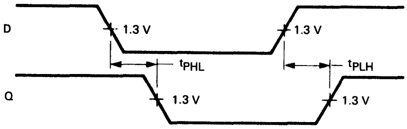
Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



D
$\overline{E}$
Q
t_W
t_W
1.3 V
1.3 V
1.3 V
1.3 V
t_{PHL}
t_{PLH}
1.3 V
1.3 V

OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

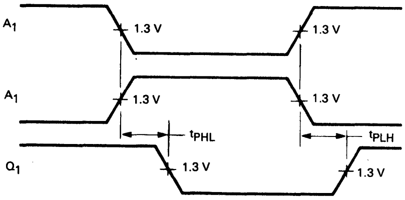
Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



D
1.3 V
1.3 V
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V

OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

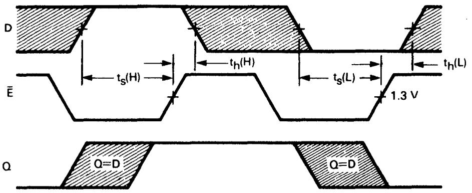
Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



A_1
1.3 V
1.3 V
A_1
1.3 V
1.3 V
t_{PHL}
t_{PLH}
Q_1
1.3 V
1.3 V

OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

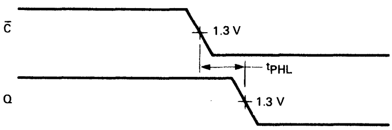
Fig. 4 SETUP AND HOLD TIME, DATA TO ENABLE



D
$t_h(H)$
$t_h(L)$
$t_s(H)$
$t_s(L)$
$\overline{E}$
1.3 V
Q
Q=D
Q=D

OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

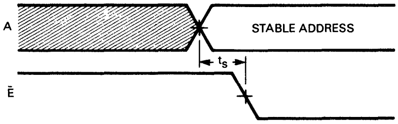
Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT



$\overline{C}$
1.3 V
t_{PHL}
Q
1.3 V

OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SETUP TIME, ADDRESS TO ENABLE (SEE NOTES 1 AND 2)



A
STABLE ADDRESS
t_s
$\overline{E}$

OTHER CONDITIONS: $\overline{C}$ = H

NOTES:

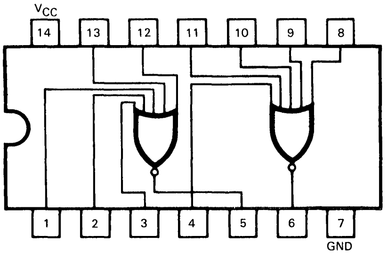
1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

MOTOROLA

SN54/74LS260

DUAL 5-INPUT NOR GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				4.0	mA	V_{CC} = MAX	
	Total, Output LOW				5.5			

AC CHARACTERISTICS: $T_A = 25°C$

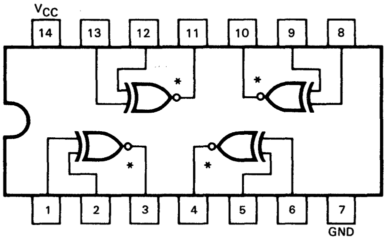
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		5.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		6.0	15	ns	C_L = 15 pF

MOTOROLA

SN54/74LS266

QUAD 2-INPUT EXCLUSIVE NOR GATE

LOW POWER SCHOTTKY



*OPEN COLLECTOR OUTPUTS

TRUTH TABLE

IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
V_{OH}	Output Voltage — High	54,74			5.5	V
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current	54,74			100	µA	V_{CC} = MIN, V_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current				13	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		18 18	30 30	ns	V_{CC} = 5.0 V C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		18 18	30 30	ns	

MOTOROLA

SN54/74LS273

OCTAL D FLIP-FLOP WITH CLEAR

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- **8-BIT HIGH SPEED REGISTER**
- **PARALLEL REGISTER**
- **COMMON CLOCK AND MASTER RESET**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_7	Register Outputs (Note b)	10 U.L.	5(2.5) U.L.

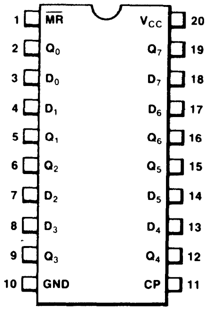
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

$\overline{MR}$	CP	D_x	Q_x
L	X	X	L
H	↑	H	H
H	↑	L	L

H = High Logic Level
L = Low Logic Level
X = Immaterial

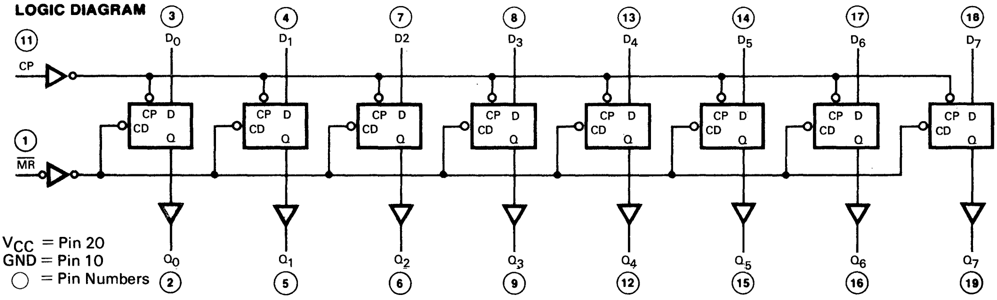
CONNECTION DIAGRAM
DIP (TOP VIEW)



1 $\overline{MR}$
2 Q_0
3 D_0
4 D_1
5 Q_1
6 Q_2
7 D_2
8 D_3
9 Q_3
10 GND
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

LOGIC DIAGRAM



③ D_0
④ D_1
⑦ D2
⑧ D_3
⑬ D_4
⑭ D_5
⑰ D_6
⑱ D_7
⑪ CP
① $\overline{MR}$
CP D
CD Q
Q_0 ②
Q_1 ⑤
Q_2 ⑥
Q_3 ⑨
Q_4 ⑫
Q_5 ⑮
Q_6 ⑯
Q_7 ⑲

V_{CC} = Pin 20
GND = Pin 10
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The SN54LS/74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX

AC CHARACTERISTICS: $T_A = 25°C, V_{CC} = 5.0$ V

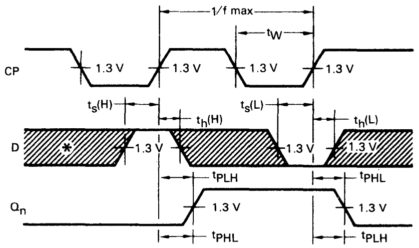
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Input Clock Frequency	30	40		MHz	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output		18	27	ns	Fig. 2
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 18	27 27	ns	Fig. 1

AC SETUP REQUIREMENTS: $T_A = 25°C, V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Pulse Width, Clock or Clear	20			ns	Fig. 1
t_s	Data Setup Time	20			ns	Fig. 1
t_h	Hold Time	5.0			ns	Fig. 1
t_{rec}	Recovery Time	25			ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

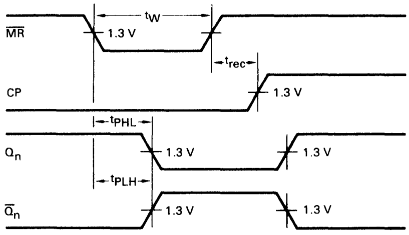


Fig. 2

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

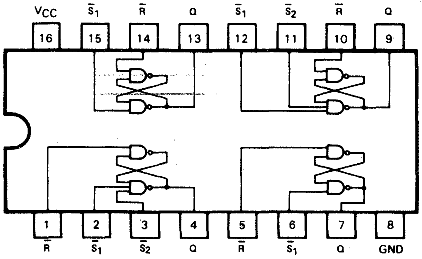
RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

MOTOROLA

SN54/74LS279

QUAD SET-RESET LATCH

LOW POWER SCHOTTKY



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

TRUTH TABLE

INPUTS			OUTPUT
$\overline{S}_1$	$\overline{S}_2$	$\overline{R}$	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				7.0	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{S}$ to Output		12 13	22 21	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{R}$ to Output		15	27	ns	

MOTOROLA

SN54/74LS280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

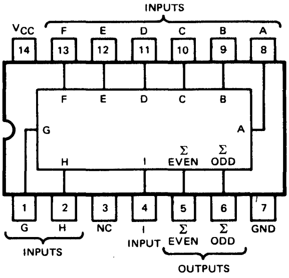
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS280 is a Universal 9-Bit Parity Generator/Checker. It features odd/even outputs to facilitate either odd or even parity. By cascading, the word length is easily expanded.

The LS280 is designed without the expander input implementation, but the corresponding function is provided by an input at Pin 4 and the absence of any connection at Pin 3. This design permits the LS280 to be substituted for the LS180 which results in improved performance. The LS280 has buffered inputs to lower the drive requirements to one LS unit load.

- **GENERATES EITHER ODD OF EVEN PARITY FOR NINE DATA LINES**
- **TYPICAL DATA-TO-OUTPUT DELAY OF ONLY 33 ns**
- **CASCADABLE FOR n-BITS**
- **CAN BE USED TO UPGRADE SYSTEMS USING MSI PARITY CIRCUITS**
- **TYPICAL POWER DISSIPATION = 80 mW**

(TOP VIEW)


INPUTS
VCC
F
E
D
C
B
A
14
13
12
11
10
9
8
F
E
D
C
B
G
A
H
I
Σ EVEN
Σ ODD
1
2
3
4
5
6
7
G
H
NC
I
Σ
Σ
GND
INPUT
EVEN
ODD
INPUTS
OUTPUTS

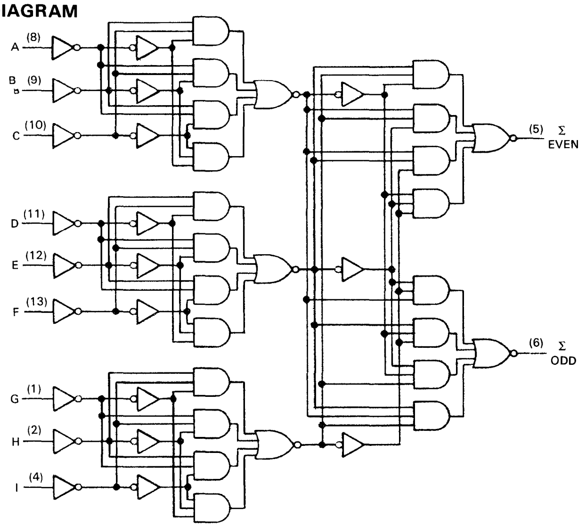
J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

FUNCTON TABLE

NUMBER OF INPUTS A THRU 1 THAT ARE HIGH	OUTPUTS	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

FUNCTIONAL BLOCK DIAGRAM


A (8)
B (9)
C (10)
D (11)
E (12)
F (13)
G (1)
H (2)
I (4)
(5) Σ EVEN
(6) Σ ODD

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output Σ EVEN		33 29	50 45	ns	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output Σ ODD		23 31	35 50	ns	

MOTOROLA

SN54/74LS283

4-BIT BINARY FULL ADDER WITH FAST CARRY

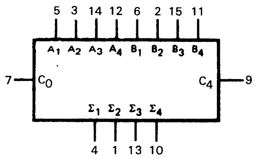
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 — A_4, B_1 — B_4) and a Carry Input (C_0). It generates the binary Sum outputs (Σ_1 — Σ_4) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
A_1 — A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1 — B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
Σ_1 — Σ_4	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

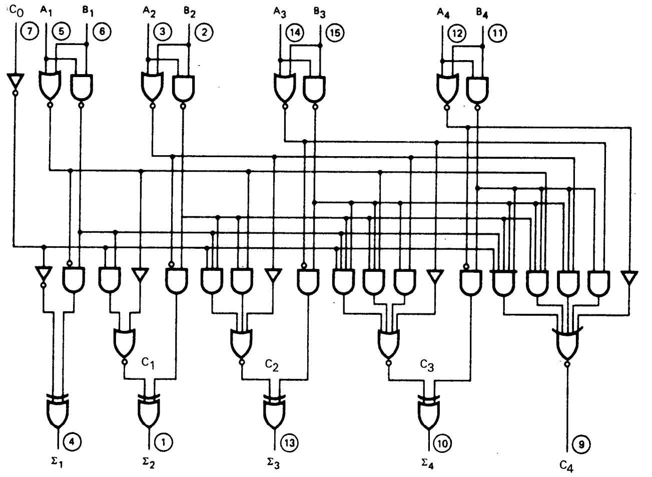
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


5 3 14 12 6 2 15 11
A1 A2 A3 A4 B1 B2 B3 B4
7
C0
C4
9
Σ1 Σ2 Σ3 Σ4
4 1 13 10

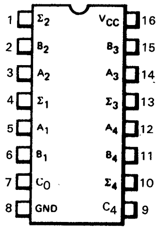
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM


C0 A1 B1 A2 B2 A3 B3 A4 B4
7 5 6 3 2 14 15 12 11
C1 C2 C3
4 1 13 10 9
Σ1 Σ2 Σ3 Σ4 C4

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 Σ2
2 B2
3 A2
4 Σ1
5 A1
6 B1
7 C0
8 GND
16 VCC
15 B3
14 A3
13 Σ3
12 A4
11 B4
10 Σ4
9 C4

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTES:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 — Σ_4) and outgoing carry (C_4) outputs.

$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\ \Sigma_2+4\ \Sigma_3+8\ \Sigma_4+16C_4$
Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 7, 5 or 3.

FUNCTIONAL TRUTH TABLE

C (n−1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 is an external input
C_4 is an output generated internally

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	C_0			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
		Any A or B			40	µA	
		C_0			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
		Any A or B			0.2	mA	
I_{IL}	Input LOW Current	C_0			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
		Any A or B			−0.8	mA	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				34	mA	V_{CC} = MAX
	Total, Output LOW				39		

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to Any Σ Output		16 15	24 24	ns	C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 11	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

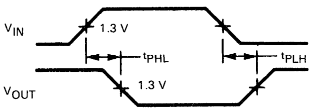


Fig. 1

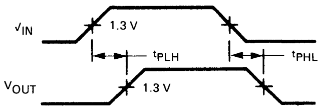


Fig. 2

MOTOROLA

SN54/74LS290
SN54/74LS293

DECADE COUNTER; 4-BIT BINARY COUNTER

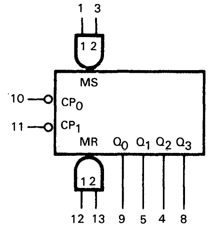
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS290 and SN54LS/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- **CORNER POWER PIN VERSIONS OF THE LS90 and LS93**
- **LOW POWER CONSUMPTION . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . TYPICALLY 42 MHz**
- **CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

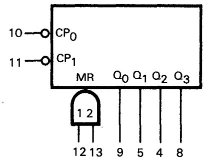
LOGIC SYMBOL

LS290



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

LS293



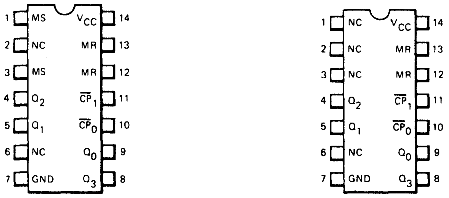
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

PIN NAMES

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section.	0.05 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS290).	0.05 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS293).	0.05 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS290) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ Input of the device.

CONNECTION DIAGRAM
DIP (TOP VIEW)



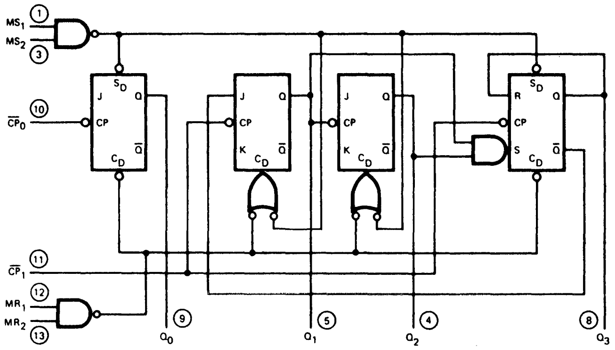
LS290 LS293

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

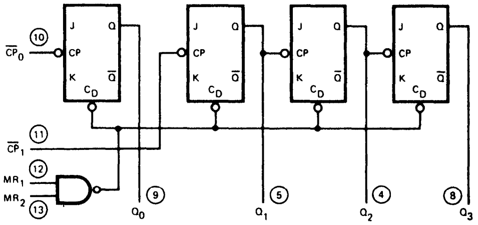
LOGIC DIAGRAMS

LS290



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

LS293



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

FUNCTIONAL DESCRIPTION – The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter – the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS293

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

5

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 , 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = – 18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS290) $\overline{CP}_1$ (LS293)				 – 0.4 – 2.4 – 3.2 – 1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0\ V$, $C_L = 15\ pF$

SYMBOL	PARAMETER	LIMITS						UNITS
		LS290			LS293			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	$\overline{CP}_0$ Input Clock Frequency	32			32			MHz
f_{MAX}	$\overline{CP}_1$ Input Clock Frequency	16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		21 23	32 35		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		21 23	32 35		34 34	51 51	ns
t_{PHL}	MS Input to Q_0 and Q_3 Outputs		20	30				ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40				ns
t_{PHL}	MR Input to Any Output		26	40		26	40	ns

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS				UNITS
		LS290		LS293		
		MIN	MAX	MIN	MAX	
t_W	$\overline{CP}_0$ Pulse Width	15		15		ns
t_W	$\overline{CP}_1$ Pulse Width	30		30		ns
t_W	MS Pulse Width	15				ns
t_W	MR Pulse Width	15		15		ns
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVE FORMS

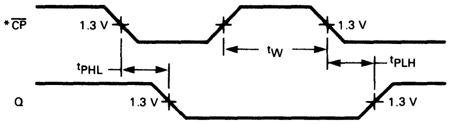


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

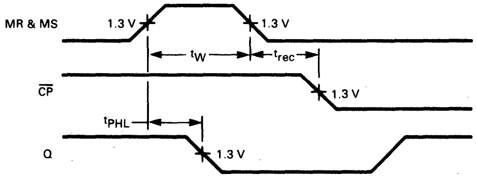


Fig. 2

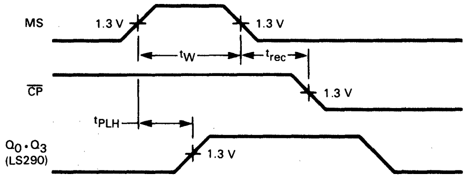


Fig. 3

MOTOROLA

SN54/74LS298

QUAD 2-INPUT MULTIPLEXER WITH STORAGE

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

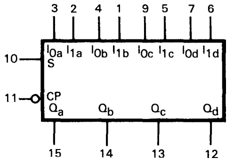
The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

- SELECT FROM TWO DATA SOURCES
- FULLY EDGE-TRIGGERED OPERATION
- TYPICAL POWER DISSIPATION OF 65 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
I_{0a}—I_{0d}	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
I_{1a}—I_{1d}	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
Q_a—Q_d	Register Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

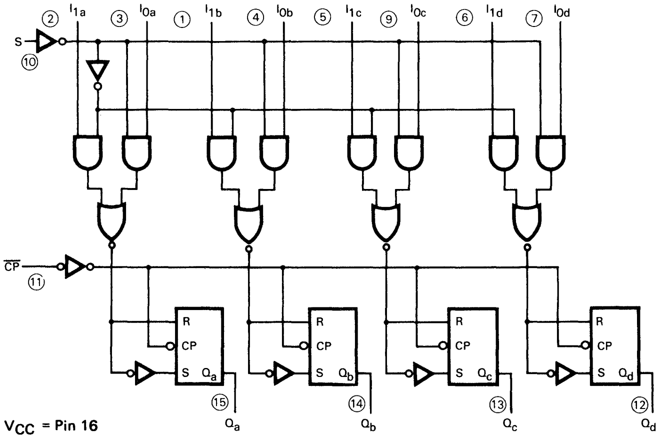
LOGIC SYMBOL



3 2 4 1 9 5 7 6
I0a I1a I0b I1b I0c I1c I0d I1d
10 S
11 CP
Qa Qb Qc Qd
15 14 13 12

V_{CC} = Pin 16
GND = Pin 8

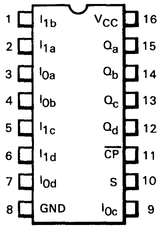
LOGIC OR BLOCK DIAGRAM



② I1a
③ I0a
① I1b
④ I0b
⑤ I1c
⑨ I0c
⑥ I1d
⑦ I0d
S ⑩
CP ⑪
R
CP
S Qa
S Qb
S Qc
S Qd
⑮ Qa
⑭ Qb
⑬ Qc
⑫ Qd

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 I1b
2 I1a
3 I0a
4 I0b
5 I1c
6 I1d
7 I0d
8 GND
16 VCC
15 Qa
14 Qb
13 Qc
12 Qd
11 CP
10 S
9 I0c

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

5

FUNCTIONAL DESCRIPTION — The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				21	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		18	27	ns	$V_{CC} = 5.0\ V$
t_{PHL}	Clock to Output		21	32	ns	$C_L = 15\ pF$

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

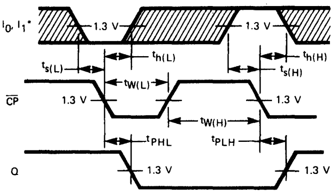
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	20			ns	$V_{CC} = 5.0\ V$
t_s	Data Setup Time	15			ns	
t_s	Select Setup Time	25			ns	
t_h	Data Hold Time	5.0			ns	
t_h	Select Hold Time	0				

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

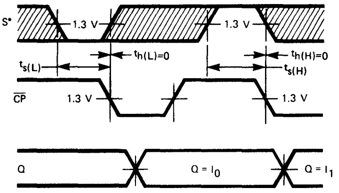


Fig. 2

MOTOROLA

SN54/74LS299

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, LOAD AND STORE**
- **SEPARATE SHIFT RIGHT SERIAL INPUT AND SHIFT LEFT SERIAL INPUT FOR EASY CASCADING**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS_0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS_7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	0.5 U.L.	0.25 U.L.
	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{MR}$	Asynchronous Master Reset (active LOW) Input	0.5 U.L.	0.25 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	0.5 U.L.

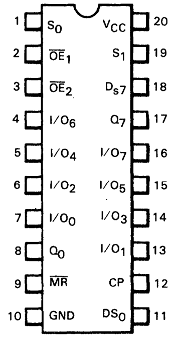
NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

c. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74), The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

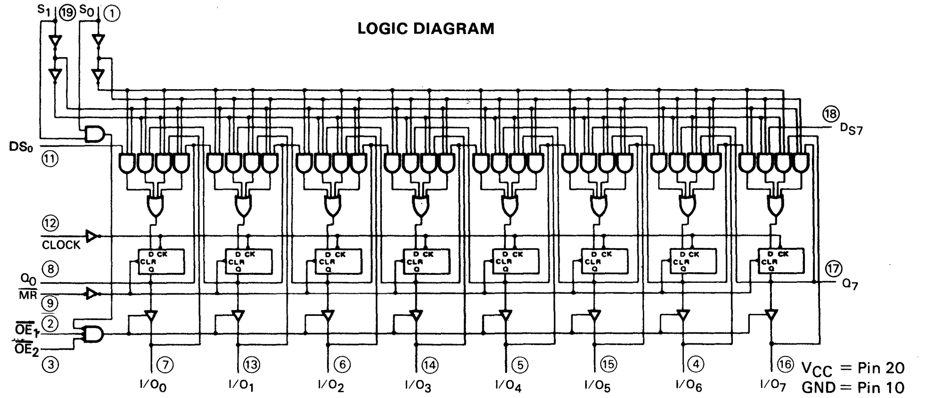
CONNECTION DIAGRAM
DIP (TOP VIEW)


1 S_0
2 $\overline{OE}_1$
3 $\overline{OE}_2$
4 I/O_6
5 I/O_4
6 I/O_2
7 I/O_0
8 Q_0
9 $\overline{MR}$
10 GND
20 V_{CC}
19 S_1
18 D_{S7}
17 Q_7
16 I/O_7
15 I/O_5
14 I/O_3
13 I/O_1
12 CP
11 DS_0

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


S_1 ⑲
S_0 ①
DS_0 ⑪
⑱ DS_7
⑫ CLOCK
D CK
CLR
Q
⑧ Q_0
$\overline{MR}$ ⑨
$\overline{OE}_1$ ②
$\overline{OE}_2$ ③
⑰ Q_7
⑦ I/O_0
⑬ I/O_1
⑥ I/O_2
⑭ I/O_3
⑤ I/O_4
⑮ I/O_5
④ I/O_6
⑯ I/O_7

V_{CC} = Pin 20
GND = Pin 10
○ = Pin Numbers

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		54	4.5	5.0	5.5	V
			74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range		54	−55	25	125	°C
			74	0	25	70	
I_{OH}	Output Current — High	Q_0, Q_7	54,74			−0.4	mA
I_{OL}	Output Current — Low	Q_0, Q_7	54			4.0	mA
		Q_0, Q_7	74			8.0	
I_{OH}	Output Current — High	I/O_0—I/O_7	54			−1.0	mA
		I/O_0—I/O_7	74			−2.6	
I_{OL}	Output Current — Low	I/O_0—I/O_7	54			12	mA
		I/O_0—I/O_7	74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage I/O_0—I/O_7	54	2.4	3.2		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.4	3.1		V		
V_{OH}	Output HIGH Voltage Q_0, Q_7	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.7	3.4		V		
V_{OL}	Output LOW Voltage I/O_0—I/O_7	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
V_{OL}	Output LOW Voltage Q_0—Q_7	54,74			0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74			0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH I/O_0—I/O_7				40	µA	V_{CC}= MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW I/O_0—I/O_7				−400	µA	V_{CC}= MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	Others			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		S_0, S_1, I/O_0—I/O_7			40	µA		
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		S_0, S_1			0.2	mA		
		I/O_0—I/O_7			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	Others			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		S_0, S_1			−0.8	mA		
I_{OS}	Short Circuit Current	Q_0, Q_7	−20		−100	mA	V_{CC} = MAX	
		I/O_0—I/O_7	−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				53	mA	V_{CC} = MAX	

FUNCTION TABLE

INPUTS								RESPONSE
$\overline{MR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L	X	X	H	X	X	X	X	Asynchronous Reset; $Q_0 = Q_7 =$ LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; $Q_0 = Q_7 =$ LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
H	L	H	X	X	↑	D	X	Shift Right; $D \rightarrow Q_0$; $Q_0 \rightarrow Q_1$; etc.
H	L	H	L	L	↑	D	X	Shift Right; $D \rightarrow Q_0$ & I/O_0; $Q_0 \rightarrow Q_1$ & I/O_1; etc.
H	H	L	X	X	↑	X	D	Shift Left; $D \rightarrow Q_7$; $Q_7 \rightarrow Q_6$; etc.
H	H	L	L	L	↑	X	D	Shift Left; $D \rightarrow Q_7$ & I/O_7; $Q_7 \rightarrow Q_6$ & I/O_6; etc.
H	H	H	X	X	↑	X	X	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	$C_L = 15$ pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_0 or Q_7		26 22	39 33	ns	
t_{PHL}	Propagation Delay, Clear to Q_0 or Q_7		27	40	ns	
t_{PHL} t_{PLH}	Propagation Delay, Clock to $I/O_0 - I/O_7$		26 17	39 25	ns	$C_L = 45$ pF, $R_L = 667\ \Omega$
t_{PHL}	Propagation Delay, Clear to $I/O_0 - I/O_7$		26	40	ns	
t_{PZH} t_{PZL}	Output Enable Time		13 19	21 30	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		10 10	15 15	ns	$C_L = 5.0$ pF

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width HIGH	25			ns	$V_{CC} = 5.0$ V
t_W	Clock Pulse Width LOW	15			ns	
t_W	Clear Pulse Width LOW	20			ns	
t_s	Data Setup Time	20			ns	
t_s	Select Setup Time	35			ns	
t_h	Data Hold Time	0			ns	
t_h	Select Hold Time	10			ns	
t_{rec}	Recovery Time	20			ns	

3- STATE WAVEFORMS

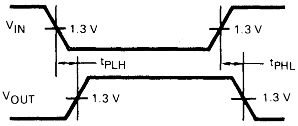

VIN
1.3 V
1.3 V
tPLH
tPHL
VOUT
1.3 V
1.3 V

Fig. 1

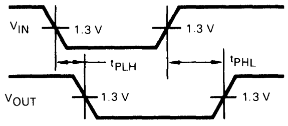

VIN
1.3 V
1.3 V
tPLH
tPHL
VOUT
1.3 V
1.3 V

Fig. 2

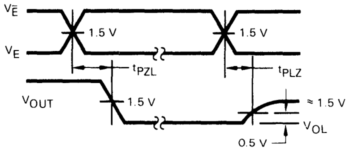

VĒ
VE
1.5 V
1.5 V
tPZL
tPLZ
VOUT
1.5 V
≈ 1.5 V
VOL
0.5 V

Fig. 3

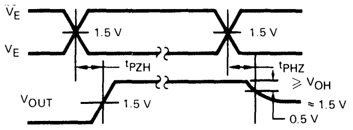
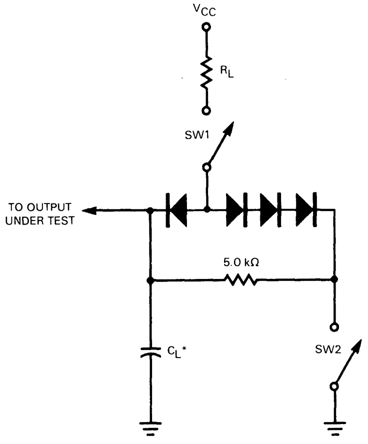

VĒ
VE
1.5 V
1.5 V
tPZH
tPHZ
≥ VOH
VOUT
1.5 V
≈ 1.5 V
0.5 V

Fig. 4

AC LOAD CIRCUIT


VCC
RL
SW1
TO OUTPUT UNDER TEST
5.0 kΩ
CL*
SW2

*Includes Jig and Probe Capacitance.

Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

MOTOROLA

SN54/74LS322A

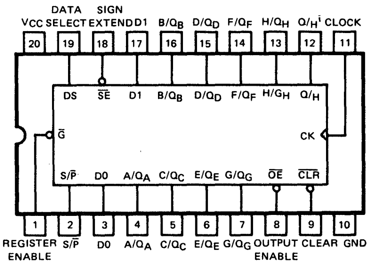
8-BIT SHIFT REGISTERS WITH SIGN EXTEND

LOW POWER SCHOTTKY

DESCRIPTION — These 8-bit shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D0 or D1 inputs as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/$\overline{\text{P}}$ inputs low. This places the three-state input/output ports in the data input mode. Data is entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip-flop during shifting. An overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

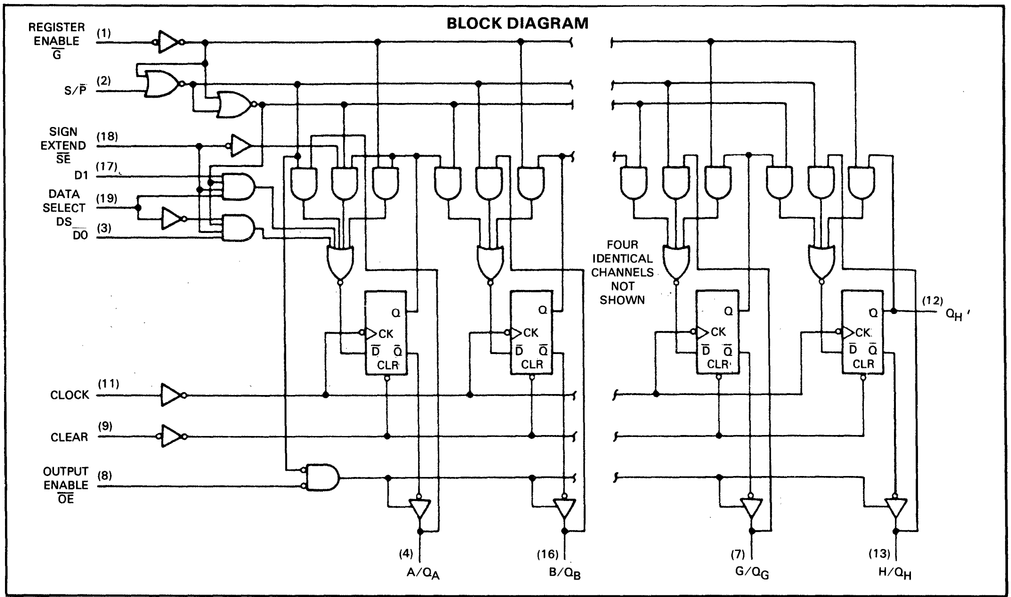
- **MULTIPLEXED INPUTS/OUTPUTS PROVIDE IMPROVED BIT DENSITY**
- **SIGN EXTEND FUNCTION**
- **DIRECT OVERRIDING CLEAR**
- **3-STATE OUTPUTS DRIVE BUS LINES DIRECTLY**

(TOP VIEW)


DATA SELECT
SIGN EXTEND
VCC
D1
B/QB
D/QD
F/QF
H/QH
Q/H'
CLOCK
20
19
18
17
16
15
14
13
12
11
DS
SE
D1
B/QB
D/QD
F/QF
H/GH
Q/H
G
CK
S/P
D0
A/QA
C/QC
E/QE
G/QG
OE
CLR
1
2
3
4
5
6
7
8
9
10
REGISTER ENABLE
S/P
D0
A/QA
C/QC
E/QE
G/QG
OUTPUT ENABLE
CLEAR
GND

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

BLOCK DIAGRAM


REGISTER ENABLE G
(1)
S/P
(2)
SIGN EXTEND SE
(18)
D1
(17)
DATA SELECT DS
(19)
D0
(3)
CLOCK
(11)
CLEAR
(9)
OUTPUT ENABLE OE
(8)
FOUR IDENTICAL CHANNELS NOT SHOWN
Q
CK
D
Q
CLR
(12)
QH'
(4)
A/QA
(16)
B/QB
(7)
G/QG
(13)
H/QH

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range		54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	Q_H'	54,74			−0.4	mA
I_{OL}	Output Current — Low	Q_H' Q_H'	54 74			4.0 8.0	mA
I_{OH}	Output Current — High	Q_A—Q_H Q_A—Q_H	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	Q_A—Q_H Q_A—Q_H	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage Q_A-Q_H	54	2.4	3.2		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.4	3.2		V		
V_{OH}	Output HIGH Voltage Q_H'	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.7	3.4		V		
V_{OL}	Output LOW Voltage Q_A-Q_H	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
V_{OL}	Output LOW Voltage Q_H'	54,74			0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74			0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH Q_A-Q_H				40	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW Q_A-Q_H				−400	µA	V_{CC}= MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	Other			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		A-H, Data Select			40	µA		
		Sign Extend			60	µA		
		Other			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		Data Select			0.2	mA		
		Sign Extend			0.3	mA		
		A-H			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	Other			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Data Select			−0.8	mA		
		Sign Extend			−1.2	mA		
I_{OS}	Short Circuit Current	Q_H'	−20		−100	mA	V_{CC} = MAX	
		Q_A-Q_H	−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				60	mA	V_{CC} = MAX	

FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLEAR	REGISTER ENABLE	$S/\overline{P}$	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q_A	B/Q_B	C/Q_C …	H/Q_H	Q_H'
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}	Q_{H0}
Shift Right	H	L	H	H	L	L	↑	D0	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the $S/\overline{P}$ input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$Q_{A0} \ldots Q_{H0}$ = the level of Q_A through Q_H, respectively, before the indicated steady-state conditions were established
$Q_{An} \ldots Q_{Hn}$ = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a . . . h = the level of steady-state inputs at inputs A through H respectively

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	$C_L = 15$ pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_H'		26 22	35 33	ns	
t_{PHL}	Propagation Delay, Clear to Q_H'		27	35	ns	
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_A-Q_H		22 16	33 25	ns	$C_L = 45$ pF, $R_L = 667\ \Omega$
t_{PHL}	Propagation Delay, Clear to Q_A-Q_H		22	35	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 15	35 35	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		15 15	25 25	ns	$C_L = 5.0$ pF

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width HIGH	25			ns	$V_{CC} = 5.0$ V
t_W	Clock Pulse Width LOW	15			ns	
t_W	Clear Pulse Width LOW	20			ns	
t_s	Data Setup Time	20			ns	
t_s	Select Setup Time	15			ns	
t_h	Data Hold Time	0			ns	
t_h	Select Hold Time	10			ns	
t_{rec}	Recovery Time	20			ns	

DEFINITION OF TERMS:

SETUP TIME t_s is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME t_h is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME t_{rec} is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

MOTOROLA

SN54/74LS323

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the SN54LS/74LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading.

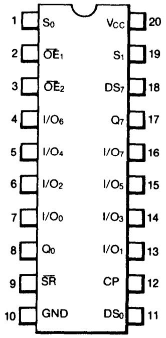
Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD AND STORE**
- **SEPARATE CONTINUOUS INPUTS AND OUTPUTS FROM Q_0 AND Q_7 ALLOW EASY CASCADING**
- **FULLY SYNCHRONOUS RESET**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS_0	Serial Data Input For Right Shift	0.5 U.L.	0.25 U.L.
DS_7	Serial Data Input For Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	1.0 U.L.	0.5 U.L.
	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	
$\overline{SR}$	Synchronous Reset (active LOW) Input	0.5 U.L.	0.25 U.L.

NOTES:
a. 1 TTL LOAD =. 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial Temperature Ranges.
c. The output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial Temperature Ranges.
The output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial Temperature Ranges.

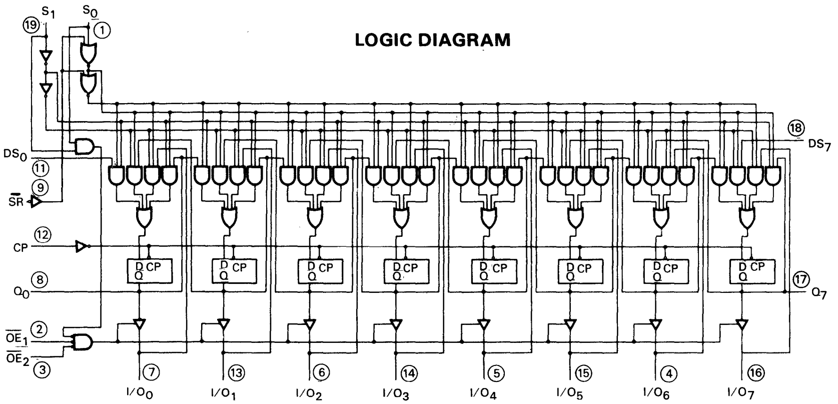
CONNECTION DIAGRAM
DIP (TOP VIEW)


1
S_0
2
$\overline{OE}_1$
3
$\overline{OE}_2$
4
I/O_6
5
I/O_4
6
I/O_2
7
I/O_0
8
Q_0
9
$\overline{SR}$
10
GND
20
V_{CC}
19
S_1
18
DS_7
17
Q_7
16
I/O_7
15
I/O_5
14
I/O_3
13
I/O_1
12
CP
11
DS_0

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


S_1
S_0
⑲
①
DS_0
⑪
⑨
$\overline{SR}$
⑫
CP
⑧
Q_0
$\overline{OE}_1$
②
$\overline{OE}_2$
③
⑱
DS_7
⑰
Q_7
D CP
Q
⑦
I/O_0
⑬
I/O_1
⑥
I/O_2
⑭
I/O_3
⑤
I/O_4
⑮
I/O_5
④
I/O_6
⑯
I/O_7

FUNCTIONAL DESCRIPTION The logic diagram and truth table indicate the functional characteristics of the SN54LS/74LS323 Universal Shift/Storage Register. This device is similar in operation to the SN54LS/74LS299 except for synchronous reset. A partial list of the common features are described below:

1. They use eight D-type edge-triggered flip-flops that respond only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control (S_0, S_1) and data inputs (DS_0, DS_7, I/O_0-I/O_7) may be stable at least a setup time prior to the positive transition of the Clock Pulse.

2. When $S_0 = S_1 = 1$, I/O_0-I/O_7 are parallel inputs to flip-flops Q_0-Q_7 respectively, and the outputs of Q_0-Q_7 are in the high impedance state regardless of the state of $\overline{OE}_1$ or $\overline{OE}_2$.

An important unique feature of the SN54LS/74LS323 is a fully Synchronous Reset that requires only to be stable at least one setup time prior to the positive transition of the Clock Pulse.

TRUTH TABLE

INPUTS								RESPONSE
$\overline{SR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L	X	X	H	X	↑	X	X	Synchronous Reset; $Q_0 = Q_7 =$ LOW I/O voltage undetermined
L	X	X	X	H	↑	X	X	
L	H	H	X	X	↑	X	X	
L	L	X	L	L	↑	X	X	Synchronous Reset; $Q_0 = Q_7 =$ LOW I/O voltage LOW
L	X	L	L	L	↑	X	X	
H	L	H	X	X	↑	D	X	Shift Right; $D \to Q_0$; $Q_0 \to Q_1$; etc.
H	L	H	L	L	↑	D	X	Shift Right; $D \to Q_0$ & I/O_0; $Q_0 \to Q_1$ & I/O_1; etc.
H	H	L	X	X	↑	X	D	Shift Left; $D \to Q_7$; $Q_7 \to Q_6$; etc.
H	H	L	L	L	↑	X	D	Shift Left; $D \to Q_7$ & I/O_7; $Q_7 \to Q_6$ & I/O_6; etc.
H	H	H	X	X	↑	X	X	Parallel Load $I/O_n \to Q_n$
H	L	L	H	X	X	X	X	Hold; I/O Voltage Undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold; $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		54	4.5	5.0	5.5	V
			74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range		54	−55	25	125	°C
			74	0	25	70	
I_{OH}	Output Current — High	Q_0, Q_7	54,74			−0.4	mA
I_{OL}	Output Current — Low	Q_0, Q_7	54			4.0	mA
		Q_0, Q_7	74			8.0	
I_{OH}	Output Current — High	I/O_0—I/O_7	54			−1.0	mA
		I/O_0—I/O_7	74			−2.6	
I_{OL}	Output Current — Low	I/O_0—I/O_7	54			12	mA
		I/O_0—I/O_7	74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage I/O_0—I/O_7	54	2.4	3.2		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.4	3.1		V		
V_{OH}	Output HIGH Voltage Q_0,Q_7	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.7	3.4		V		
V_{OL}	Output LOW Voltage I/O_0-I/O_7	54,74		0.25	0.4	V	$I_{OL} = 12$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 24$ mA	
V_{OL}	Output LOW Voltage Q_0-Q_7	54,74			0.4	V	$I_{OL} = 4.0$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74			0.5	V	$I_{OL} = 8.0$ mA	
I_{OZH}	Output Off Current HIGH I/O_0-I/O_7				40	µA	V_{CC}= MAX, $V_{OUT} = 2.7$ V	
I_{OZL}	Output Off Current LOW I/O_0-I/O_7				−400	µA	V_{CC}= MAX, $V_{OUT} = 0.4$ V	
I_{IH}	Input HIGH Current	Others			20	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
		S_0, S_1, I/O_0-I/O_7			40	µA		
		Others			0.1	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
		S_0, S_1			0.2	mA		
		I/O_0-I/O_7			0.1	mA	V_{CC} = MAX, $V_{IN} = 5.5$ V	
I_{IL}	Input LOW Current	Others			−0.4	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
		S_0, S_1			−0.8	mA		
I_{OS}	Short Circuit Current	Q_0, Q_7	−20		−100	mA	V_{CC} = MAX	
		I/O_0-I/O_7	−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				53	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	$C_L = 15$ pF
t_{PHL}	Propagation Delay, Clock to Q_0 or Q_7		26	39	ns	
t_{PLH}			22	33		
t_{PHL}	Propagation Delay, Clock to I/O_0-I/O_7		25	39	ns	$C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH}			17	25		
t_{PZH}	Output Enable Time		14	21	ns	
t_{PZL}			20	30		
t_{PHZ}	Output Disable Time		10	15	ns	$C_L = 5.0$ pF
t_{PLZ}			10	15		

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width HIGH	25			ns	$V_{CC} = 5.0\ V$
t_W	Clock Pulse Width LOW	15			ns	
t_W	Clear Pulse Width LOW	20			ns	
t_s	Data Setup Time	20			ns	
t_s	Select Setup Time	35			ns	
t_h	Data Hold Time	0			ns	
t_h	Select Hold Time	10			ns	
t_{rec}	Recovery Time	20			ns	

3 - STATE WAVEFORMS

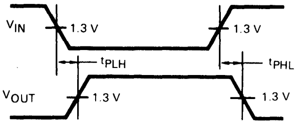

V_IN
1.3 V
1.3 V
t_PLH
t_PHL
V_OUT
1.3 V
1.3 V

Fig. 1

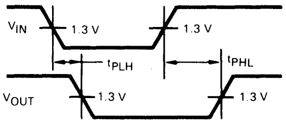

V_IN
1.3 V
1.3 V
t_PLH
t_PHL
V_OUT
1.3 V
1.3 V

Fig. 2

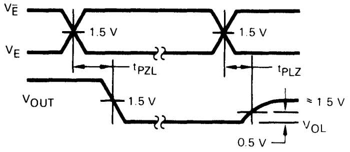

V_Ē
V_E
1.5 V
1.5 V
t_PZL
t_PLZ
V_OUT
1.5 V
≈ 1.5 V
V_OL
0.5 V

Fig. 3

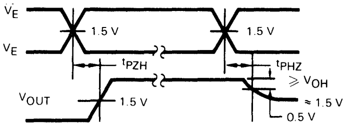
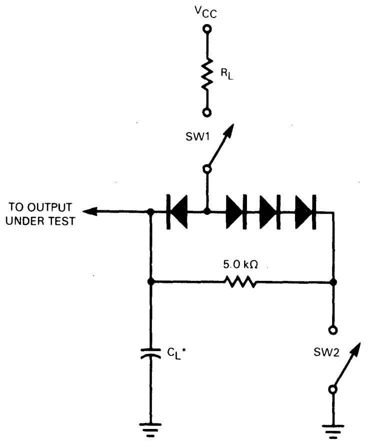

V_Ē
V_E
1.5 V
1.5 V
t_PZH
t_PHZ
≥ V_OH
V_OUT
1.5 V
≈ 1.5 V
0.5 V

Fig. 4

AC LOAD CIRCUIT


V_CC
R_L
SW1
TO OUTPUT UNDER TEST
5.0 kΩ
C_L*
SW2

*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

MOTOROLA

SN54/74LS348
SN54/74LS848

8-INPUT PRIORITY ENCODER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS348 and the SN54LS/74LS848 are eight input priority encoders which provide the 8-line to 3-line function.

The outputs(A0–A2) and inputs (0–7) are active low. The active low input which has the highest priority (input 7 has the highest) is represented on the outputs (output A0 is the lowest bit). An example would be if inputs 1, 2 and 4 were low, then a binary 4 would be represented on the outputs.

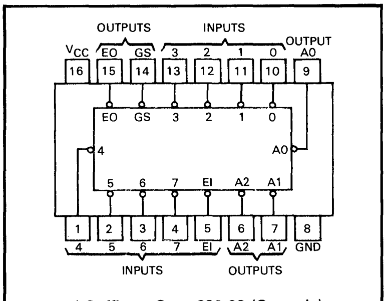
The GS (Group Signal) output is active low when any of the inputs are low. It serves to indicate when any of the inputs are active.

A0, A1 and A2 are three-state outputs. This allows for up to 64 line expansion without the need for special external circuitry.

A logical one on the Enable Input (EI) forces A0, A1 and A2 to the disabled state and outputs GS and EO to the high state. A high on all data inputs (0–7) together with a low on the EI input disables outputs A0, A1, and A2 and forces output GS to the high state and output EO to the low state.

Use of the EI input in conjunction with the EO output provides for the capability of having priority encoding of n input signals.

The LS848 has special internal circuitry providing for a greatly reduced negative going glitch on the GS (Group Signal) output and on a reduced tendency for the A0, A1 and A2 outputs to become momentarily enabled. Both of these occurrences happen when the EI input goes from a logical one to a logical zero and all data inputs (0–7) are held at logical ones. The internal glitch reduction circuitry does add an additional fan-in of one on all data inputs (compared to that of the LS348).


OUTPUTS
INPUTS
OUTPUT
VCC
EO
GS
3
2
1
0
A0
16
15
14
13
12
11
10
9
EO GS 3 2 1 0
4
A0
5 6 7 EI A2 A1
1
2
3
4
5
6
7
8
4
5
6
7
EI
A2
A1
GND
INPUTS
OUTPUTS

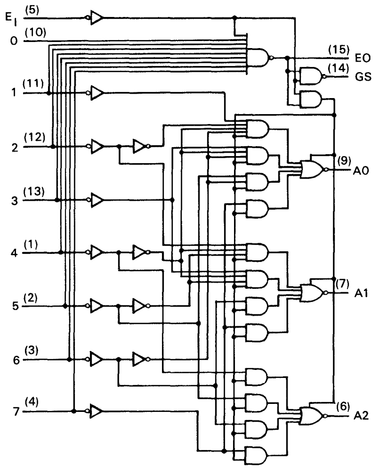
J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

FUNCTION TABLE

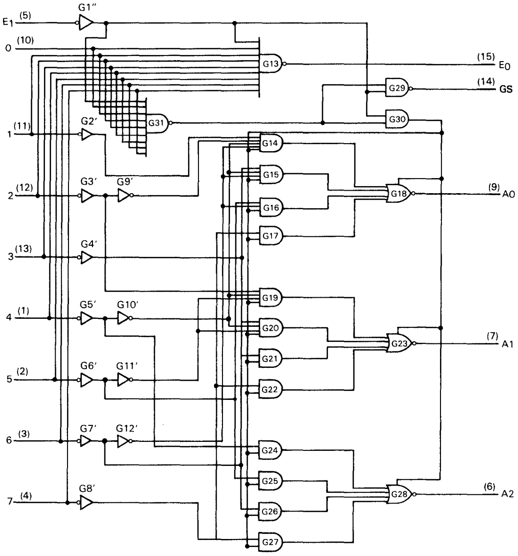
INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level
L = low logic level
X = irrelevant
Z = high impedance state

BLOCK DIAGRAMS


EI (5)
0 (10)
1 (11)
2 (12)
3 (13)
4 (1)
5 (2)
6 (3)
7 (4)
(15) EO
(14) GS
(9) A0
(7) A1
(6) A2

SN54LS/74LS348


E1 (5)
0 (10)
1 (11)
2 (12)
3 (13)
4 (1)
5 (2)
6 (3)
7 (4)
G1″
G2′
G3′
G9′
G4′
G5′
G10′
G6′
G11′
G7′
G12′
G8′
G13
G14
G15
G16
G17
G18
G19
G20
G21
G22
G23
G24
G25
G26
G27
G28
G29
G30
G31
(15) EO
(14) GS
(9) A0
(7) A1
(6) A2

SN54LS/74LS848

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High EO, GS	54,74			−0.4	mA
I_{OH}	Output Current — High A0, A1, A2 A0, A1, A2	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low EO, GS	54 74			4.0 8.0	mA
I_{OL}	Output Current — Low A0, A1, A2 A0, A1, A2	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage A0, A1, A2	54,74	2.4	3.1		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
	EO, GS	54	2.5	3.5		V		
	EO, GS	74	2.7	3.5		V		
V_{OL}	Output LOW Voltage EO, GS	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
V_{OL}	Output LOW Voltage A0, A1, A2	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current Input 0, EI — LS348				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Input 0 — LS848				40	μA		
	Other — LS348				40	μA		
	Other — LS848				60	μA		
	Input 0, EI — LS348				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
	Input 0 — LS848				0.2	mA		
	Other — LS348				0.2	mA		
	Other — LS848				0.3	mA		
I_{IL}	Input LOW Current Input 0, EI — LS348				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	Input 0 — LS848				−0.8	mA		
	Other — LS348				−0.8	mA		
	Other — LS848				−1.2	mA		
I_{OS}	Short Circuit Current	EO, GS	−20		−120	mA	V_{CC} = MAX	
		A0,A1,A2	−30		−130	mA		
I_{CC}	Power Supply Current Total, Output HIGH			12	23	mA	V_{CC} = MAX, All Inputs and Outputs Open	
	Total, Output LOW			13	25		V_{CC} = MAX, Inputs 7, E1 = GND All Others Open	

AC CHARACTERISTICS: $V_{CC} = 5.0$ V, $T_A = 25°C$

SYMBOL	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	LS348 LIMITS			LS848 LIMITS			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	1 thru 7	A0, A1, or A2	In-Phase output		11	17		12	18	ns	$C_L = 45$ pF
t_{PHL}					20	30		20	30		
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-Phase output		23	35		23	35	ns	$R_L = 667\ \Omega$
t_{PHL}					23	35		23	35		
t_{PZH}	EI	A0, A1, or A2			25	39		25	39	ns	
t_{PZL}					24	41		24	41		
t_{PLH}	0 thru 7	EO	Out-of-Phase output		11	18		11	18	ns	
t_{PHL}					26	40		26	40		
t_{PLH}	0 thru 7	GS	In-Phase output		38	55		38	55	ns	$C_L = 15$ pF
t_{PHL}					9.0	21		9.0	21		
t_{PLH}	EI	GS	In-Phase output		11	17		11	17	ns	$R_L = 2.0\ k\Omega$
t_{PHL}					14	36		14	36		
t_{PLH}	EI	EO	In-Phase output		17	21		17	21	ns	
t_{PHL}					25	40		30	45		
t_{PHZ}	EI	A0, A1 or A2			18	27		18	27	ns	$C_L = 5.0$ pF
t_{PLZ}					23	35		23	35		$R_L = 667\ \Omega$

SN54/74LS352

DUAL 4-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

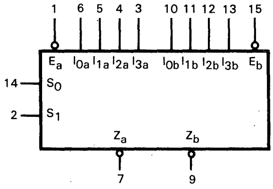
DESCRIPTION — The SN54LS/74LS352 is a very high-speed Dual 4-Input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The SN54LS/74LS352 is the functional equivalent of the SN54LS/74LS153 except with inverted outputs.

- **INVERTED VERSION OF THE SN54LS/74LS153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0—I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}$	Multiplexer Outputs (note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

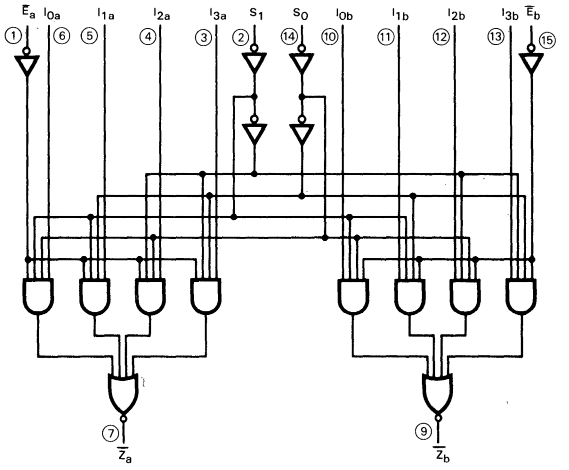
LOGIC SYMBOL



1 6 5 4 3 10 11 12 13 15
E_a I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b} E_b
14 S_0
2 S_1
Z_a Z_b
7 9

V_{CC} = Pin 16
GND = Pin 8

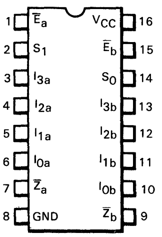
LOGIC DIAGRAM



$\overline{E}_a$ I_{0a} I_{1a} I_{2a} I_{3a} S_1 S_0 I_{0b} I_{1b} I_{2b} I_{3b} $\overline{E}_b$
① ⑥ ⑤ ④ ③ ② ⑭ ⑩ ⑪ ⑫ ⑬ ⑮
⑦ $\overline{Z}_a$
⑨ $\overline{Z}_b$

V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 $\overline{E}_a$
2 S_1
3 I_{3a}
4 I_{2a}
5 I_{1a}
6 I_{0a}
7 $\overline{Z}_a$
8 GND
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Z}_b$

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS352 is a Dual 4-Input Multiplexer. It selects two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\bar{E}_a$, $\bar{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\bar{E}_a$, $\bar{E}_b$) are HIGH, the corresponding outputs ($\bar{Z}_a$, $\bar{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below.

$$\bar{Z}_a = \bar{E}_a \bullet (\overline{I_{0a} \bullet \bar{S}_1 \bullet \bar{S}_0 + I_{1a} \bullet \bar{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \bar{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\bar{Z}_b = \bar{E}_b \bullet (\overline{I_{0b} \bullet \bar{S}_1 \bullet \bar{S}_0 + I_{1b} \bullet \bar{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \bar{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

The SN54LS/74LS352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The SN54LS/74LS352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	$\bar{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		19 25	29 38	ns	Fig. 1 or 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		16 21	24 32	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		13 17	20 26	ns	Fig. 1	

AC WAVEFORMS

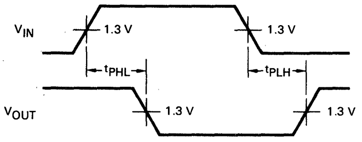


Fig. 1

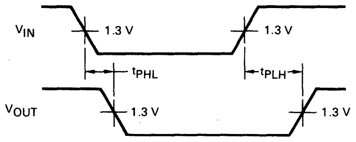


Fig. 2

MOTOROLA

SN54/74LS353

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

- **INVERTED VERSION OF SN54LS/74LS253**
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

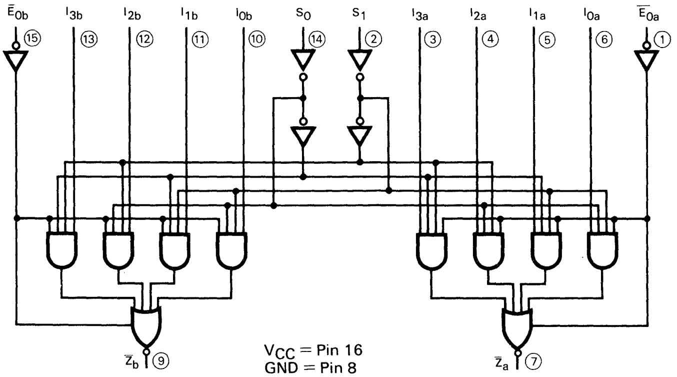
PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_{0a}—I_{3a}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}_a$	Multiplexer Output (Note b)	65(25)U.L.	15(7.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_{0b}—I_{3b}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}_b$	Multiplexer Output (Note b)	65(25)U.L.	15(7.5) U.L.

NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

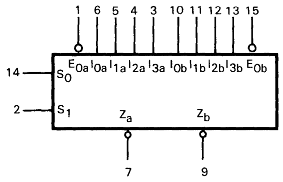
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC DIAGRAM


$\overline{E}_{0b}$ ⑮
I_{3b} ⑬
I_{2b} ⑫
I_{1b} ⑪
I_{0b} ⑩
S_0 ⑭
S_1 ②
I_{3a} ③
I_{2a} ④
I_{1a} ⑤
I_{0a} ⑥
$\overline{E}_{0a}$ ①
$\overline{Z}_b$ ⑨
$\overline{Z}_a$ ⑦

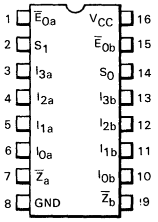
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL


1 6 5 4 3 10 11 12 13 15
$\overline{E}_{0a}$ I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b} $\overline{E}_{0b}$
14 S_0
2 S_1
$\overline{Z}_a$
$\overline{Z}_b$
7
9

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 $\overline{E}_{0a}$
2 S_1
3 I_{3a}
4 I_{2a}
5 I_{1a}
6 I_{0a}
7 $\overline{Z}_a$
8 GND
16 V_{CC}
15 $\overline{E}_{0b}$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Z}_b$

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS353 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable (E_{0a}, E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The logic equations for the outputs are shown below:

$$\overline{Z_a} = \overline{\bar{E}_{0a} \bullet (I_{0a} \bullet \bar{S}_1 \bullet \bar{S}_0 + I_{1a} \bullet \bar{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \bar{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z_b} = \overline{\bar{E}_{0b} \bullet (I_{0b} \bullet \bar{S}_1 \bullet \bar{S}_0 + I_{1b} \bullet \bar{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \bar{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\bar{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Level
L = LOW Level
X = Immaterial
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage $Q_A - Q_H$	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output 3-State				14	mA	V_{CC} = MAX	
	Total, Output LOW				12			

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		11 13	25 20	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 21	45 32	ns	Fig. 1 or 2	
t_{PZH}	Output Enable Time to HIGH Level		11	23	ns	Figs. 4, 5	
t_{PZL}	Output Enable Time to LOW Level		15	23	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		12	27	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level		27	41	ns	Figs. 4, 5	

3- STATE WAVEFORMS

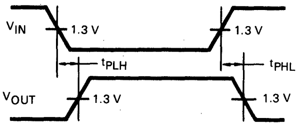

V_{IN}
1.3 V
1.3 V
t_{PLH}
t_{PHL}
V_{OUT}
1.3 V
1.3 V

Fig. 1

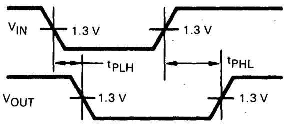

V_{IN}
1.3 V
1.3 V
t_{PLH}
t_{PHL}
V_{OUT}
1.3 V
1.3 V

Fig. 2

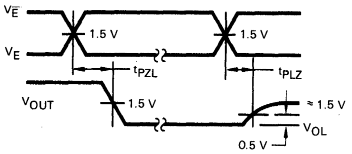

$V_{\overline{E}}$
V_E
1.5 V
1.5 V
t_{PZL}
t_{PLZ}
V_{OUT}
1.5 V
≈ 1.5 V
V_{OL}
0.5 V

Fig. 3

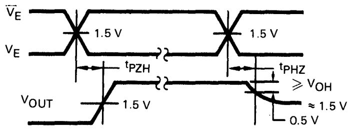
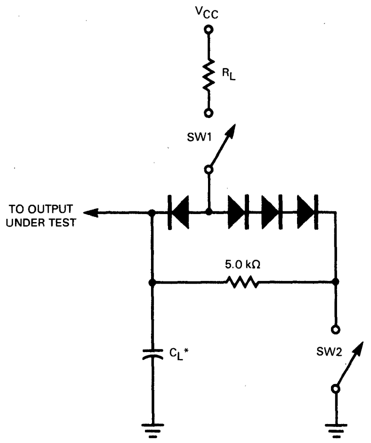

$V_{\overline{E}}$
V_E
1.5 V
1.5 V
t_{PZH}
t_{PHZ}
≥ V_{OH}
V_{OUT}
1.5 V
≈ 1.5 V
0.5 V

Fig. 4

AC LOAD CIRCUIT


V_{CC}
R_L
SW1
TO OUTPUT UNDER TEST
5.0 kΩ
C_L*
SW2

*Includes Jig and Probe Capacitance.

Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

MOTOROLA

SN54/74LS365A
SN54/74LS366A
SN54/74LS367A
SN54/74LS368A

3-STATE HEX BUFFERS

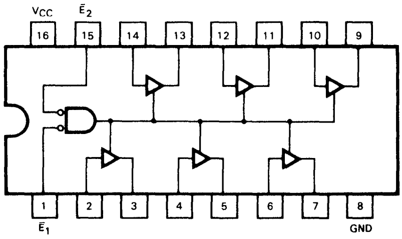
LOW POWER SCHOTTKY

DESCRIPTION — These devices are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

When the Output Enable (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

SN54LS/74LS365A
HEX 3-STATE BUFFER WITH
COMMON 2-INPUT NOR ENABLE

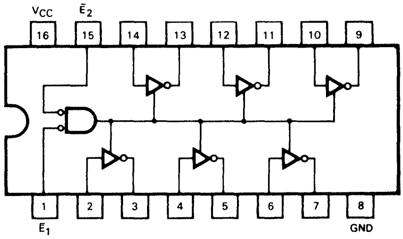


V_{CC}
$\overline{E}_2$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
$\overline{E}_1$
GND

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

SN54LS/74LS366A
HEX 3-STATE INVERTER BUFFER
WITH COMMON 2-INPUT NOR ENABLE

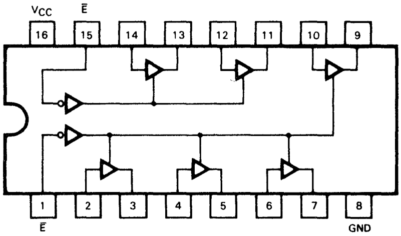


V_{CC}
$\overline{E}_2$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
$\overline{E}_1$
GND

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

SN54LS/74LS367A
HEX 3-STATE BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS

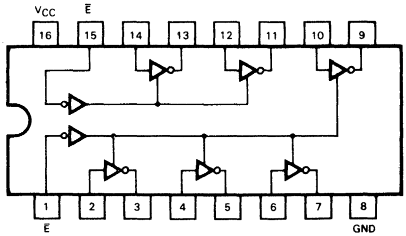


V_{CC}
$\overline{E}$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
$\overline{E}$
GND

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

SN54LS/74LS368A
HEX 3-STATE INVERTER BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS



V_{CC}
$\overline{E}$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
$\overline{E}$
GND

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.4 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{E}$ Inputs				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	D Inputs				−20	µA	V_{CC} = MAX, V_{IN} = 0.5 V Either, $\overline{E}$ Input at 2 V	
					−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V Both $\overline{E}$ Inputs at 0.4 V	
I_{OS}	Short Circuit Current		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current LS365A, 367A				24	mA	V_{CC} = MAX	
	LS366A, 368A				21			

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS LS365A/LS367A MIN	LIMITS LS365A/LS367A TYP	LIMITS LS365A/LS367A MAX	LIMITS LS366A/LS368A MIN	LIMITS LS366A/LS368A TYP	LIMITS LS366A/LS368A MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay		10 9.0	16 22		7.0 12	15 18	ns	C_L = 45 pF, R_L = 667 Ω
t_{PZH} t_{PZL}	Output Enable Time		19 24	35 40		18 28	35 45	ns	
t_{PHZ} t_{PLZ}	Output Disable Time			30 35			32 35	ns	C_L = 5.0 pF

MOTOROLA

SN54/74LS373
SN54/74LS374

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS;

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{\text{OE}}$) is LOW. When $\overline{\text{OE}}$ is HIGH the bus output is in the high impedence state.

The SN54LS/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54LS/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**
- **HYSTERESIS ON LATCH ENABLE**
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **HYSTERESIS ON CLOCK INPUT TO IMPROVE NOISE MARGIN**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a) HIGH	LOADING (Note a) LOW
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{\text{OE}}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0—O_7	Outputs (Note b)	65(25)U.L.	15(7.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

LS373

Dn	LE	$\overline{\text{OE}}$	On
H	H	L	H
L	H	L	L
X	X	H	Z*

LS374

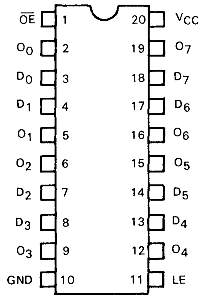
Dn	CP	$\overline{\text{OE}}$	On
H	↑	L	H
L	↑	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedence

*Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{\text{OE}}$)

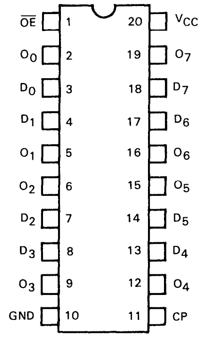
CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS373



CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS374

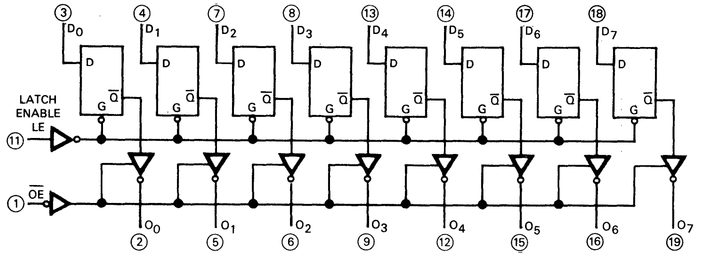


J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

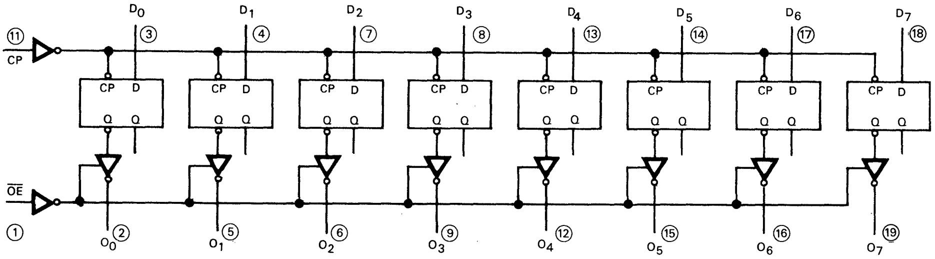
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS

SN54LS/74LS373


③ D0
④ D1
⑦ D2
⑧ D3
⑬ D4
⑭ D5
⑰ D6
⑱ D7
D
G
Q̄
LATCH ENABLE LE
⑪
OE
①
O0 ②
O1 ⑤
O2 ⑥
O3 ⑨
O4 ⑫
O5 ⑮
O6 ⑯
O7 ⑲

SN54LS/74LS374


D0 ③
D1 ④
D2 ⑦
D3 ⑧
D4 ⑬
D5 ⑭
D6 ⑰
D7 ⑱
⑪
CP
CP D
Q Q
OE
①
O0 ②
O1 ⑤
O2 ⑥
O3 ⑨
O4 ⑫
O5 ⑮
O6 ⑯
O7 ⑲

V_{CC} = Pin 20
GND = Pin 10
○ = Pin Numbers

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				40	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS373			LS374				
		MIN	TYP	MAX	MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency				35	50		MHz	C_L = 45 pF, R_L = 667 Ω
t_{PLH}	Propagation Delay, Data to Output		12	18				ns	
t_{PHL}			12	18					
t_{PLH}	Clock or Enable to Output		20	30		15	28	ns	
t_{PHL}			18	30		19	28		
t_{PZH}	Output Enable Time		15	28		20	28	ns	
t_{PZL}			25	36		21	28		
t_{PHZ}	Output Disable Time		12	20		12	20	ns	C_L = 5.0 pF
t_{PLZ}			15	25		15	25		

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS				UNITS
		LS373		LS374		
		MIN	MAX	MIN	MAX	
t_W	Clock Pulse Width	15		15		ns
t_s	Setup Time	5.0		20		ns
t_h	Hold Time	20		0		ns

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

AC WAVEFORMS

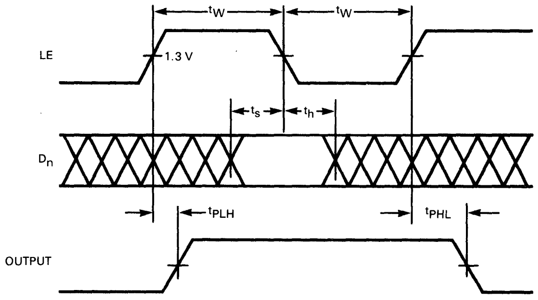

tW
tW
LE
1.3 V
ts
th
Dn
tPLH
tPHL
OUTPUT

Fig. 1

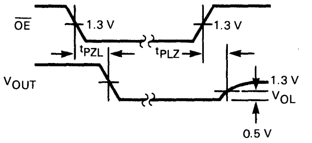

OE
1.3 V
1.3 V
tPZL
tPLZ
VOUT
1.3 V
VOL
0.5 V

Fig. 2

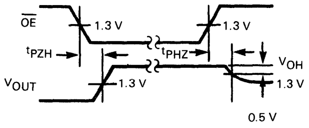
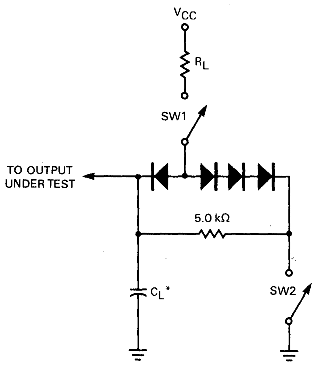

OE
1.3 V
1.3 V
tPZH
tPHZ
VOH
VOUT
1.3 V
1.3 V
0.5 V

Fig. 3

AC LOAD CIRCUIT


VCC
RL
SW1
TO OUTPUT
UNDER TEST
5.0 kΩ
CL*
SW2

*Includes Jip and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 4

AC WAVEFORMS

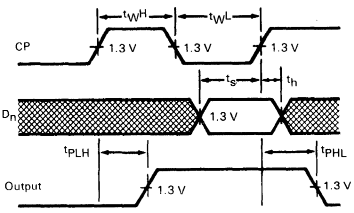

t_{WH}
t_{WL}
CP
1.3 V
1.3 V
1.3 V
t_s
t_h
D_n
1.3 V
t_{PLH}
t_{PHL}
Output
1.3 V
1.3 V

Fig. 5

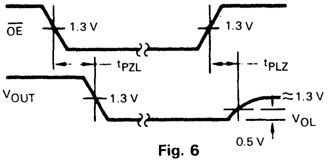

$\overline{OE}$
1.3 V
1.3 V
t_{PZL}
t_{PLZ}
V_{OUT}
1.3 V
≈1.3 V
V_{OL}
0.5 V

Fig. 6

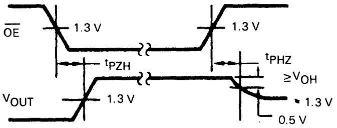
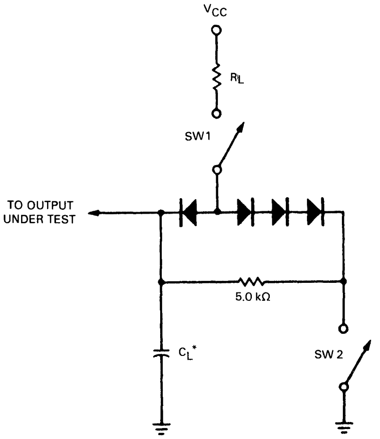

$\overline{OE}$
1.3 V
1.3 V
t_{PZH}
t_{PHZ}
≥V_{OH}
V_{OUT}
1.3 V
1.3 V
0.5 V

Fig. 7

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

AC LOAD CIRCUIT


V_{CC}
R_L
SW1
TO OUTPUT UNDER TEST
5.0 kΩ
C_L*
SW 2

*Includes Jig and Probe Capacitance.

Fig. 8

MOTOROLA

SN54/74LS375

4-BIT D LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.

TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

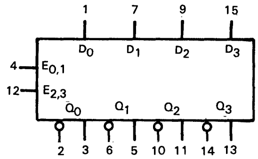
NOTES:
t_n = bit time before enable negative-going transition
t_{n+1} = bit time after enable negative-going transition

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_1—D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1—Q_4	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q_1}$—$\overline{Q_4}$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

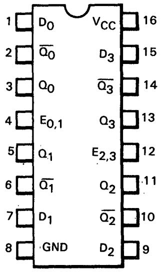
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL


1
7
9
15
D0
D1
D2
D3
4
E0,1
12
E2,3
Q̄0
Q1
Q2
Q3
2
3
6
5
10
11
14
13

V_{CC} = 16
GND = Pin 8

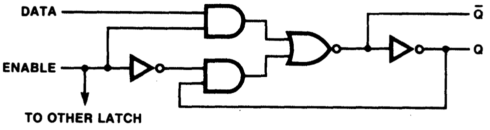
CONNECTION DIAGRAM
DIP (TOP VIEW)


1
D0
2
Q̄0
3
Q0
4
E0,1
5
Q1
6
Q̄1
7
D1
8
GND
16
VCC
15
D3
14
Q̄3
13
Q3
12
E2,3
11
Q2
10
Q̄2
9
D2

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


DATA
ENABLE
TO OTHER LATCH
Q̄
Q

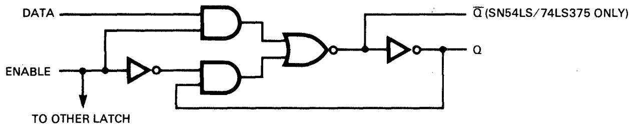
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, $I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0$ mA	$V_{CC} = V_{CC}$ MIN, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0$ mA	
I_{IH}	Input HIGH Current	D Input E Input			20 80	µA	V_{CC} = MAX, $V_{IN} = 2.7$ V	
		D Input E Input			0.1 0.4	mA	V_{CC} = MAX, $V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current	D Input E Input			−0.4 −1.6	mA	V_{CC} = MAX, $V_{IN} = 0.4$ V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				12	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		15 9.0	27 17	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Q}$		12 7.0	20 15	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		15 14	27 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$		16 7.0	30 15	ns	

LOGIC DIAGRAM


DATA
ENABLE
TO OTHER LATCH
$\overline{Q}$ (SN54LS/74LS375 ONLY)
Q

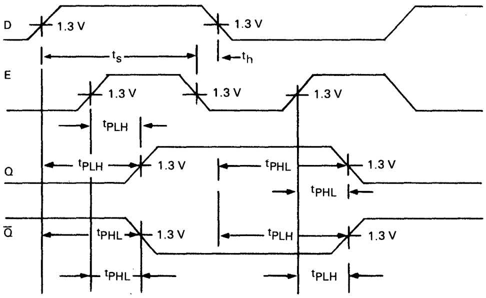
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Enable Pulse Width	20			ns	$V_{CC} = 5.0$ V
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

AC WAVEFORMS


D
1.3 V
1.3 V
t_s
t_h
E
1.3 V
1.3 V
1.3 V
t_{PLH}
Q
t_{PLH}
1.3 V
t_{PHL}
1.3 V
t_{PHL}
$\overline{Q}$
t_{PHL}
1.3 V
t_{PLH}
1.3 V
t_{PHL}
t_{PLH}

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

MOTOROLA

SN54/74LS377
SN54/74LS378
SN54/74LS379

OCTAL D FLIP-FLOP WITH ENABLE; HEX D FLIP-FLOP WITH ENABLE; 4-BIT D FLIP-FLOP WITH ENABLE

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

The SN54LS/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the SN54LS/74LS174, but with common Enable rather than common Master Reset.

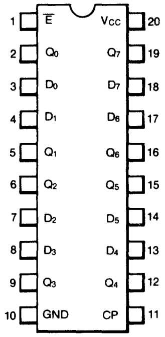
The SN54LS/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the SN54LS/74LS175 but features the common Enable rather than common Master Reset.

- **8-BIT HIGH SPEED PARALLEL REGISTERS**
- **POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **TRUE AND COMPLEMENT OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0—D_3	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0—Q_3	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0$—$\overline{Q}_3$	Complemented Outputs (Note b)	10 U.L	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

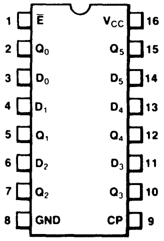
CONNECTION DIAGRAM
DIP (TOP VIEW)
SN54LS/74LS377


1 E̅
2 Q0
3 D0
4 D1
5 Q1
6 Q2
7 D2
8 D3
9 Q3
10 GND
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

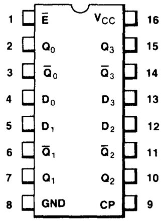
CONNECTION DIAGRAM
DIP (TOP VIEW)
SN54LS/74LS378


1 E̅
2 Q0
3 D0
4 D1
5 Q1
6 D2
7 Q2
8 GND
16 VCC
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

CONNECTION DIAGRAM
DIP (TOP VIEW)
SN54LS/74LS379

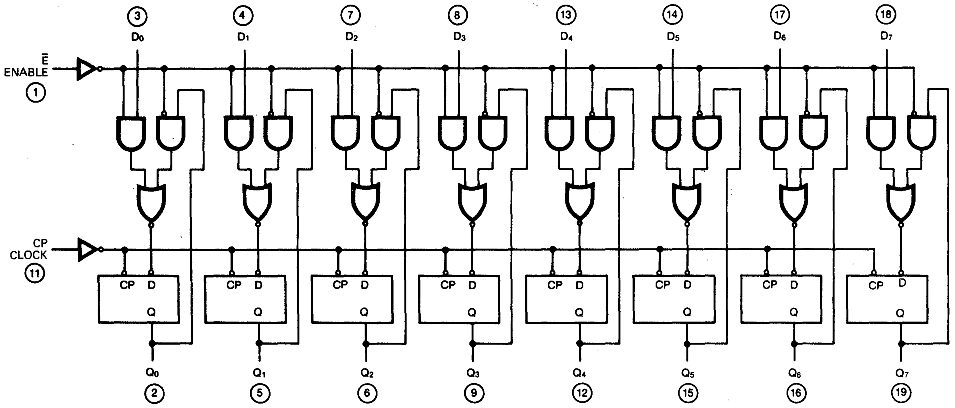

1 E̅
2 Q0
3 Q̅0
4 D0
5 D1
6 Q̅1
7 Q1
8 GND
16 VCC
15 Q3
14 Q̅3
13 D3
12 D2
11 Q̅2
10 Q2
9 CP

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

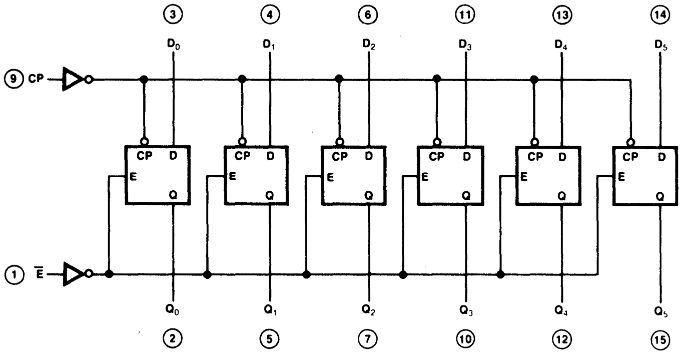
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS

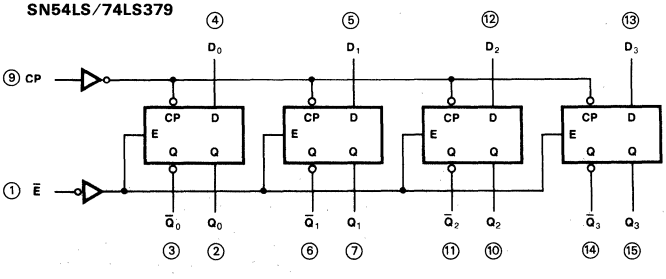
SN54LS/74LS377


③ D0
④ D1
⑦ D2
⑧ D3
⑬ D4
⑭ D5
⑰ D6
⑱ D7
$\overline{E}$ ENABLE ①
CP CLOCK ⑪
CP D Q
Q0 ②
Q1 ⑤
Q2 ⑥
Q3 ⑨
Q4 ⑫
Q5 ⑮
Q6 ⑯
Q7 ⑲

SN54LS/74LS378


③ D0
④ D1
⑥ D2
⑪ D3
⑬ D4
⑭ D5
⑨ CP
① $\overline{E}$
CP D E Q
Q0 ②
Q1 ⑤
Q2 ⑦
Q3 ⑩
Q4 ⑫
Q5 ⑮

SN54LS/74LS379


④ D0
⑤ D1
⑫ D2
⑬ D3
⑨ CP
① $\overline{E}$
CP D E Q Q
$\overline{Q}_0$ ③
Q0 ②
$\overline{Q}_1$ ⑥
Q1 ⑦
$\overline{Q}_2$ ⑪
Q2 ⑩
$\overline{Q}_3$ ⑭
Q3 ⑮

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current	LS377 LS378 LS379			28 22 15	mA	V_{CC} = MAX, NOTE 1

Note: With all inputs open and GND applied to all data and enable inputs, I_{CC} is measured after a momentary GND, then 4.5 V is applied to clock.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	30	40		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Propagation Delay, Clock to Output		17	27	ns	
t_{PHL}			18	27		

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
t_W	Any Pulse Width		20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time		20			ns	
t_s	Enable Setup Time	Inactive — State	10			ns	
		Active — State	25			ns	
t_h	Any Hold Time		5.0			ns	

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

TRUTH TABLE

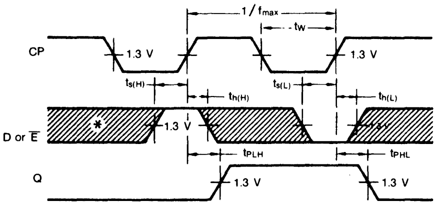
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	No Change	No Change
L	↑	H	H	L
L	↑	L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

AC WAVEFORMS

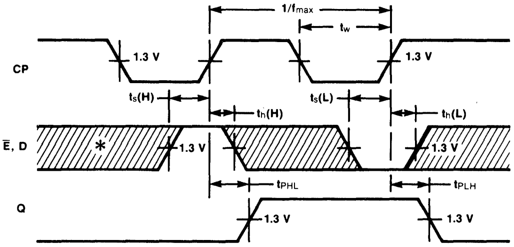
SN54LS/74LS377

**CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH, FREQUENCY,
SETUP AND HOLD TIMES DATA OR ENABLE TO CLOCK**


1 / fmax
tw
CP
1.3 V
1.3 V
ts(H)
th(H)
ts(L)
th(L)
D or $\overline{E}$
*
1.3 V
1.3 V
tPLH
tPHL
Q
1.3 V
1.3 V

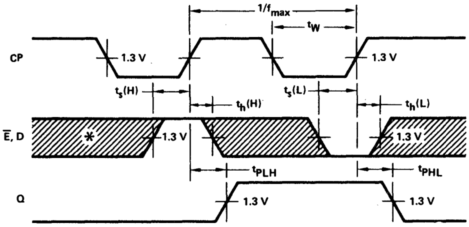
SN54LS/74LS378

**CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH, FREQUENCY,
SETUP AND HOLD TIMES DATA OR ENABLE TO CLOCK**


1/fmax
tw
CP
1.3 V
1.3 V
ts(H)
th(H)
ts(L)
th(L)
$\overline{E}$, D
*
1.3 V
1.3 V
tPHL
tPLH
Q
1.3 V
1.3 V

SN54LS/74LS379

**CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH, FREQUENCY,
SETUP AND HOLD TIMES DATA, ENABLE TO CLOCK**


1/fmax
tW
CP
1.3 V
1.3 V
ts(H)
th(H)
ts(L)
th(L)
$\overline{E}$, D
*
1.3 V
1.3 V
tPLH
tPHL
Q
1.3 V
1.3 V

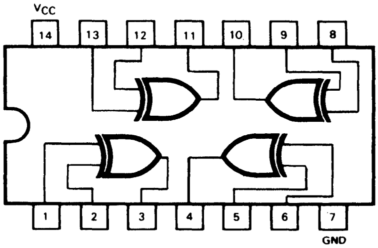
*The shaded areas indicate when the input is permitted to change for predictable output performance.

MOTOROLA

SN54/74LS386

QUAD 2-INPUT EXCLUSIVE-OR GATE

LOW POWER SCHOTTKY



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				10	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		12 10	23 17	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		20 13	30 22	ns	

MOTOROLA

SN54/74LS390
SN54/74LS393

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS390 and SN54LS/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the 'LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- **DUAL VERSIONS OF LS290 AND LS293**
- **LS390 HAS SEPARATE CLOCKS ALLOWING ÷2, ÷2.5, ÷5**
- **INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER**
- **TYPICAL MAX COUNT FREQUENCY OF 50 MHZ**
- **INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS**

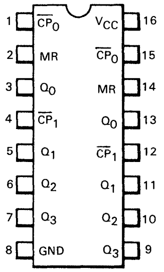
PIN NAMES **LOADING** (Note a)

PIN NAMES		LOADING HIGH	LOADING LOW
$\overline{CP}$	Clock (Active LOW going edge) Input to ÷16 (LS393)	0.5 U.L.	1.0 U.L.
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 (LS390)	0.5 U.L.	1.5 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.25 U.L.
Q_0—Q_3	Flip-Flop outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

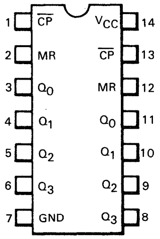
CONNECTION DIAGRAMS
DIP (TOP VIEW)

SN54LS/74LS390



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

SN54LS/74LS393



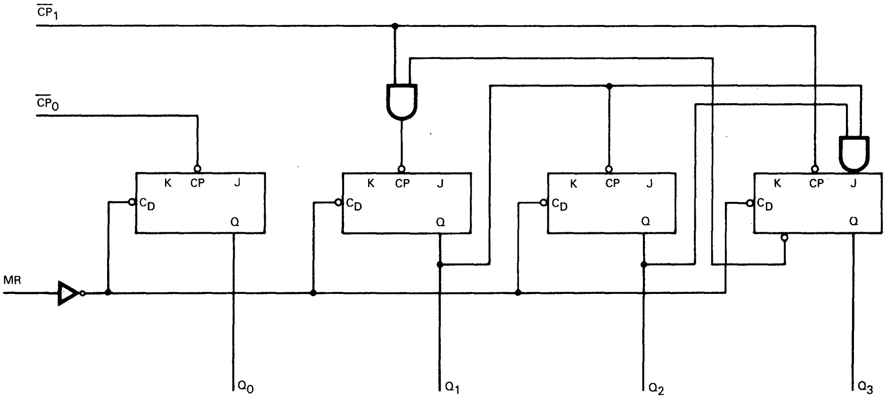
J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

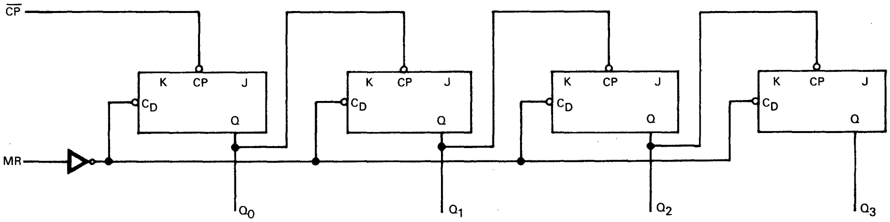
FUNCTIONAL DESCRIPTION—Each half of the SN54LS/74LS393 Operates in the Modulo16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the 'LS390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 4.2.1 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to $\overline{CP}_1$ and connect the Q_3 output to the $\overline{CP}_0$ input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to $\overline{CP}_0$ and the Q_0 output is connected to $\overline{CP}_1$, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of 'LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

SN54LS/74LS390 LOGIC DIAGRAM (one half shown)



SN54LS/74LS393 LOGIC DIAGRAM (one half shown)



SN54LS/74LS390 BCD TRUTH TABLE
(Input on $\overline{CP_0}$; $Q_0 \cdot \overline{CP_1}$)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

SN54LS/74LS390 ÷ 5 TRUTH TABLE
(Input on $\overline{CP_1}$)

COUNT	OUTPUTS		
	Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

SN54LS/74LS393 TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	MR			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		$\overline{CP}$, $\overline{CP_0}$			−1.6	mA		
		$\overline{CP_1}$			−2.4	mA		
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				26	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency $\overline{CP}_0$ to Q_0		25	35		MHz	$C_L = 15$ pF
f_{MAX}	Maximum Clock Frequency $\overline{CP}_1$ to Q_1		12.5	20		MHz	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0	LS393		12 13	20 20	ns	
t_{PLH} t_{PHL}	$\overline{CP}_0$ to Q_0	LS390		12 13	20 20	ns	
t_{PLH} t_{PHL}	$\overline{CP}$ to Q_3	LS393		40 40	60 60	ns	
t_{PLH} t_{PHL}	$\overline{CP}_0$ to Q_2	LS390		37 39	60 60	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_1	LS390		13 14	21 21	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_2	LS390		24 26	39 39	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ to Q_3	LS390		13 14	21 21	ns	
t_{PHL}	MR to Any Output	LS390/393		24	39	ns	

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
t_W	Clock Pulse Width	LS393	20			ns	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_0$ Pulse Width	LS390	20			ns	
t_W	$\overline{CP}_1$ Pulse Width	LS390	40			ns	
t_W	MR Pulse Width	LS390/393	20			ns	
t_{rec}	Recovery Time	LS390/393	25			ns	

AC WAVEFORMS

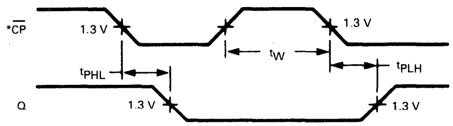


Fig. 1

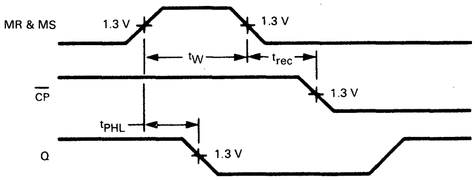


Fig. 2

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.

SN74LS395

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

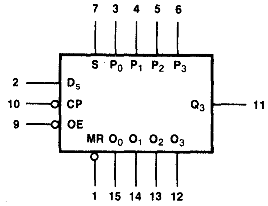
DESCRIPTION — The SN74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active HIGH Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- **SHIFT LEFT OR PARALLEL 4-BIT REGISTER**
- **3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
S	Mode Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
O_0—O_3	3-State Register Outputs	65 U.L.	15 U.L.
Q_3	Register Output	10 U.L.	5 U.L.

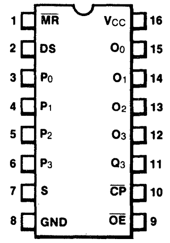
NOTE:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL


7 3 4 5 6
S P0 P1 P2 P3
2 Ds
10 CP
9 OE
Q3 11
MR O0 O1 O2 O3
1 15 14 13 12

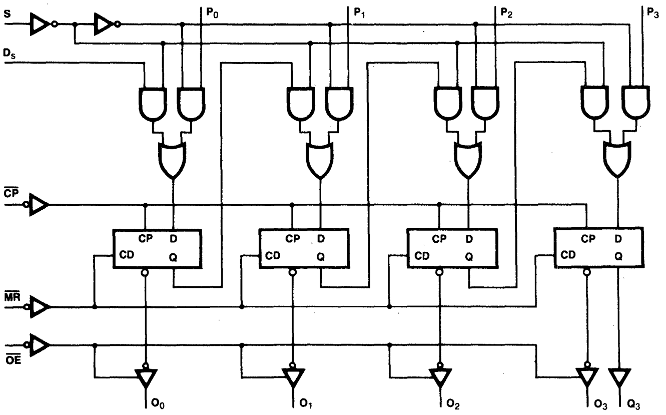
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 MR
2 DS
3 P0
4 P1
5 P2
6 P3
7 S
8 GND
16 VCC
15 O0
14 O1
13 O2
12 O3
11 Q3
10 CP
9 OE

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

LOGIC DIAGRAM


S
Ds
P0
P1
P2
P3
CP
MR
OE
CP D
CD Q
O0
O1
O2
O3
Q3

FUNCTIONAL DESCRIPTION — The SN74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (Pn) input or from the preceding stage. When the Select input is HIGH, the Pn inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the P_n, D_S and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2, O_2 to P_1 and O_1 to P_0, with P_3 acting as the linking input from another package.

When the $\overline{OE}$ input is HIGH, the output buffers are disabled and the Q_0–Q_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			−0.4	mA
I_{OL}	Output Current — Low			8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH			20	μA	V_{CC} = MAX, V_O = 2.4 V
I_{OZL}	Output Off Current LOW			−20	μA	V_{CC} = MAX, V_O = 0.4 V
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
				−0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current	−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH			31	mA	V_{CC} = MAX, $\overline{OE}$ = GND, $\overline{CP}$ = GND
	Total, Output LOW			34	mA	V_{CC} = MAX, $\overline{OE}$ = 4.5 V, $\overline{CP}$ momentary 3.0 V then GND

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PHL}	Propagation Delay, Clear to Output		22	35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Low to High Propagation Delay, High to Low		15 25	30 30	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 17	25 25	ns	
t_{PLZ} t_{PHZ}	Output Disable Time		12 11	20 17	ns	$C_L = 5.0$ pF

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	16			ns	$V_{CC} = 5.0$ V
t_s	Setup Time, Mode Select	40			ns	
t_s	Setup Time, All Others	20			ns	
t_h	Data Hold Time	10			ns	

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_s	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	↘	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H	↘	L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H	↘	H	X	P_n	P_0	P_1	P_2	P_3

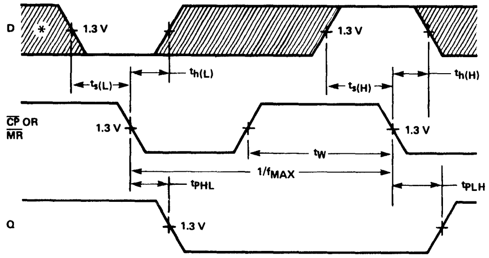
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

$t_{n,\ n+1}$ = time before and after CP HIGH-to-LOW transition

NOTE:
When $\overline{OE}$ is HIGH, outputs O_0—O_3 are in the high impedance state; however, this does not affect other operations or the O_3 output.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.


D
*
1.3 V
1.3 V
$t_{s(L)}$
$t_{h(L)}$
$t_{s(H)}$
$t_{h(H)}$
$\overline{CP}$ OR
$\overline{MR}$
1.3 V
1.3 V
t_W
$1/f_{MAX}$
t_{PHL}
t_{PLH}
Q
1.3 V

*The Data Input is D_S for S = LOW and P_n for S = HIGH.

Fig. 1

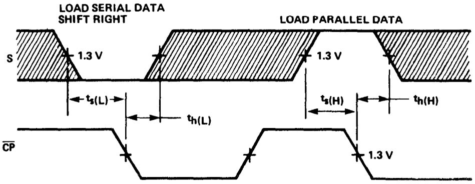

LOAD SERIAL DATA
SHIFT RIGHT
LOAD PARALLEL DATA
S
1.3 V
1.3 V
$t_{s(L)}$
$t_{h(L)}$
$t_{s(H)}$
$t_{h(H)}$
$\overline{CP}$
1.3 V

Fig. 2

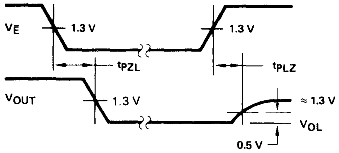

$V_{\overline{E}}$
1.3 V
1.3 V
t_{PZL}
t_{PLZ}
V_{OUT}
1.3 V
≈ 1.3 V
V_{OL}
0.5 V

Fig. 3

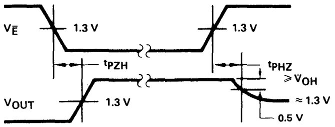
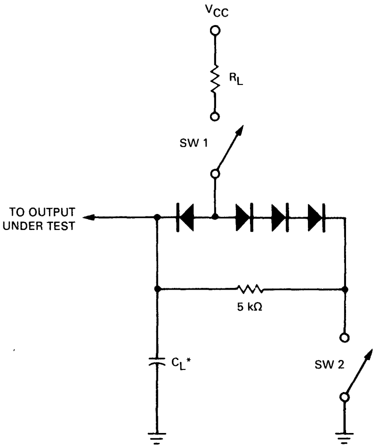

$V_{\overline{E}}$
1.3 V
1.3 V
t_{PZH}
t_{PHZ}
$\geq V_{OH}$
V_{OUT}
1.3 V
≈ 1.3 V
0.5 V

Fig. 4

AC LOAD CIRCUIT


V_{CC}
R_L
SW 1
TO OUTPUT
UNDER TEST
5 kΩ
C_L*
SW 2

*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

MOTOROLA

SN54/74LS398
SN54/74LS399

QUAD 2-PORT REGISTER

LOW POWER SCHOTTKY

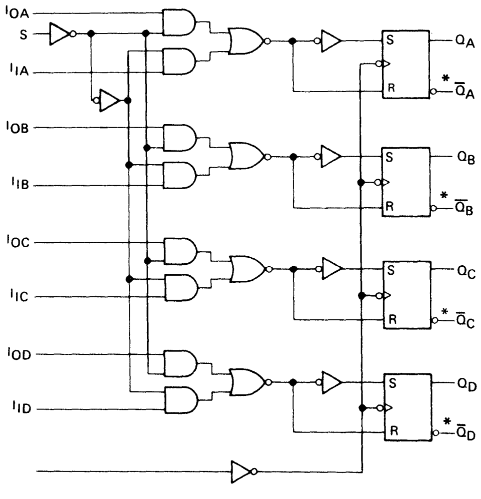
DESCRIPTION — The SN54LS/74LS398 and SN54LS/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The SN54LS/74LS398 features both Q and $\overline{Q}$ inputs, while the SN54LS/74LS399 has only Q outputs.

- **SELECT FROM TWO DATA SOURCES**
- **FULLY POSITIVE EDGE-TRIGGERED OPERATION**
- **BOTH TRUE AND COMPLEMENTED OUTPUTS ON SN54LS/74LS398**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
I_{0a}—I_{0d}	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
I_{1a}—I_{0d}	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
Q_a—Q_d	Register True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_a$—$\overline{Q}_d$	Register Complementary Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

FUNCTIONAL BLOCK DIAGRAM

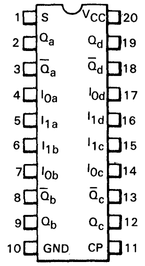


I_{0A}
S
I_{1A}
I_{0B}
I_{1B}
I_{0C}
I_{1C}
I_{0D}
I_{1D}
S
R
Q_A
* $\overline{Q}_A$
Q_B
* $\overline{Q}_B$
Q_C
* $\overline{Q}_C$
Q_D
* $\overline{Q}_D$

* **SN54LS/74LS398 only**

CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS398



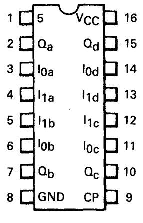
1 S
2 Q_a
3 $\overline{Q}_a$
4 I_{0a}
5 I_{1a}
6 I_{1b}
7 I_{0b}
8 $\overline{Q}_b$
9 Q_b
10 GND
20 V_{CC}
19 Q_d
18 $\overline{Q}_d$
17 I_{0d}
16 I_{1d}
15 I_{1c}
14 I_{0c}
13 $\overline{Q}_c$
12 Q_c
11 CP

V_{CC} = Pin 20
GND = Pin 10

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS399



1 S
2 Q_a
3 I_{0a}
4 I_{1a}
5 I_{1b}
6 I_{0b}
7 Q_b
8 GND
16 V_{CC}
15 Q_d
14 I_{0d}
13 I_{1d}
12 I_{1c}
11 I_{0c}
10 Q_c
9 CP

V_{CC} = 16
GND = 8

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

FUNCTIONAL DESCRIPTION — The SN54LS/74LS398 and SN54LS/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The SN54LS/74LS398 has both Q and $\overline{Q}$ Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

***SN54LS/74LS398 only**

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				13	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output Q		18 21	27 32	ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	20			ns	$V_{CC} = 5.0\ V$
t_s	Data Setup Time	25			ns	
t_s	Select Setup Time	45			ns	
t_h	Hold Time, Any Input	0			ns	

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

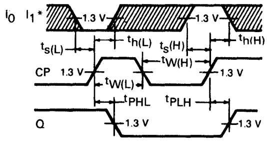

I0 I1*
1.3 V
1.3 V
ts(L)
th(L)
ts(H)
th(H)
tW(H)
CP 1.3 V
1.3 V
tW(L)
tPHL
tPLH
Q
1.3 V
1.3 V

Fig. 1

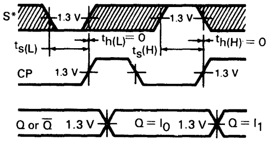

S*
1.3 V
1.3 V
ts(L)
th(L) = 0
ts(H)
th(H) = 0
CP 1.3 V
1.3 V
Q or Q̄ 1.3 V
Q = I0 1.3 V
Q = I1

Fig. 2

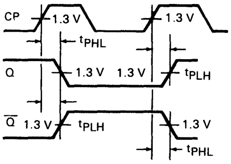

CP
1.3 V
1.3 V
tPHL
Q
1.3 V 1.3 V
tPLH
Q̄ 1.3 V
tPLH
1.3 V
tPHL

Fig. 3

*The shaded areas indicate when the input is permitted to change for predictable output performance.

MOTOROLA

SN54/74LS490

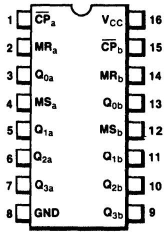
DUAL DECADE COUNTER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the SN54LS/74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8, 4, 2, 1 BCD code.

- **DUAL VERSION OF SN54LS/74LS90**
- **INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER**
- **COUNT FREQUENCY — TYPICALLY 65 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 $\overline{CP}_a$
2 MR_a
3 Q_{0a}
4 MS_a
5 Q_{1a}
6 Q_{2a}
7 Q_{3a}
8 GND
16 V_{CC}
15 $\overline{CP}_b$
14 MR_b
13 Q_{0b}
12 MS_b
11 Q_{1b}
10 Q_{2b}
9 Q_{3b}

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

PIN NAMES

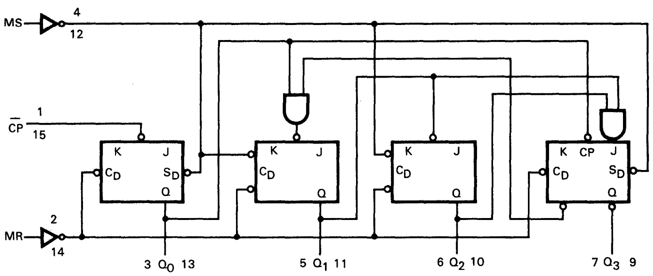
		LOADING (Note a) HIGH	LOW
MS	Master Set (Set to 9) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Input (Active LOW Going Edge)	1.5 U.L.	1.5 U.L.
Q_0—Q_3	Counter Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

COUNT	OUTPUTS Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LOGIC DIAGRAM (ONE HALF SHOWN)



MS
4
12
$\overline{CP}$
1
15
MR
2
14
K
J
C_D
S_D
Q
CP
3 Q_0 13
5 Q_1 11
6 Q_2 10
7 Q_3 9

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	MS, MR			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Clock			−1.6	mA		
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				26	mA	V_{CC} = MAX	

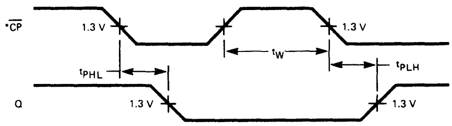
AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Any Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	MR or MS to Setup Time	25			ns	

AC CHARACTERISTICS: $T_A = 25°C$

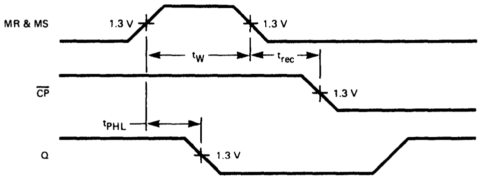
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	25	35		MHz	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0		12 13	20 20	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_1 or Q_3		24 26	39 39	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_2		32 36	54 54	ns	Fig. 2	
t_{PHL}	Propagation Delay, MR to Output		24	39	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, MS to Output		24 20	39 36	ns	Fig. 2	

AC WAVEFORMS



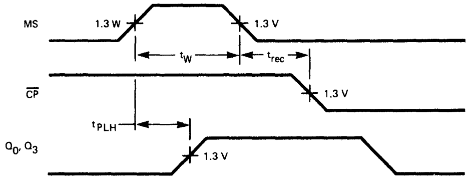
*$\overline{CP}$
1.3 V
1.3 V
t_W
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V

Fig. 1



MR & MS
1.3 V
1.3 V
t_W
t_{rec}
$\overline{CP}$
1.3 V
t_{PHL}
Q
1.3 V

Fig. 2



MS
1.3 W
1.3 V
t_W
t_{rec}
$\overline{CP}$
1.3 V
t_{PLH}
Q_0, Q_3
1.3 V

Fig. 3

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.

MOTOROLA

SN54/74LS540
SN54/74LS541

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS540 and SN54LS/74LS541 are octal buffers and line drivers with the same functions as the LS240 and LS241, but with pinouts on the opposite side of the package.

These device types are designed to be used as memory address drivers, clockdrivers and bus-oriented transmitters/receivers. These devices are especially useful as output ports for the microprocessors, allowing ease of layout and greater PC board density.

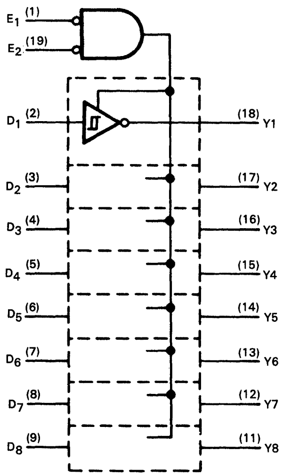
- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGIN**
- **PNP INPUTS REDUCE LOADING**
- **3-STATE OUTPUTS DRIVE BUS LINES**
- **INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIER INTERFACE TO MICROPROCESSORS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**

INPUTS			OUTPUTS	
E_1	E_2	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

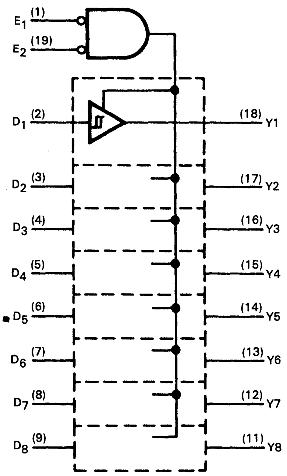
BLOCK DIAGRAM

LS540



E1 (1)
E2 (19)
D1 (2)
(18) Y1
D2 (3)
(17) Y2
D3 (4)
(16) Y3
D4 (5)
(15) Y4
D5 (6)
(14) Y5
D6 (7)
(13) Y6
D7 (8)
(12) Y7
D8 (9)
(11) Y8

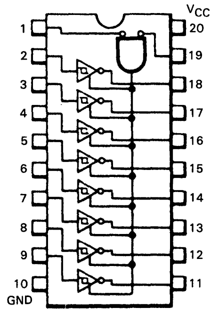
LS541



E1 (1)
E2 (19)
D1 (2)
(18) Y1
D2 (3)
(17) Y2
D3 (4)
(16) Y3
D4 (5)
(15) Y4
D5 (6)
(14) Y5
D6 (7)
(13) Y6
D7 (8)
(12) Y7
D8 (9)
(11) Y8

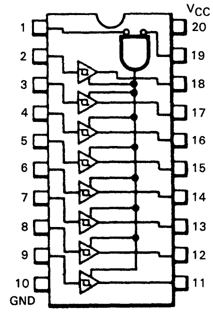
LOGIC DIAGRAMS AND CONNECTION DIAGRAMS
DIP (TOP VIEW)

SN54LS/74LS540



VCC
1
2
3
4
5
6
7
8
9
10
GND
20
19
18
17
16
15
14
13
12
11

SN54LS/74LS541



VCC
1
2
3
4
5
6
7
8
9
10
GND
20
19
18
17
16
15
14
13
12
11

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

GUARANTEED OPERATING RANGES

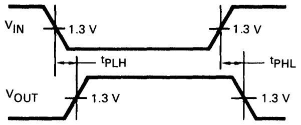
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA
		54,74	2.0			V	V_{CC} =MIN, I_{OH} =MAX, V_{IL} =0.5 V
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
V_{T+}, V_{T-}	Hysteresis		0.2	0.4		V	V_{CC} =MIN
I_{OZH}	Output Off Current High				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V
I_{OZL}	Output Off Current Low				−20	μA	V_{CC} = MAX, V_{OUT} =0.4 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} =MAX, V_{IN} =2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−40		−225	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH	LS540			25	mA	V_{CC} =MAX
		LS541			32	mA	
	Total, Output LOW	LS540			45	mA	
		LS541			52	mA	
	Total Output 3-State	LS540			52	mA	
		LS541			55	mA	

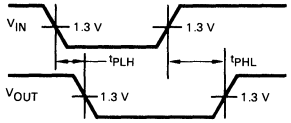
AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Data to Output	LS540		9.0	15	ns	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH}		LS541		12	15		
t_{PHL}		LS540		12	15		
t_{PHL}		LS541		12	18		
t_{PZH}	Output Enable Time to HIGH Level	LS540		15	25	ns	
		LS541		15	32		
t_{PZL}	Output Enable Time to LOW Level	LS540		20	38	ns	
		LS541		20	38		
t_{PHZ}	Output Disable Time from HIGH Level	LS540		10	18	ns	$C_L = 5.0$ pF
		LS541		10	18		
t_{PLZ}	Output Disable Time from LOW Level	LS540		15	25	ns	
		LS541		15	29		



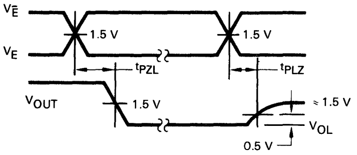
V_IN
1.3 V
1.3 V
t_PLH
t_PHL
V_OUT
1.3 V
1.3 V

Fig. 1



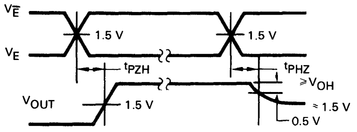
V_IN
1.3 V
1.3 V
t_PLH
t_PHL
V_OUT
1.3 V
1.3 V

Fig. 2



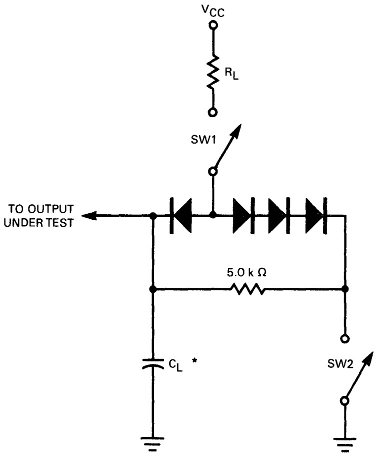
V_Ē
V_E
1.5 V
1.5 V
t_PZL
t_PLZ
V_OUT
1.5 V
≈ 1.5 V
V_OL
0.5 V

Fig. 3



V_Ē
V_E
1.5 V
1.5 V
t_PZH
t_PHZ
≥V_OH
V_OUT
1.5 V
≈ 1.5 V
0.5 V

Fig. 4



V_CC
R_L
SW1
TO OUTPUT UNDER TEST
5.0 k Ω
C_L *
SW2

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

MOTOROLA

SN54/74LS569

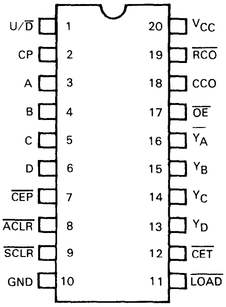
FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS569 is designed as programmable up/down BCD and Binary counters respectively. These devices have 3-state outputs for use in bus organized systems. With the exception of output enable ($\overline{\text{OE}}$) and asynchronous clear ($\overline{\text{ACLR}}$), all functions occur on the positive edge of the clock pulse (CP).

When the $\overline{\text{LOAD}}$ input is LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Enabling of the counters occurs only when $\overline{\text{CEP}}$ and $\overline{\text{CET}}$ are LOW and LOAD is HIGH. Direction of the count is controlled by the up-down input (U/$\overline{\text{D}}$), HIGH counts up and LOW counts down. High-speed counting and cascading is implemented by internal look-ahead carry logic and an active LOW ripple carry output ($\overline{\text{RCO}}$). On the LS569, the $\overline{\text{RCO}}$ is LOW at binary 15 during up-count and during down-count it is also LOW at binary 0. During normal cascading operation $\overline{\text{RCO}}$ connected to the succeeding block at $\overline{\text{CET}}$ is the only requisite. When counting and when $\overline{\text{RCO}}$ is LOW, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse. Two active LOW reset lines are provided, a master reset asynchronous clear ($\overline{\text{ACLR}}$) and a synchronous clear ($\overline{\text{SCLR}}$). When in a HIGH state, the output control ($\overline{\text{OE}}$) input forces the counter output into a HIGH impedance state and when LOW, the counter outputs are enabled.

CONNECTION DIAGRAM
(TOP VIEW)



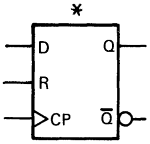
J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)
V_{CC} = Pin 20
GND = Pin 10
Note: Pin 1 is marked for orientation.

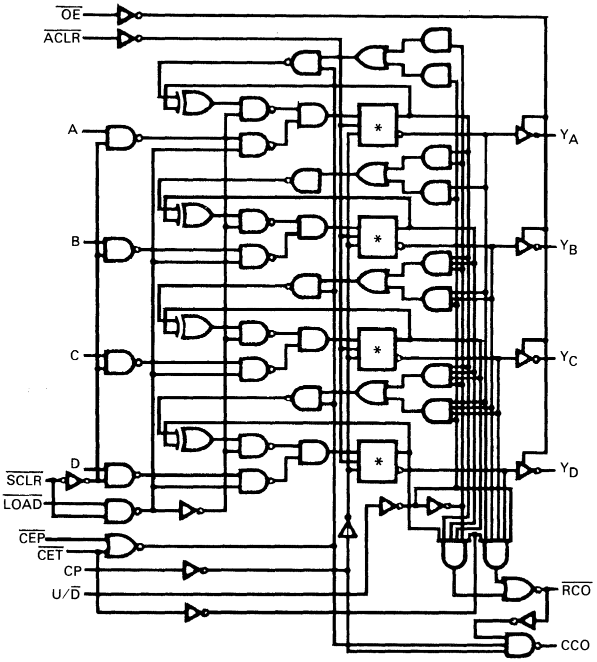
FUNCTION TABLE

INPUTS									OUTPUTS						
CP	D C B A	$\overline{\text{LOAD}}$	$\overline{\text{CET}}$	$\overline{\text{CEP}}$	U/$\overline{\text{D}}$	$\overline{\text{ACLR}}$	$\overline{\text{SCLR}}$	$\overline{\text{OE}}$	$\overline{\text{RCO}}$	CCO	Y_D	Y_C	Y_B	Y_A	
↑	X X X X	H	L	L	H	H	H	L	A/R	A/R	$(Q_T - CP) + 1$				Count Up
↑	X X X X	H	L	L	L	H	H	L	A/R	A/R	$(Q_T - CP) - 1$				Count Down
↑	X X X X	H	H	X	X	H	H	L	H	H	NC	NC	NC	NC	Count Inhibit
↑	X X X X	H	L	H	X	H	H	L	A/R	H	NC	NC	NC	NC	Count Inhibit
Ω	X X X X	X	L	L	H	H	H	L	L	⎍	H	H	H	H	Overflow
↑	X X X X	X	L	H	H	H	H	L	L	H	H	H	H	H	Overflow
↑	X X X X	X	H	X	H	H	H	L	H	H	H	H	H	H	Overflow Inhibit
⎍	X X X X	X	L	L	L	H	H	L	L	⎍	L	L	L	L	Underflow
↑	X X X X	X	L	H	L	H	H	L	L	H	L	L	L	L	Underflow
↑	X X X X	X	H	X	L	H	H	L	H	H	L	L	L	L	Underflow Inhibit
↑	L H L H	L	X	X	X	H	H	L	H	H	L	H	L	H	Load Example
↑	X X X X	X	H	X	H	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
⎍	X X X X	X	L	L	L	H	L	L	L	⎍	L	L	L	L	Clear (Synchronous)
↑	X X X X	X	L	H	L	H	L	L	L	H	L	L	L	L	Clear (Synchronous)
↑	X X X X	X	H	X	L	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
X	X X X X	X	X	X	H	L	X	L	H	H	L	L	L	L	Asynchronous Clear
⎍	X X X X	X	L	L	L	L	X	L	L	⎍	L	L	L	L	Asynchronous Clear
X	X X X X	X	L	H	L	L	X	L	L	H	L	L	L	L	Asynchronous Clear
X	X X X X	X	H	X	L	L	X	L	H	H	L	L	L	L	Asynchronous Clear
X	X X X X	X	X	X	X	X	X	H	X	X	Hi-Z				Output Disabled

$(Q_T - CP)$ = Output state prior to clock edge
NC = No change
A/R = Assumes required output state;
High except during Overflow and Underflow
X = Don't care

LOGIC DIAGRAM

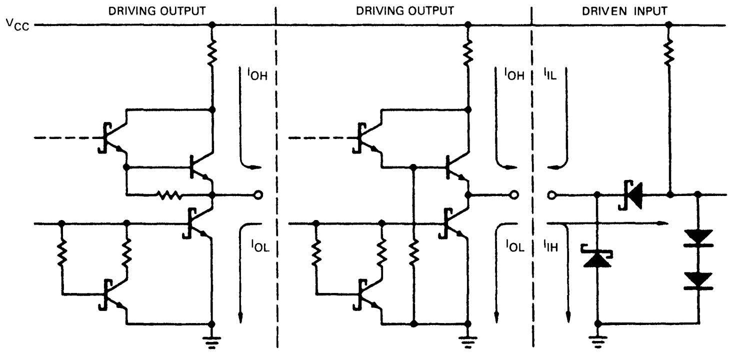

*
D
Q
R
CP
$\overline{Q}$


$\overline{OE}$
$\overline{ACLR}$
A
B
C
D
$\overline{SCLR}$
$\overline{LOAD}$
$\overline{CEP}$
$\overline{CET}$
CP
U/$\overline{D}$
*
Y_A
Y_B
Y_C
Y_D
$\overline{RCO}$
CCO

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D	The four programmable data inputs.
$\overline{\text{CEP}}$	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{\text{CEP}}$ must be LOW to count.
$\overline{\text{CET}}$	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
CP	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
$\overline{\text{LOAD}}$	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
U/$\overline{\text{D}}$	Up/Down Count Control. HIGH counts up and LOW counts down.
$\overline{\text{ACLR}}$	Asynchronous Clear. Master reset of counters to zero when $\overline{\text{ACLR}}$ is LOW, independent of the clock.
$\overline{\text{SCLR}}$	Synchronous clear of counters to zero on the next clock edge when $\overline{\text{SCLR}}$ is LOW.
$\overline{\text{OE}}$	A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output.
Y_A, Y_B, Y_C, Y_D	The four counter outputs.
$\overline{\text{RCO}}$	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, $\overline{\text{RCO}}$ is LOW at 0000.
CCO	Clock Carry Output. While counting and $\overline{\text{RCO}}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High Except $\overline{RCO}$, CCO	54			−1.0	mA
		74			−2.6	
I_{OH}	Output Current — High $\overline{RCO}$, CCO	54,74			−0.44	mA
I_{OL}	Output Current — Low Except $\overline{RCO}$, CCO	54			12	mA
		74			24	
I_{OL}	Output Current — Low, RCO, CCO	54			4	mA
		74			8	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS			UNITS	TEST CONDITIONS
				MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage		54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
			74			0.8		
V_{IK}	Input Clamp Diode Voltage				−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	YA-YD	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
			74	2.4	3.1		V	
		$\overline{RCO}$, CCO	54	2.5	3.5		V	
			74	2.7	3.5		V	
V_{OL}	Output LOW Voltage		54,74		0.25	0.4	V	I_{OL} = I_{OL} MAX V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			74		0.35	0.5	V	
I_{OZH}	Output Off Current—High					20	µA	V_{CC} = MAX, V_O = 2.7 V
I_{OZL}	Output Off Current—Low					−20	µA	V_{CC} = MAX, V_O = 0.4 V
I_{IH}	Input HIGH Current					20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
						0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	Others				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
		$\overline{CET}$				−0.8	mA	
I_{OS}	Short Circuit Current	$\overline{RCO}$,CCO		−20		−100	mA	V_{CC} = MAX
		Others		−30		−130	mA	
I_{CC}	Power Supply Current, 3-State					43	mA	V_{CC} = MAX

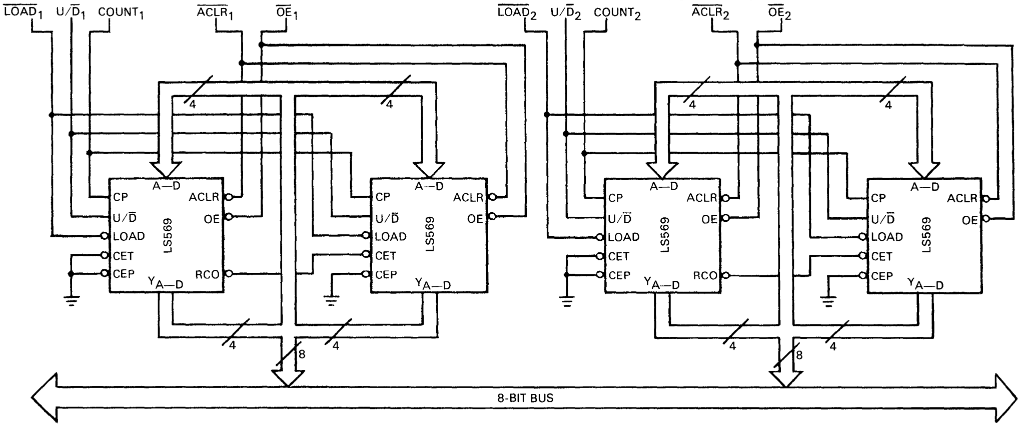
AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Toggle Frequency	25			MHz	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		15 23	24 35	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CET}}$ to $\overline{\text{RCO}}$		14 14	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay U/D to $\overline{\text{RCO}}$		20 15	30 24	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to $\overline{\text{RCO}}$		25 26	40 40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CET}}$ or $\overline{\text{CEP}}$ to CCO		12 20	20 30	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to CCO		17 26	27 40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{ACLR}}$ to Q		21 21	32 32	ns	
t_{PZH} t_{PZL}	Output Enable Time		10 17	16 24	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		20 17	25 27	ns	$C_L = 5.0$ pF

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Clock Pulse Width (Low)	30			ns	$V_{CC} = 5.0$ V
t_s	Setup Time, A, B, C, D	20			ns	
t_s	Setup Time, $\overline{\text{SCLR}}$	20			ns	
t_s	Setup Time, $\overline{\text{LOAD}}$	30			ns	
t_s	Setup Time, U/$\overline{\text{D}}$	50			ns	
t_s	Setup Time, $\overline{\text{CET}}$, $\overline{\text{CEP}}$	32			ns	
t_h	Hold Time, Any Inputs	0			ns	

MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS



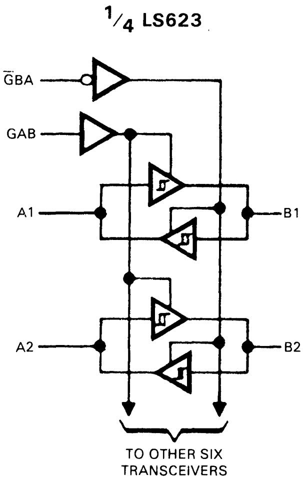
SN54/74LS623

DESCRIPTION — The SN54LS/74LS623 series is an octal bus transceiver designed for asynchronous two-way communication between data buses. Control function implementation allows maximum timing flexibility. Enable inputs may be used to disable the device so that buses are effectively isolated. Depending on the Logic Levels at the enable inputs, Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus. The dual-enable configuration gives the LS623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled all other data sources to the two sets of bus lines (16 in all) will remain at their last states.

OCTAL BUS TRANSCEIVER

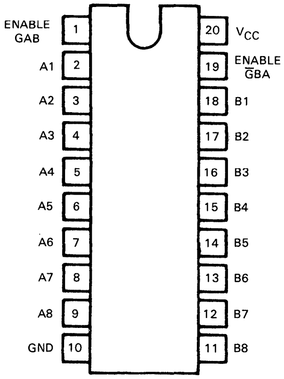
LOW POWER SCHOTTKY

BLOCK DIAGRAM


$^1/_4$ LS623
$\overline{G}$BA
GAB
A1
B1
A2
B2
TO OTHER SIX TRANSCEIVERS

CONNECTION DIAGRAM

(TOP VIEW)


ENABLE GAB
A1
A2
A3
A4
A5
A6
A7
A8
GND
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
V_{CC}
ENABLE $\overline{G}$BA
B1
B2
B3
B4
B5
B6
B7
B8

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	LS623
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

H = high level, L = low level, X = irrelevant

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−3.0	mA
		54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.5	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.6			
$V_{T+}—V_{T-}$	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA	
		54,74	2.0			V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−400	µA	V_{CC} = MAX, V_{OUT} = 4.0 V	
I_{IH}	Input HIGH Current	A or B, $\overline{GBA}$ or GAB			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		$\overline{GBA}$ or GAB			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		A or B			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current					mA	V_{CC} = MAX	
	Total Output HIGH				70			
	Total, Output LOW				90			
	Total at HIGH Z				95			

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A to B		8.0 11	15 15	ns	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay B to A		8.0 11	15 15	ns	
t_{PZL} t_{PZH}	Output Enable Time $\overline{GBA}$ to A		31 26	40 40	ns	
t_{PZL} t_{PZH}	Output Enable Time GAB to B		31 26	40 40	ns	
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{GBA}$ to A		15 15	25 25	ns	C_L = 5.0 pF
t_{PLZ} t_{PHZ}	Output Disable Time GAB to B		15 15	25 25	ns	

MOTOROLA

SN54/74LS640
SN54/74LS641
SN54/74LS642
SN54/74LS645

OCTAL BUS TRANSCEIVERS

LOW POWER SCHOTTKY

DESCRIPTION — These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

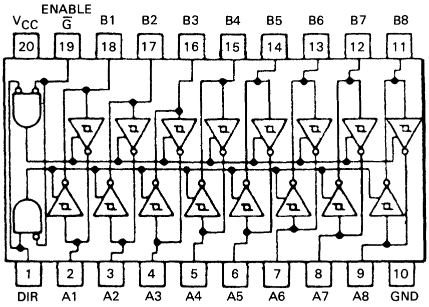
DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	LS640 LS642	LS641 LS645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

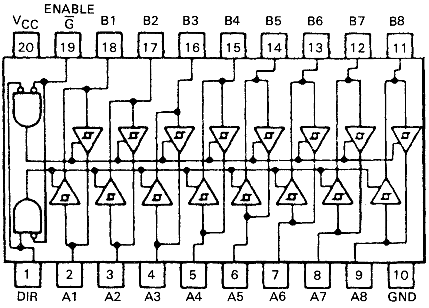
H = High level, L = low level, X = irrelevant

CONNECTION DIAGRAMS
(TOP VIEW)



ENABLE
VCC
G
B1
B2
B3
B4
B5
B6
B7
B8
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
DIR
A1
A2
A3
A4
A5
A6
A7
A8
GND

SN54/74LS640
SN54/74LS642



ENABLE
VCC
G
B1
B2
B3
B4
B5
B6
B7
B8
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
DIR
A1
A2
A3
A4
A5
A6
A7
A8
GND

SN54/74LS641
SN54/74LS645

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−3.0	mA
		54 74			−12 −15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.5	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.6		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA
		54,74	2.0			V	V_{CC} = MIN, I_{OH} = MAX
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V
I_{OZL}	Output Off Current LOW				−400	μA	V_{CC} = MAX, V_{OUT} = 0.4 V
I_{IH}	Input HIGH Current	A or B, DIR or $\overline{G}$			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
		DIR or $\overline{G}$			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
		A or B			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−40		−225	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total Output HIGH				70	mA	V_{CC} = MAX
	Total Output LOW				90		
	Total at HIGH Z				95		

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS640			LS645				
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A to B		6.0	10		8.0	15	ns	C_L = 45 pF, R_L = 667 Ω
t_{PHL}			8.0	15		11	15		
t_{PLH}	Propagation Delay, B to A		6.0	10		8.0	15	ns	
t_{PHL}			8.0	15		11	15		
t_{PZL}	Output Enable Time $\overline{G}$, DIR to A		31	40		31	40	ns	
t_{PZH}			23	40		26	40		
t_{PZL}	Output Enable Time $\overline{G}$, DIR to B		31	40		31	40	ns	
t_{PZH}			23	40		26	40		
t_{PLZ}	Output Disable Time $\overline{G}$, DIR to A		15	25		15	25	ns	C_L = 5.0 pF
t_{PHZ}			15	25		15	25		
t_{PLZ}	Output Disable Time $\overline{G}$, DIR to B		15	25		15	25	ns	
t_{PHZ}			15	25		15	25		

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54,74			5.5	V
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.5	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.6		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current	54,74			100	μA	V_{CC} = MIN, V_{OH} = MAX
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					−0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current Total, Output HIGH				70	mA	V_{CC} = MAX
	Total, Output LOW				90	mA	V_{CC} = MAX
	Total at HIGH Z				95	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS641			LS642				
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, B to A		17 16	25 25		19 14	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, DIR to A		23 34	40 50		26 43	40 60	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, DIR to B		25 37	40 50		28 39	40 60	ns	

SN54/74LS669

SYNCHRONOUS 4-BIT UP/DOWN COUNTER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS669 is a synchronous 4-bit up/down counter. The LS669 is a 4-bit binary counter. For high speed counting applications, this presettable counter features an internal carry lookahead for cascading purposes. By clocking all flip-flops simultaneously so the outputs change coincident with each other (when instructed to do so by the count enable inputs and internal gating) synchronous operation is provided. This helps to eliminate output counting spikes, normally associated with asynchronous (ripple-clock) counters. The four master-slave flip-flops are triggered on the rising (positive-going) edge of the clock waveform by a buffered clock input.

Circuitry of the load inputs allows loading with the carry-enable output of the cascaded counters. Because loading is synchronous, disabling of the counter by setting up a low level on the load input will cause the outputs to agree with the data inputs after the next clock pulse.

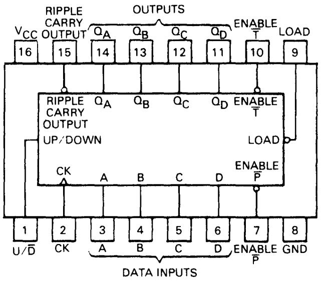
Cascading counters for N-bit synchronous applications are provided by the carry look-ahead circuitry, without additional gating. Two count-enable inputs and a carry output help accomplish this function. Count-enable inputs ($\overline{P}$ and $\overline{T}$) must both be low to count. The level of the up-down input determines the direction of the count. When the input level is low, the counter counts down, and when the input is high, the count is up. Input $\overline{T}$ is fed forward to enable the carry output. The carry output will now produce a low level output pulse with a duration ≈ equal to the high portion of the Q_A output when counting up and when counting down ≈ equal to the low portion of the Q_A output. This low level carry pulse may be utilized to enable successive cascaded stages. Regardless of the level of the clock input, transitions at the $\overline{P}$ or $\overline{T}$ inputs are allowed. By diode-clamping all inputs, transmission line effects are minimized which allows simplification of system design.

Any changes at control inputs (ENABLE $\overline{P}$, ENABLE $\overline{T}$, LOAD, UP/DOWN) will have no effect on the operating mode until clocking occurs because of the fully independant clock circuits. Whether enabled, disabled, loading or counting, the function of the counter is dictated entirely by the conditions meeting the stable setup and hold times.

PROGRAMMABLE LOOK-AHEAD UP/DOWN BINARY/DECADE COUNTERS

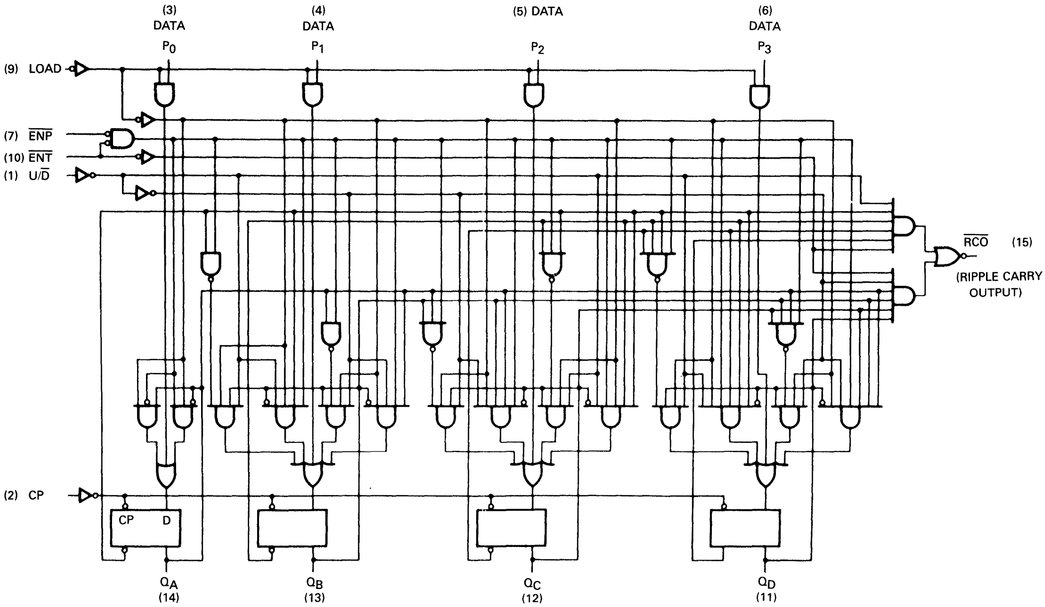
- **FULLY SYNCHRONOUS OPERATION FOR COUNTING AND PROGRAMMING**
- **INTERNAL LOOK-AHEAD FOR FAST COUNTING**
- **CARRY OUTPUT FOR n-BIT CASCADING**
- **FULLY INDEPENDENT CLOCK CIRCUIT**
- **BUFFERED OUTPUTS**

CONNECTION DIAGRAM
(TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

LOGIC DIAGRAM


(3) DATA P0
(4) DATA P1
(5) DATA P2
(6) DATA P3
(9) LOAD
(7) ENP
(10) ENT
(1) U/D
RCO (15)
(RIPPLE CARRY OUTPUT)
(2) CP
CP
D
QA (14)
QB (13)
QC (12)
QD (11)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	Others			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
		Enable T			40	µA	
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
		Enable T			0.2	mA	
I_{IL}	Input LOW Current	Others			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
		Enable T			−0.8	mA	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX

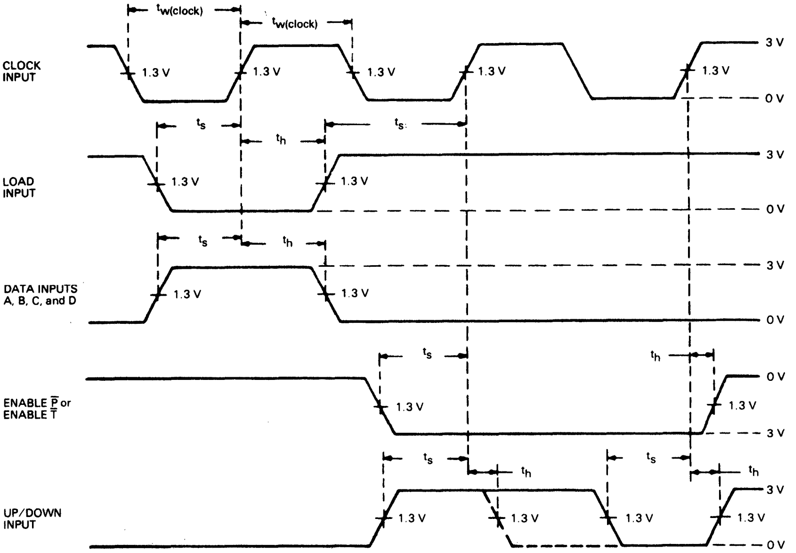
AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to $\overline{RCO}$		26 40	40 60	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Any Q		18 18	27 27	ns	
t_{PLH} t_{PHL}	Enable to $\overline{RCO}$		11 29	17 45	ns	
t_{PLH} t_{PHL}	U/$\overline{D}$ to $\overline{RCO}$		22 26	35 40	ns	

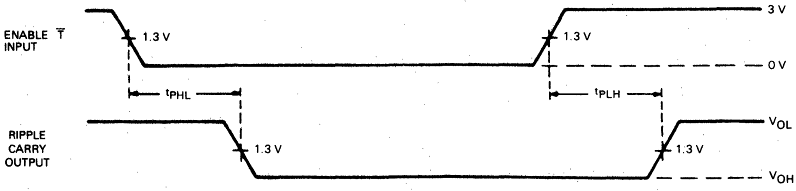
AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	20			ns	
t_s	Enable Setup Time	35			ns	
t_s	$\overline{Load}$ Setup Time	25			ns	
t_s	U/$\overline{D}$ Setup Time	30			ns	
t_h	Hold Time, Any Input	0			ns	

PARAMETER MEASUREMENT INFORMATION


t_w(clock)
t_w(clock)
CLOCK INPUT
1.3 V
1.3 V
1.3 V
1.3 V
1.3 V
3 V
0 V
t_s
t_h
t_s
LOAD INPUT
1.3 V
1.3 V
3 V
0 V
t_s
t_h
DATA INPUTS A, B, C, and D
1.3 V
1.3 V
3 V
0 V
t_s
t_h
ENABLE P̄ or ENABLE T̄
1.3 V
1.3 V
0 V
3 V
t_s
t_h
t_s
t_h
UP/DOWN INPUT
1.3 V
1.3 V
1.3 V
1.3 V
3 V
0 V

VOLTAGE WAVEFORMS


ENABLE T̄ INPUT
1.3 V
1.3 V
3 V
0 V
t_PHL
t_PLH
RIPPLE CARRY OUTPUT
1.3 V
1.3 V
V_OL
V_OH

MOTOROLA

SN54/74LS670

4 x 4 REGISTER FILE WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN54LS/74LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

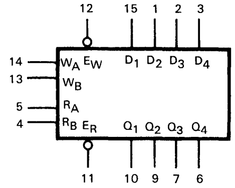
The SN54LS/74LS170 provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.5 U.L.	0.75 U.L.
Q_1-Q_4	Outputs (Note b)	65(25) U.L.	15(7.5) U.L.

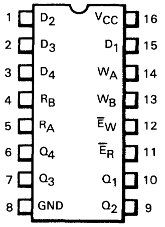
NOTES:
1. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

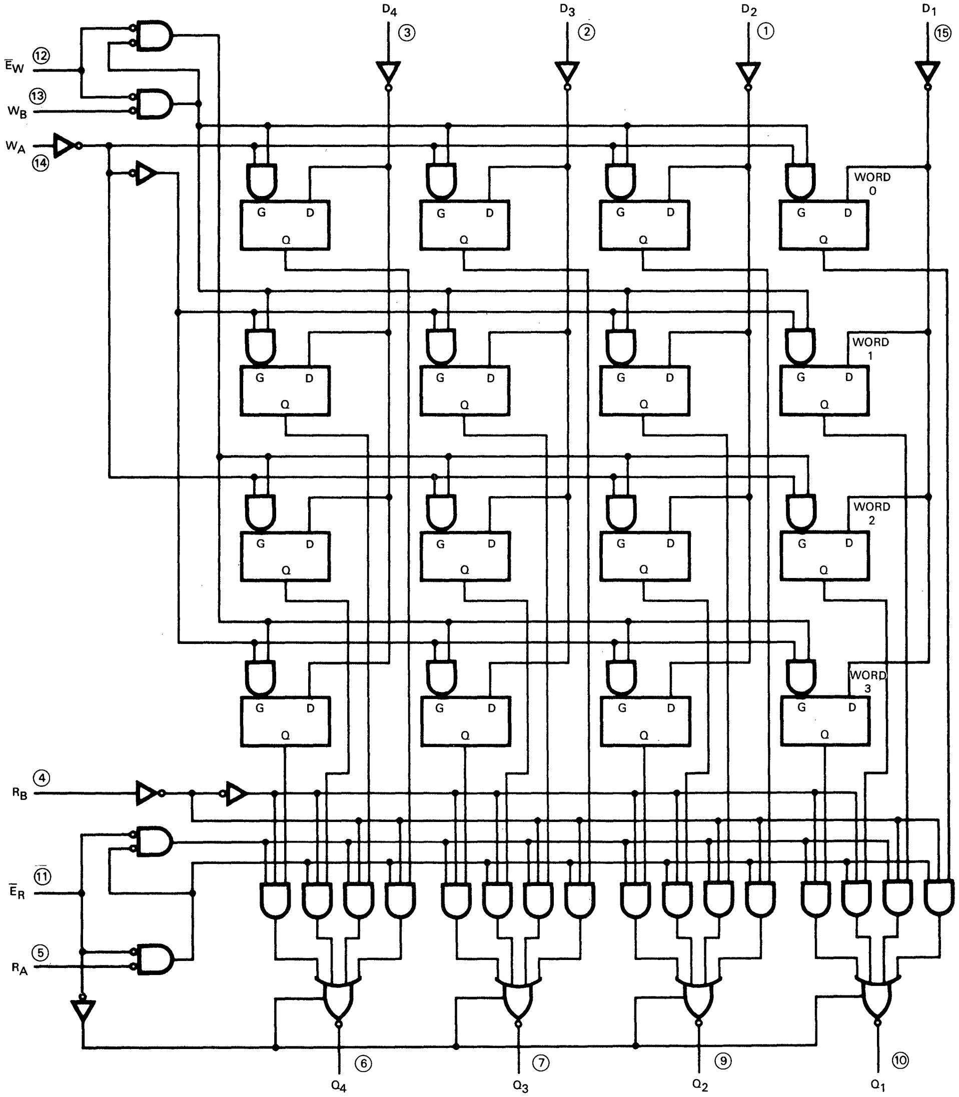
CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM


D4
③
D3
②
D2
①
D1
⑮
E̅W ⑫
WB ⑬
WA ⑭
WORD 0
WORD 1
WORD 2
WORD 3
G
D
Q
RB ④
E̅R ⑪
RA ⑤
⑥
Q4
⑦
Q3
⑨
Q2
⑩
Q1

○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	µA	V_{CC} = MAX, V_O = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	µA	V_{CC} = MAX, V_O = 0.4 V	
I_{IH}	Input HIGH Current D, R, W $\bar{E}_W$ $\bar{E}_R$				 20 40 60	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	D, R, W $\bar{E}_W$ $\bar{E}_R$				0.1 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current D, R, W $\bar{E}_W$ $\bar{E}_R$				 −0.4 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				50	mA	V_{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Output		23 25	40 45	ns	$V_{CC} = 5.0$ V $C_L = 45$ pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_W$ to Output		26 28	45 50	ns	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		25 23	45 40	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 22	35 40	ns	
t_{PLZ} t_{PHZ}	Output Disable Time		16 30	35 50	ns	$C_L = 5.0$ pF

AC SETUP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width	25			ns	$V_{CC} = 5.0$ V
t_s	Setup Time, (D)	10			ns	
t_s	Setup Time, (W)	15			ns	
t_h	Hold Time (D)	15			ns	
t_h	Hold Time (W)	5.0			ns	
t_{rec}	Recovery Time	25			ns	

AC WAVEFORMS

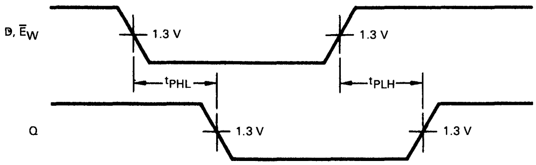

D, $\overline{E}_W$
1.3 V
1.3 V
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V

Fig. 1

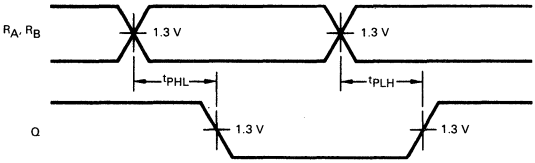

R_A, R_B
1.3 V
1.3 V
t_{PHL}
t_{PLH}
Q
1.3 V
1.3 V

Fig. 2

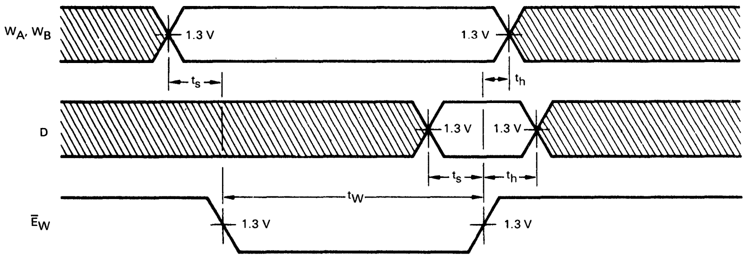

W_A, W_B
1.3 V
1.3 V
t_s
t_h
D
1.3 V
1.3 V
t_s
t_h
t_W
$\overline{E}_W$
1.3 V
1.3 V

Fig. 3

MOTOROLA

SN54/74LS682
SN54/74LS684
SN54/74LS688

8-BIT MAGNITUDE COMPARATORS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $\overline{P=Q}$ outputs and the LS682 and LS684 have $\overline{P>Q}$ outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 kΩ pullup resistor on the Q inputs for analog or switch data.

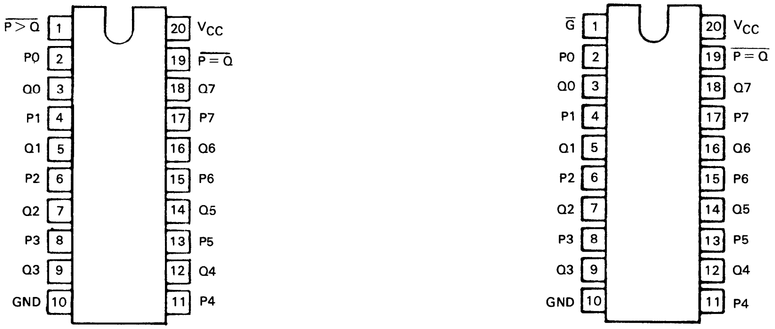
TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS683	yes	yes	no	open-collector	yes
LS684	yes	yes	no	totem-pole	no
LS685	yes	yes	no	open-collector	no
LS686	yes	yes	yes	totem-pole	no
LS687	yes	yes	yes	open-collector	no
LS688	yes	no	yes	totem-pole	no
LS689	yes	no	yes	open-collector	no

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{GT}$	$\overline{G2}$	$\overline{P=Q}$	$\overline{P>Q}$
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = high level, L = low level, X = irrelevant

CONNECTION DIAGRAMS
(TOP VIEW)


$\overline{P>Q}$ 1
P0 2
Q0 3
P1 4
Q1 5
P2 6
Q2 7
P3 8
Q3 9
GND 10
20 V_{CC}
19 $\overline{P=Q}$
18 Q7
17 P7
16 Q6
15 P6
14 Q5
13 P5
12 Q4
11 P4
$\overline{G}$ 1
P0 2
Q0 3
P1 4
Q1 5
P2 6
Q2 7
P3 8
Q3 9
GND 10
20 V_{CC}
19 $\overline{P=Q}$
18 Q7
17 P7
16 Q6
15 P6
14 Q5
13 P5
12 Q4
11 P4

SN54LS/74LS682/684

SN54LS/74LS688

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

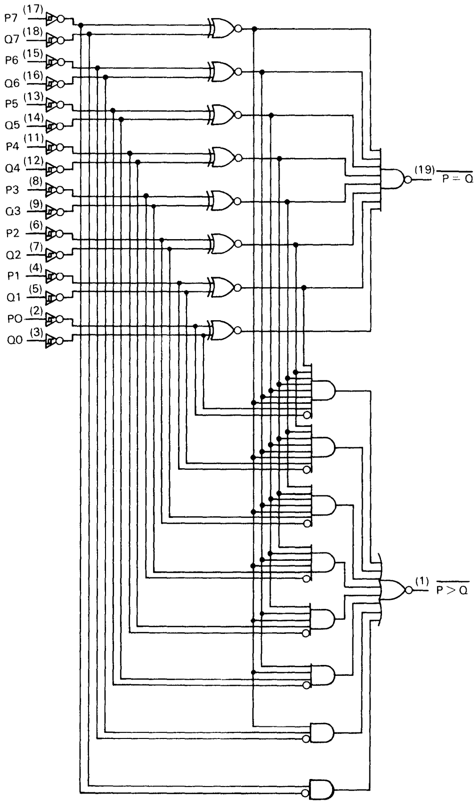
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

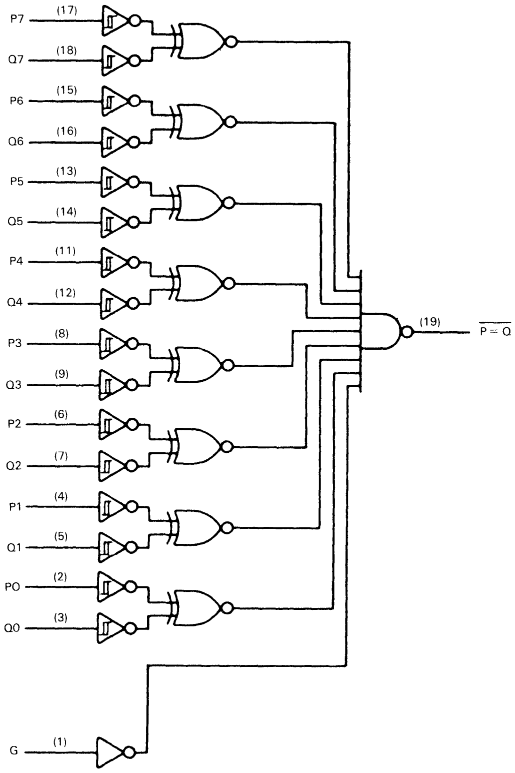
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		LS682-Q Inputs			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	LS682-Q Inputs			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Others			−0.2	mA		
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current	LS682			70	mA	V_{CC} = MAX	
		LS684			65	mA		
		LS688			65	mA		

LOGIC DIAGRAMS


P7 (17)
Q7 (18)
P6 (15)
Q6 (16)
P5 (13)
Q5 (14)
P4 (11)
Q4 (12)
P3 (8)
Q3 (9)
P2 (6)
Q2 (7)
P1 (4)
Q1 (5)
PO (2)
Q0 (3)
(19) $\overline{P = Q}$
(1) $\overline{P > Q}$

SN54LS/74LS682 thru LS684


P7 (17)
Q7 (18)
P6 (15)
Q6 (16)
P5 (13)
Q5 (14)
P4 (11)
Q4 (12)
P3 (8)
Q3 (9)
P2 (6)
Q2 (7)
P1 (4)
Q1 (5)
PO (2)
Q0 (3)
G (1)
(19) $\overline{P = Q}$

SN54LS/74LS688

AC CHARACTERISTICS: T_A = 25°C

SN54LS/74LS682

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		13 15	25 25	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		14 15	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P > Q}$		20 15	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P > Q}$		21 19	30 30	ns	

SN54LS/74LS684

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		15 17	25 25	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		16 15	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P > Q}$		22 17	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P > Q}$		24 20	30 30	ns	

SN54LS/74LS688

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		12 17	18 23	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		12 17	18 23	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P = Q}$		12 13	18 20	ns	

MOTOROLA

SN74LS783/
MC6883
SN74LS785

SYNCHRONOUS ADDRESS MULTIPLEXER

LOW POWER SCHOTTKY

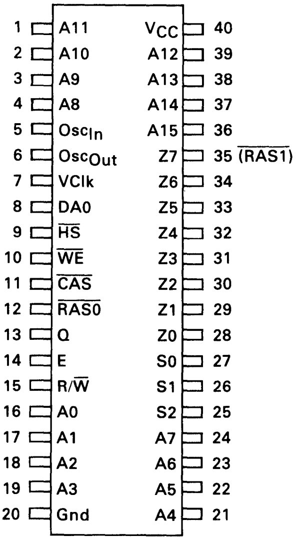
SYNCHRONOUS ADDRESS MULTIPLEXER

The SN74LS783/MC6883 and SN74LS785 bring together the MC6809E (MPU), the MC6847 (Color Video Display Generator) and dynamic RAM to form a highly effective, compact and cost effective computer and display system.

The SN74LS783/MC6883 is designed to support 4K x 1, 16K x 1 and 64K x 1 (128 column refresh) dynamic RAMs. The SN74LS785 has been modified to support the above listed products as well as 16K x 4 and 64K x 1 (256 column refresh) dynamic RAMs. A further enhancement allows the LS785 to support low power dynamic ROMs (such as MCM68364) without additional logic.

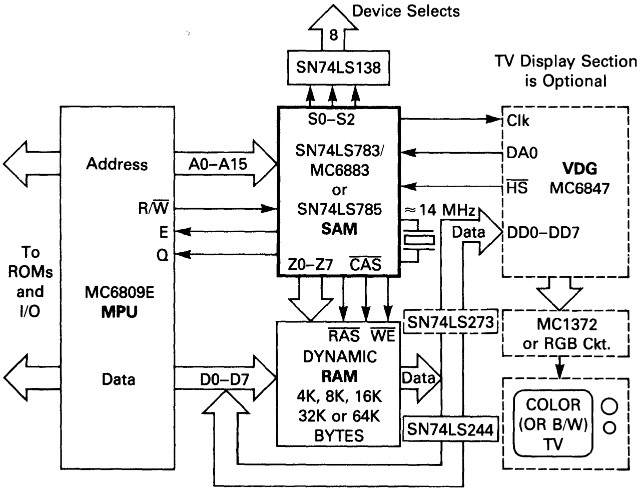
- MC6809E, MC6800, MC6801E, MC68000 and MC6847 (VDG) Compatible
- Transparent MPU/VDG/Refresh
- RAM size — 4K, 8K, 16K, 32K or 64K Bytes (Dynamic or Static)
- Addressing Range — 96K Bytes
- Single Crystal Provides All Timing
- Register Programmable:
  - VDG Addressing Modes
  - VDG Offset (0 to 64K)
  - RAM Size
  - Page Switch
  - MPU Rate (Crystal ÷ 16 or ÷ 8)
  - MPU Rate (Address Dependent or Independent)
- System "Device Selects" Decoded 'On Chip'
- Timing is Optimized for Standard Dynamic RAMs
- +5.0 V Only Operation
- Easy Synchronization of Multiple SAM Systems
- DMA Mode

PIN ASSIGNMENT



1 A11 VCC 40
2 A10 A12 39
3 A9 A13 38
4 A8 A14 37
5 OscIn A15 36
6 OscOut Z7 35 (RAS1)
7 VClk Z6 34
8 DA0 Z5 33
9 HS Z4 32
10 WE Z3 31
11 CAS Z2 30
12 RAS0 Z1 29
13 Q Z0 28
14 E S0 27
15 R/W S1 26
16 A0 S2 25
17 A1 A7 24
18 A2 A6 23
19 A3 A5 22
20 Gnd A4 21

TYPICAL SYSTEM BLOCK DIAGRAM



Device Selects
8
SN74LS138
TV Display Section is Optional
S0–S2
SN74LS783/ MC6883 or SN74LS785 SAM
Clk
DA0
HS
VDG MC6847
≈14 MHz
Data
DD0–DD7
Address
A0–A15
R/W
E
Q
To ROMs and I/O
MC6809E MPU
Z0–Z7
CAS
RAS
WE
DYNAMIC RAM 4K, 8K, 16K 32K or 64K BYTES
SN74LS273
MC1372 or RGB Ckt.
Data
D0–D7
Data
SN74LS244
COLOR (OR B/W) TV

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage (Except Osc_{In})	V_I	−0.5 to 10	Vdc
Input Current (Except Osc_{In})	I_I	−30 to +5.0	mA
Output Voltage	V_O	−0.5 to +7.0	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Input Voltage Osc_{In}	$V_{IOsc_{In}}$	−0.5 to V_{CC}	Vdc
Input Current Osc_{In}	$I_{IOsc_{In}}$	−0.5 to +5.0	mA

GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Operating Ambient Temperature Range	T_A	0	25	75	°C
Output Current High	I_{OH}				mA
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$		—	—	−1.0	
All Other Outputs		—	—	−0.2	
Output Current Low	I_{OL}				mA
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$		—	—	8.0	
VClk		—	—	0.8	
All Other Outputs		—	—	4.0	

DC CHARACTERISTICS (Unless otherwise noted specifications apply over recommended power supply and temperature ranges.)

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage — High Logic State	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	V
Input Clamp Voltage (V_{CC} = Min, I_{in} = −18 mA) All Inputs Except Osc_{In}	V_{IK}	—	—	−1.5	V
Input Current — High Logic State at Max Input Voltage	I_I				µA
(V_{CC} = Max, V_{in} = 5.25 V) VClk Input		—	—	200	
(V_{CC} = Max, V_{in} = 5.25 V) DA0 Input		—	—	100	
(V_{CC} = Max, V_{in} = 5.25 V Osc_{In} = Gnd) Osc_{Out} Input		—	—	250	
(V_{CC} = Max, V_{in} = 7.0 V) All Other Inputs Except Osc_{In}		—	—	100	
Input Current High Logic State All Inputs Except VClk, DA0 Osc_{In}, Osc_{Out} (V_{CC} = Max, V_{in} = 2.7 V)	I_{IH}	—	—	20	µA
Input Current — Low Logic State	I_{IL}				mA
(V_{CC} = Max, V_{in} = 0.4 V) DA0 Input		—	—	−1.2	
(V_{CC} = Max, V_{in} = 0.4 V) VClk Input		—	−30	−60	
(V_{CC} = Max, V_{in} = 0.4 V, Osc_{In} = Gnd) Osc_{Out} Input		—	—	−8	
(V_{CC} = Max, V_{in} = 0.4 V) All Other Inputs Except Osc_{In}		—	—	−.4	
Output Voltage — High Logic State					V
(V_{CC} = Min, I_{OH} = −1.0 mA) $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	$V_{OH(C)}$	3.0	—	—	
(V_{CC} = Min, I_{OH} = −0.2 mA) E, Q	$V_{OH(E)}$	V_{CC} − 0.75	—	—	
(V_{CC} = Min, I_{OH} = −0.2 mA) All Other Outputs	V_{OH}	2.7	—	—	
Output Voltage — Low Logic State					V
(V_{CC} = Min, I_{OL} = 8.0 mA) $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	$V_{OL(C)}$	—	—	0.5	
(V_{CC} = Min, I_{OL} = 4.0 mA) E, Q Outputs	$V_{OL(E)}$	—	—	0.5	
(V_{CC} = Min, I_{OL} = 0.8 mA) VClk Output	$V_{OL(V)}$	—	—	0.6	
(V_{CC} = Min, I_{OL} = 4.0 mA) All Other Outputs	V_{OL}	—	—	0.5	
Power Supply Current	I_{CC}	—	180	230	mA
Output Short-Circuit Current	I_{OS}	30	—	225	mA

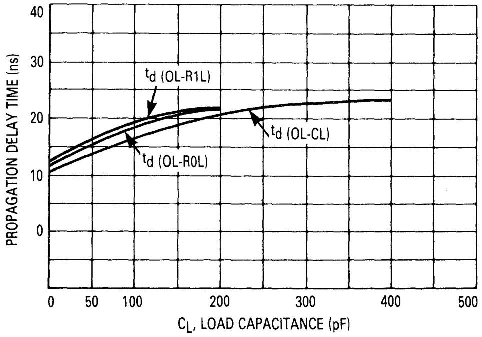
AC CHARACTERISTICS (4.75 V≤V_{CC}≤5.25 V and 0≤T_A≤70°C, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Units
Propagation Delay Times					ns
(See Circuit in Figure 9) Oscillator-In ↓ to Oscillator-Out ↑	$t_{d(OL-OH)}$	—	3.0	—	
Oscillator-In ↑ to Oscillator-Out ↓	$t_{d(OH-OL)}$	—	20	—	
(C_L = 195 pF) A0 thru A15 to Z0, Z1, Z2 thru Z7	$t_{d(A-Z)}$	—	28	—	
(C_L = 30 pF) A0 thru A15, R/W to S0, S1, S3	$t_{d(A-S)}$	—	18	—	
(C_L = 95 pF) Oscillator-Out ↓ to $\overline{RAS0}$ ↑	$t_{d(OL-R0H)}$	—	20	—	
(C_L = 95 pF) Oscillator-Out ↓ to $\overline{RAS0}$ ↓	$t_{d(OL-R0L)}$	—	18	—	
(C_L = 95 pF) Oscillator-Out ↓ to $\overline{RAS1}$ ↑	$t_{d(OL-R1H)}$	—	22	—	
(C_L = 95 pF) Oscillator-Out ↓ to $\overline{RAS1}$ ↓	$t_{d(OL-R1L)}$	—	20	—	
(C_L = 195 pF) Oscillator-Out ↓ to $\overline{CAS}$ ↑	$t_{d(OL-CH)}$	—	20	—	
(C_L = 195 pF) Oscillator-Out ↓ to $\overline{CAS}$ ↓	$t_{d(OL-CL)}$	—	20	—	
(C_L = 195 pF) Oscillator-Out ↓ to $\overline{WE}$ ↑	$t_{d(OL-WH)}$	—	22	—	
(C_L = 195 pF) Oscillator-Out ↓ to $\overline{WE}$ ↓	$t_{d(OL-WL)}$	—	40	—	
(C_L = 100 pF) Oscillator-Out ↓ to E ↑	$t_{d(OL-EH)}$	—	55	—	
(C_L = 100 pF) Oscillator-Out ↓ to E ↓	$t_{d(OL-EL)}$	—	25	—	
(C_L = 100 pF) Oscillator-Out ↓ to Q ↑	$t_{d(OL-QH)}$	—	55	—	
(C_L = 100 pF) Oscillator-Out ↓ to Q ↓	$t_{d(OL-QL)}$	—	25	—	
(C_L = 30 pF) Oscillator-Out ↑ to VClk ↑	$t_{d(OH-VH)}$	—	50	—	
(C_L = 30 pF) Oscillator-Out ↑ to VClk ↓	$t_{d(OH-VL)}$	—	65	—	
(C_L = 195 pF) Oscillator-Out ↓ to Row Address	$t_{d(OL-AR)}$	—	36	—	
(C_L = 195 pF) Oscillator-Out ↓ to Column Address	$t_{d(OL-AC)}$	—	33	—	
(C_L = 15 pF) Oscillator-Out ↓ to DA0 ↑ Earliest(1)	$t_{d(OL-DH)}$	—	−15	—	
(C_L = 15 pF) Oscillator-Out ↓ to DA0 ↑ Latest(1)	$t_{d(OL-DH)}$	—	+15	—	
(C_L = 95 pF on $\overline{RAS}$, C_L = 195 pF on $\overline{CAS}$) $\overline{CAS}$ ↓ to $\overline{RAS}$ ↑	$t_{d(CL-RH)}$	—	208	—	
Setup Time for A0 thru A15, R/$\overline{W}$ Rate = ÷16	$t_{su(A)}$	—	28	—	ns
Rate = ÷ 8		—	28		
Hold Time for A0 thru A15, R/$\overline{W}$ Rate = ÷16	$t_{h(A)}$	—	30	—	ns
Rate = ÷ 8		—	30	—	
Width of $\overline{HS}$ Low 2	$t_{WL(HS)}$	2.0	5.0	6.0	µs

Notes: 1. When using the SAM with an MC6847, the rising edge of DA0 is confined within the range shown in the timing diagrams (unless the synchronizing process is incomplete.) The synchronization process requires a maximum of 32 cycles of Osc_{Out} for completion.

2. $t_{WL(HS)}$ wider than 6.0 µs may yield more than 8 sequential refresh addresses.

FIGURE 1 — PROPAGATION DELAY TIMES versus LOAD CAPACITANCE



PIN DESCRIPTION TABLE

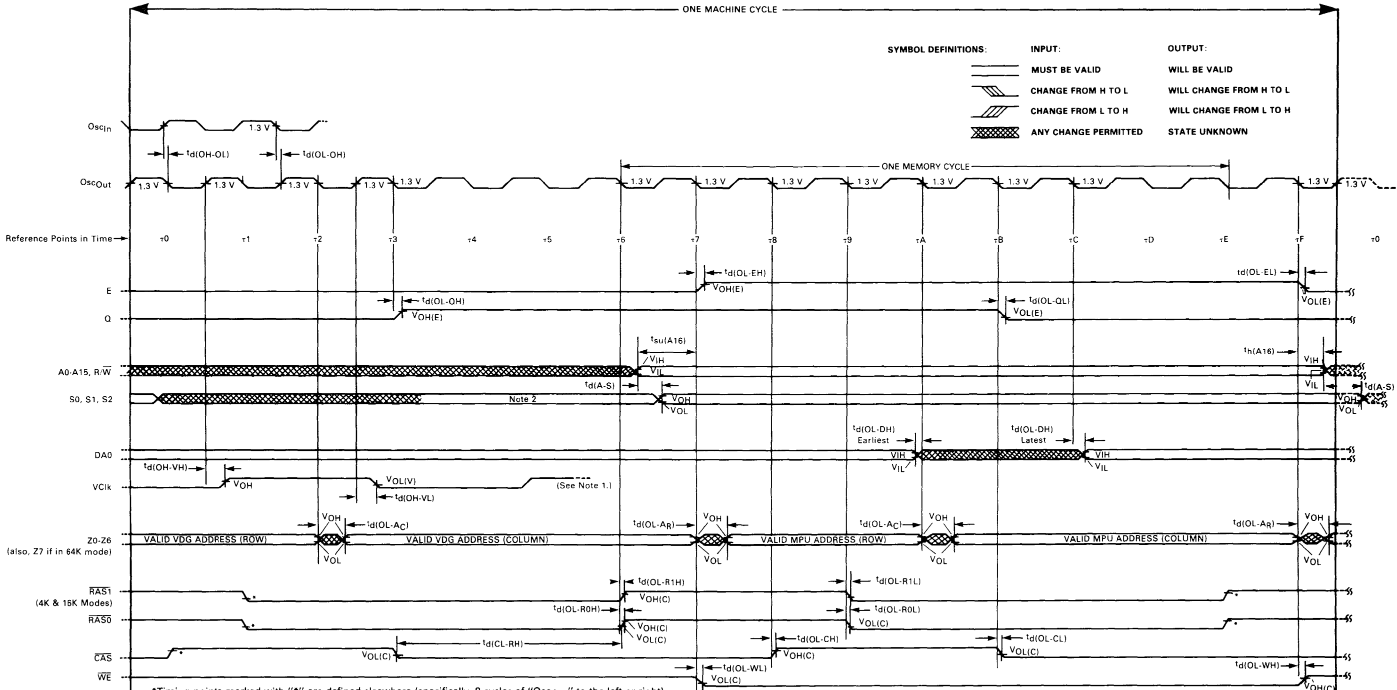
		Name	No.	Function
Input Pins	Power	V_{CC}	40	Apply + 5 volts ± 5%. SAM draws less than 230 mA.
		Gnd	20	Return Ground for +5 volts.
	MPU Address and Control	A15	36	Most Significant Bit.
		A14	37	
		A13	38	MPU address bits A0-A15. These 16 signals come directly from the MPU and are used to directly address up to 64K memory locations or to indirectly address up to 96K memory locations. (See pages 17 and 18 for memory maps). Each input is approximately equivalent to one low power Schottky load.
		A12	39	
		A11	1	
		A10	2	
		A9	3	
		A8	4	
		A7	24	
		A6	23	
		A5	22	
		A4	21	
		A3	19	
		A2	18	
		A1	17	
		A0	16	Least Significant Bit.
		$R/\overline{W}$	15	MPU READ or $\overline{\text{WRITE}}$. This signal comes directly from the MPU and is used to enable writing to the SAM control register, dynamic RAM (via $\overline{\text{WE}}$), and to enable device select #0.
		Osc$_{In}$	5	Apply 14.31818* MHz crystal and 2.5–30 pF trimmer to ground. See page 12.
	VDG Control	DA0	8	Display Address DA0. The primary function of this pin is to input the least significant bit of a 16-bit video display address. The more significant 15-bits are outputs from an internal 15-bit counter which is clocked by DA0. The secondary function of this pin is to indirectly input the logic level of the VDG "$\overline{\text{FS}}$" (field synchronization pulse) for vertical video address updating.
		$\overline{\text{HS}}$	9	Horizontal Synchronization. The primary function of this pin is to detect the falling edge of VDG "$\overline{\text{HS}}$" pulse in order to initiate eight dynamic RAM refresh cycles. The secondary function is to reset up to 4 least significant bits of the internal video address counter.
Output Pins		VClk	7	VDG Clock. The primary function of this pin is to **output** a 3.579545 MHz square wave** to the VDG "Clk" pin. The secondary function resets the SAM when this VClk pin is pulled to logic "0" level, acting as an **input**.
		Osc$_{Out}$	6	Apply 1.5 kΩ resistor to 14.31818* MHz crystal and 33 pF capacitor to ground. See page 12.
	Device Selects	S2	25	Most Significant Bit (Device Select Bits). The binary value of S2, S1, S0 selects one of eight "chunks" of MPU address space (numbers 0 through 7). Varying in length, these "chunks" provide efficient memory mapping for ROMs, RAMs, Input/Output devices, and MPU Vectors. (Requires 74LS 138-type demultiplexer).
		S1	26	
		S0	27	Least Significant Bit.
	MPU Clocks	E	14	E (Enable Clock) "E" and "Q" are 90° out of phase and are both used as MPU clocks for the MC6809E. For the MC6800 and MC6801E, only "E" is used. "E" is also used for many MC6800 peripheral chips.
		Q	13	Q (Quadrature Clock).
	RAM Address	Z7†	35	Most Significant Bit
		Z6†	34	First, the least significant address bits from the MPU or "VDG" are presented to Z0–Z5 (4K x 1 RAMs) or Z0–Z6 (16K x 1 RAMs) or Z0–Z7 (64K x 1 RAMs). Next, the most significant address bits from the MPU or "VDG" are presented to Z0–Z5 (4K x 1 RAMs) or Z0–Z6 (16K x 1 RAMs) or Z0–Z7 (64K x 1 RAMs). Note that for 4K x 1 and 16K x 1 RAMs, Z7 (Pin 35) is not needed for address information. Therefore, Pin 35 is used for a second row address select which is labeled ($\overline{\text{RAS1}}$).
		Z5†	33	
		Z4†	32	
		Z3†	31	
		Z2†	30	
		Z1†	29	
		Z0†	28	Least Significant Bit.
	RAM Control	$\overline{\text{RAS1}}$†	35	Row Address Strobe One. This pulse strobes the least significant 6,7 or 8 address bits into dynamic RAMs in Bank #1.
		$\overline{\text{RAS0}}$†	12	Row Address Strobe Zero. This pulse strobes the least significant 6,7 or 8 address bits into dynamic RAMs in Bank #0.
		$\overline{\text{CAS}}$†	11	Column Address Strobe. This pulse strobes the most significant 6,7 or 8 address bits into dynamic RAMs.
		$\overline{\text{WE}}$†	10	Write Enable. When low, this pulse enables the MPU to write into dynamic RAM.

*14.31818 MHz is 4 times 3.579545 MHz television color subcarrier. Other frequencies may be used. (See page 12.)

**When VDG and SAM are not yet synchronized the "square wave" will stretch (see page 10.)

† Due to fast transitions, ferrite beads in series with these outputs may be necessary to avoid high frequency (≈ 60 MHz) resonances.

FIGURE 2 — TIMING WAVEFORMS for MPU RATE = SLOW

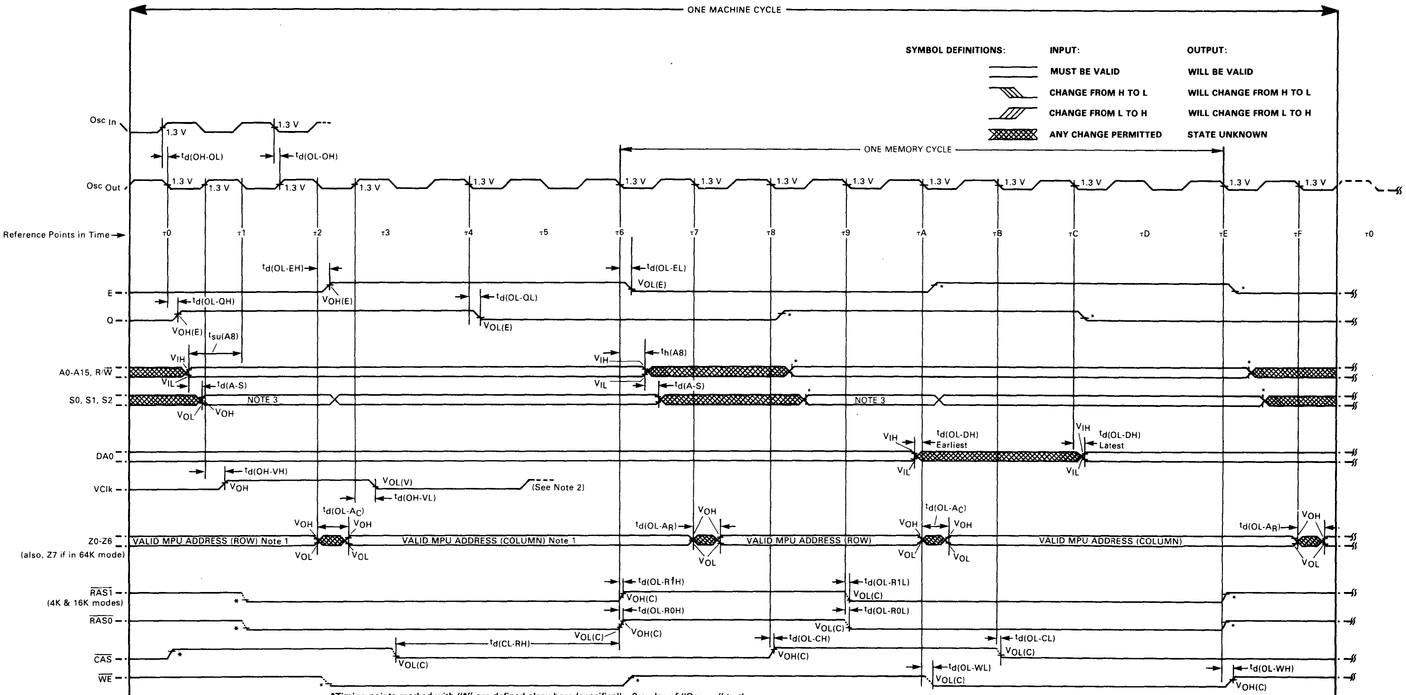

ONE MACHINE CYCLE
SYMBOL DEFINITIONS:
INPUT:
OUTPUT:
MUST BE VALID
WILL BE VALID
CHANGE FROM H TO L
WILL CHANGE FROM H TO L
CHANGE FROM L TO H
WILL CHANGE FROM L TO H
ANY CHANGE PERMITTED
STATE UNKNOWN
ONE MEMORY CYCLE
OscIn
OscOut
Reference Points in Time
E
Q
A0-A15, R/W̄
S0, S1, S2
DA0
VClk
Z0-Z6 (also, Z7 if in 64K mode)
RAS̄1 (4K & 16K Modes)
RAS̄0
CAS̄
WĒ
1.3 V
τ0
τ1
τ2
τ3
τ4
τ5
τ6
τ7
τ8
τ9
τA
τB
τC
τD
τE
τF
td(OH-OL)
td(OL-OH)
td(OL-EH)
td(OL-EL)
td(OL-QH)
td(OL-QL)
VOH(E)
VOL(E)
tsu(A16)
th(A16)
td(A-S)
VIH
VIL
VOH
VOL
Note 2
td(OL-DH) Earliest
td(OL-DH) Latest
td(OH-VH)
VOL(V)
td(OH-VL)
(See Note 1.)
td(OL-AC)
td(OL-AR)
VALID VDG ADDRESS (ROW)
VALID VDG ADDRESS (COLUMN)
VALID MPU ADDRESS (ROW)
VALID MPU ADDRESS (COLUMN)
td(OL-R1H)
td(OL-R0H)
td(OL-R1L)
td(OL-R0L)
VOH(C)
VOL(C)
td(CL-RH)
td(OL-CH)
td(OL-CL)
td(OL-WL)
td(OL-WH)

Timing points marked with "" are defined elsewhere (specifically, 8 cycles of "OscOut" to the left or right).

Notes 1: The period of "VClk" is four times that of "OscOut" unless the synchronization process is incomplete. Also, VClk may rise without $t_{d(OH-VH)}$ nanoseconds of τ0, τ1, τ2 . . . or τF.

2: To support Dynamic ROMs, the LS785 forces the S outputs HIGH (S = 7) during τ3 to τ7 if ROM is accessed (S = 1, 2, or 3) on the previous MPU memory cycle. Otherwise the S outputs are undefined during τ3 to τ6.

FIGURE 3 — TIMING WAVEFORMS for MPU RATE = FAST


ONE MACHINE CYCLE
SYMBOL DEFINITIONS:
INPUT:
OUTPUT:
MUST BE VALID
WILL BE VALID
CHANGE FROM H TO L
WILL CHANGE FROM H TO L
CHANGE FROM L TO H
WILL CHANGE FROM L TO H
ANY CHANGE PERMITTED
STATE UNKNOWN
ONE MEMORY CYCLE
Osc In
Osc Out
Reference Points in Time
E
Q
A0-A15, R/W
S0, S1, S2
DA0
VClk
Z0-Z6
(also, Z7 if in 64K mode)
RAS1
(4K & 16K modes)
RAS0
CAS
WE
1.3 V
τ0
τ1
τ2
τ3
τ4
τ5
τ6
τ7
τ8
τ9
τA
τB
τC
τD
τE
τF
td(OH-OL)
td(OL-OH)
td(OL-EH)
td(OL-QH)
td(OL-QL)
td(OL-EL)
VOH(E)
VOL(E)
tsu(A8)
th(A8)
VIH
VIL
td(A-S)
VOH
VOL
NOTE 3
td(OL-DH)
Earliest
Latest
td(OH-VH)
td(OH-VL)
VOL(V)
(See Note 2)
td(OL-AC)
td(OL-AR)
VALID MPU ADDRESS (ROW) Note 1
VALID MPU ADDRESS (COLUMN) Note 1
VALID MPU ADDRESS (ROW)
VALID MPU ADDRESS (COLUMN)
td(OL-R1H)
td(OL-R0H)
td(OL-R1L)
td(OL-R0L)
VOH(C)
VOL(C)
td(CL-RH)
td(OL-CH)
td(OL-CL)
td(OL-WL)
td(OL-WH)

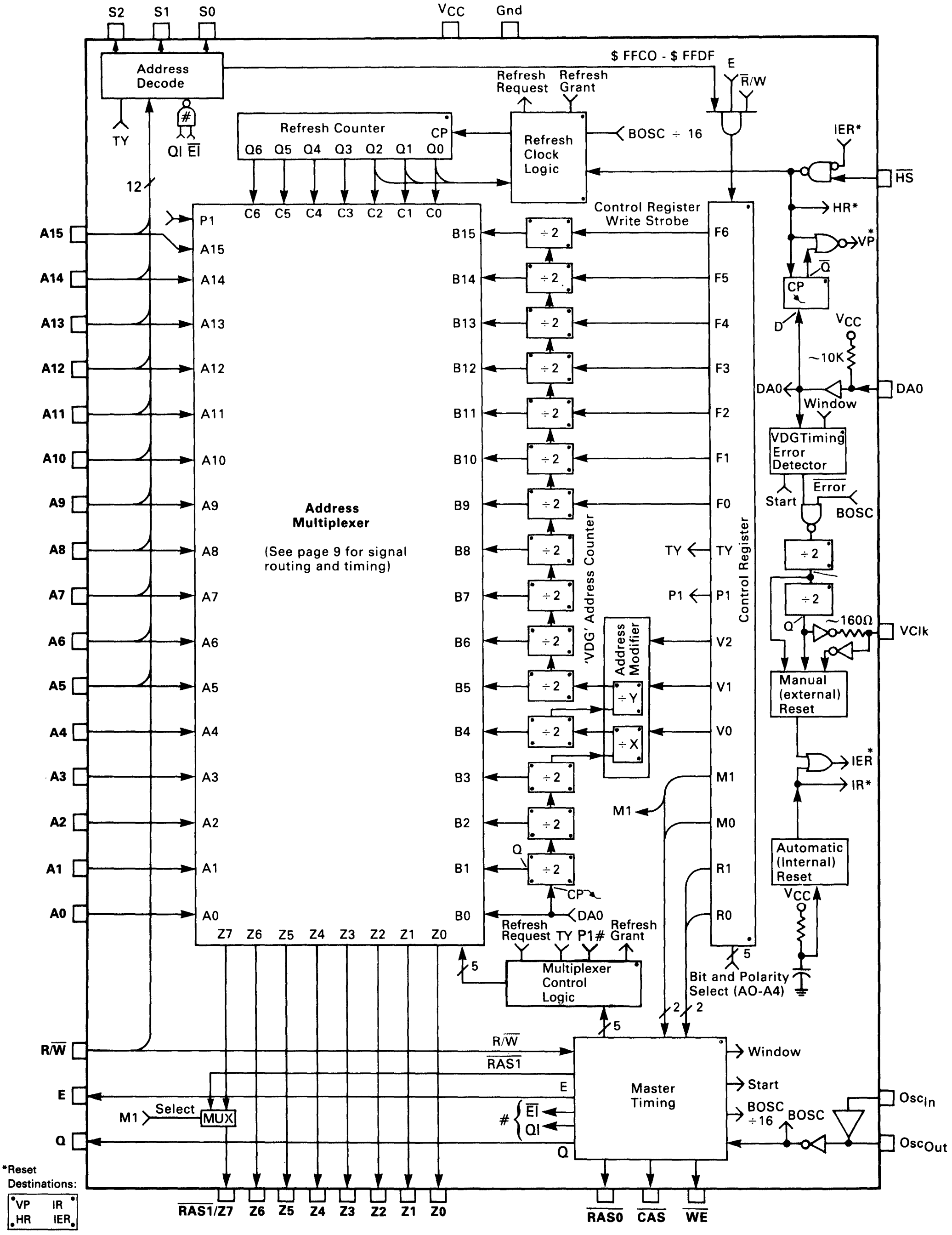
Timing points marked with "" are defined elsewhere (specifically, 8 cycles of "$\mathrm{Osc}_{\mathrm{Out}}$" to the left or the right).

Notes 1: In the "fast MPU rate" mode, the time slot otherwise used for a VDG address is used for a second MPU address.

2: The period of "VClk" is four times that of "$\mathrm{Osc}_{\mathrm{Out}}$" unless the synchronization process is incomplete. Also, VClk may rise within $t_{d(OH-VH)}$ nanoseconds of τ0, τ1, τ2 . . . or τF.

3: To support Dynamic ROMs, the LS785 forces the S outputs HIGH (S . . . 7) during τ0 to τ2 and τ8 to τA if ROM is accessed (S . . . 1, 2, or 3) on the previous MPU memory cycle. Otherwise the S outputs are decoded from the processor address bus during this time.

FIGURE 4 — SAM BLOCK DIAGRAM


S2
S1
S0
VCC
Gnd
Address Decode
$ FFCO - $ FFDF
E
R/W
Refresh Request
Refresh Grant
TY
#
QI EI
Refresh Counter
CP
Q6 Q5 Q4 Q3 Q2 Q1 Q0
Refresh Clock Logic
BOSC ÷ 16
IER*
HS
HR*
12
P1
C6 C5 C4 C3 C2 C1 C0
Control Register Write Strobe
VP*
Q
CP
D
VCC
~10K
DA0
DA0
Window
VDG Timing Error Detector
Start
Error
BOSC
÷2
÷2
~160Ω
Q
VClk
Manual (external) Reset
IER*
IR*
Automatic (Internal) Reset
VCC
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
Address Multiplexer
(See page 9 for signal routing and timing)
'VDG' Address Counter
Address Modifier
÷Y
÷X
Control Register
F6 F5 F4 F3 F2 F1 F0
TY
P1
V2 V1 V0
M1 M0
R1 R0
M1
Q
CP
DA0
Refresh Request TY P1# Refresh Grant
Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0
5
Multiplexer Control Logic
5
Bit and Polarity Select (A0-A4)
2
2
R/W
RAS1
E
Master Timing
Window
Start
BOSC ÷16
BOSC
OscIn
OscOut
M1
Select
MUX
# EI QI
Q
R/W
E
Q
*Reset Destinations:
VP IR
HR IER
RAS1/Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0
RAS0 CAS WE

Dots indicate which internal signals reset logic blocks

#These signals/logic not used by LS783

SAM BLOCK DIAGRAM DESCRIPTION

MPU Addresses (A0–A15):

These 16 signals come directly from the MPU and are used to directly address up to 64K memory locations (K = 1024) or to indirectly address up to 96K memory locations, by using a paging bit "P" (see pages 17 and 18 for memory maps). Each input is approximately equivalent to one low power Schottky load.

VDG Address Counter (B0–B15):

These 16 signals are derived from one input (DA0) which is the least significant bit of the VDG address. Most of the counter is simply binary. However, to duplicate the various addressing modes of the MC6847 VDG, ADDRESS MODIFIER logic is used. Selected by three VDG mode bits (V2, V1, and V0) from the SAM CONTROL REGISTER, eight address modifications are obtained as shown in Figure 5.

Also, notice that bits B9–B15 may be loaded from bits F0–F6 from the CONTROL REGISTER. This allows the starting address of the VDG display to be offset (in 1/2K increments) from $0000 to $FFFF†. B9–B15 are loaded when a VERTICAL PRE-LOAD (VP) pulse is generated. VP goes active (high) when $\overline{\text{HS}}$ from the VDG rises if DA0 is high (or a high impedance). This condition should occur only while the TV electron beam is in vertical blanking and is simply implemented by connecting $\overline{\text{FS}}$ and $\overline{\text{MS}}$ together on the MC6847. The VP pulse also **clears** bits B1–B8.

Finally, a HORIZONTAL RESET (HR) pulse may also affect the counter by clearing bits B1–B3 or B1–B4 when $\overline{\text{HS}}$ from the VDG is LOW (see Figure 5). The HR pulse should occur only while the TV electron beam is in horizontal blanking.

In summary, DA0 clocks the VDG ADDRESS COUNTER; HR initializes the horizontal portion and VP initializes the vertical portion of the VDG ADDRESS COUNTER.

REFresh Address Counter (Q0–Q7):

A seven bit binary counter (the LS785 uses an 8-bit counter) supplies bursts of eight* sequential addresses triggered by a $\overline{\text{HS}}$ high to low transition. Thus, while the TV electron beam is in horizontal blanking, eight sequential addresses are accessed. Likewise, the next eight addresses are accessed during the next horizontal blanking period, etc. In this manner, all 128 addresses are refreshed in less than 1.1 milliseconds.

Address Multiplexer:

Occupying a large portion of the block diagram in Figure 4, is the address multiplexer which outputs bits Z0–Z7 (as addresses to dynamic RAM's). Inputs to the address multiplexer include the VDG address (B0–B15) the REFresh address (C0–C6) and the MPU address (A0–A15) or (A0–A14 plus one paging bit "P"). The paging bit "P" is one bit in the SAM CONTROL REGISTER that is used in place of A15 when memory map TYpe #0 is selected (via the SAM CONTROL REGISTER "TY" bit).

Figure 6 shows which inputs are routed to Z0–Z7 and **when** the routing occurs relative to one SAM machine cycle. Notice that Z7 and $\overline{\text{RAS1}}$ share the same pin. Z7 is selected if "M1" in the SAM CONTROL REGISTER IS HIGH (Memory size = 64K).

Address Decode:

At the top left of Figure 4, is the Address Decode block. Outputs S2, S1, and S0 form a three bit encoded binary word(S). Thus S may be one of eight values (0 through 7) with each value representing a different range of MPU addresses. (To enable peripheral ROM's or I/O, decode the S2, S1, and S0 bits into eight separate signals by using a 74LS138, 74LS155 or 74LS156.)

On the LS783, the S2, S1 and S0 outputs are not gated with any timing signals. The LS785 forces the S outputs HIGH if accessing ROM (see Memory Map, Figures 14–16) when the E clock is LOW and the Q clock is HIGH (see Timing Diagram, Figures 2–3). This logic implementation allows the LS785 to easily interface with inexpensive "dynamic" ROMs such as MCM68364.

Along with the A5–A15 inputs is the MEMORY MAP TYpe bit (TY). This bit is soft-programmable (as are **all** 16 bits in the SAM CONTROL REGISTER), and selects one of two memory maps. Memory map #0 is intended to be used in systems that are primarily **ROM** based. Whereas, memory map #1 is intended for a primarily **RAM** based system with 64K contiguous RAM locations (minus 256 locations). The various meanings of S2, S1, S0 are tabulated in Figure 16 (page 19) and again on pages 17 and 18.

In addition to S2, S1, and S0 outputs is a decode of $FFC0 through $FFDF which, when gated with E and $\overline{\text{R}}$/W, results in the write strobe for the SAM CONTROL REGISTER.

SAM Control Register

As shown in Figure 4, the CONTROL REGISTER has 16 "outputs":

VDG Addressing Modes:	V2, V1, V0	MPU Rate:	R1, R0
VDG Address OFFset:	F6, F5, F4, F3, F2, F1, F0	Memory Size (RAM):	M1, M0
32K Page Switch:***	P	Memory Map TYpe:	TY

When the SAM is reset (see page 10), all 16 bits are cleared. To **set** any one of these 16 bits, the MPU simply **writes** to a unique** **odd** address (within $FFC1 through $FFDF). To **clear** any one of these 16 bits, the MPU simply writes to a unique** **even** address (within $FFC0 through $FFDE). Note that the **data** on the MPU data bus is irrevelant.

Inputs to the control register include A4, A3, A2, A1 (which are used to select **which one** of 16 bits is to be cleared or set), A0 (which determines the polarity . . . clear or set), and $\overline{\text{R}}$/W, E and $FFC0–$FFDF) (which restrict the method, timing and addresses for changing one of the 16 bits). For more detailed descriptions of the purposes of the 16 control bits, refer to related sections in the BLOCK DIAGRAM DESCRIPTION (pages 8 through 12) and the PROGRAMMING GUIDE (pages 14 through 18).

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* If $\overline{\text{HS}}$ is held low longer than 8 μs, then the number of sequential addresses in one refresh "BURST" is proportional to the time interval during which $\overline{\text{HS}}$ is low.

** See pages 17 or 18 for specific addresses.

*** The P bit is also used to select 16K x 4 bit dynamic RAM operation in the LS785. See the Page switch definition in the Programming Guide section.

† In this document, the "$" symbol always preceeds hexidecimal characters.

** See pages 17 or 18 for specific addresses.

FIGURE 5 — VDG ADDRESS MODIFIER

Mode			Division Variables		Bits Cleared by HS (low)
V2	V1	V0	X	Y	
0	0	0	1	12	B1–B4
0	0	1	3	1	B1–B3
0	1	0	1	3	B1–B4
0	1	1	2	1	B1–B3
1	0	0	1	2	B1–B4
1	0	1	1	1	B1–B3
1	1	0	1	1	B1–B4
1	1	1	1	1	None (DMA MODE)

FIGURE 6 — SIGNAL ROUTING for ADDRESS MULTIPLEXER

Memory Size			Signal	Row/Column	Signals Routed to Z0–Z7								Timing
	M1	M0	Source		Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0	(Figure 2)
4K ①	**0**	**0**	MPU	ROW	②	A6	A5	A4	A3	A2	A1	A0	T7–TA
				COL	②	LOW	A11	A10	A9	A8	A7	A6	TA–TF
			VDG	ROW	②	B6	B5	B4	B3	B2	B1	B0	TF–T2
				COL	②	LOW	B11	B10	B9	B8	B7	B6	T2–T7
			REF	ROW	②	C6	C5	C4	C3	C2	C1	C0	TF–T2
				COL	②	LOW	LOW	LOW	LOW	LOW	LOW	LOW	T2–T7
16K x 1	**0**	**1**	MPU	ROW	②	A6	A5	A4	A3	A2	A1	A0	T7–TA
				COL	②	A13	A12	A11	A10	A9	A8	A7	TA–TF
			VDG	ROW	②	B6	B5	B4	B3	B2	B1	B0	TF–T2
				COL	②	B13	B12	B11	B10	B9	B8	B7	T2–T7
			REF	ROW	②	C6	C5	C4	C3	C2	C1	C0	TF–T2
				COL	②	LOW	LOW	LOW	LOW	LOW	LOW	LOW	T2–T7
16K x 4	**0**	**1**	MPU	ROW	A7	A6	A5	A4	A3	A2	A1	A0	T7–TA
(Page bit = 1)				COL	③	A13	A12	A11	A10	A9	A8	A7	TA–TF
			VDG	ROW	B7	B6	B5	B4	B3	B2	B1	B0	TF–T2
This mode				COL	③	B13	B12	B11	B10	B9	B8	B7	T2–T7
only available			REF	ROW	C7	C6	C5	C4	C3	C2	C1	C0	TF–T2
with LS785				COL	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	T2–T7
64K (dynamic)			MPU	ROW	A7	A6	A5	A4	A3	A2	A1	A0	T7–TA
	1	**0**		COL	P/A15③	A14	A13	A12	A11	A10	A9	A8	TA–TF
			VDG	ROW	B7	B6	B5	B4	B3	B2	B1	B0	TF–T2
				COL	B15	B14	B13	B12	B11	B10	B9	B8	T2–T7
			REF	ROW	C7④	C6	C5	C4	C3	C2	C1	C0	TF–T2
				COL	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	T2–T2
64K (static)			MPU	ROW	A7	A6	A5	A4	A3	A2	A1	A0	T7–T9
	1	**1**		COL	P/A15③	A14	A13	A12	A11	A10	A9	A8	T9–TF
			VDG	ROW	B7	B6	B5	B4	B3	B2	B1	B0	TF–T1
				COL	B15	B14	B13	B12	B11	B10	B9	B8	T1–T7
			REF	ROW	C7④	C6	C5	C4	C3	C2	C1	C0	TF–T1
				COL	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	T1–T7

① When using 4K x 1 RAMs, two banks of eight IC's are allowed. This accounts for Addresses $0000–1FFF. Also, this same RAM can be addressed at $2000–$3FFF, $4000–$5FFF and $6000–$7FFF.

② Z7 functions as $\overline{\text{RAS1}}$ and its level is address dependent. For example, when using two banks of 16K x 1 RAMs, $\overline{\text{RAS0}}$ is active for addresses $0000 to $3FFF and $\overline{\text{RAS1}}$ is active for addresses $4000 to $7FFF.

③ If Map TYpe = 0, then page bit "P" is the output (otherwise A15). This is a "don't care" situation for 16K x 4 MOS RAM inputs.

④ C7 = Low on LS783.

Internal Reset

By lowering V_{CC} below 0.6 volts for at least one millisecond, a **complete** SAM reset is initiated and is completed within 500 nanoseconds after V_{CC} rises above 4.25 volts.

NOTE: In some applications, (for example, multiple "VDG-RAM" systems controlled by a single MPU) **multiple** SAM ICs can be synchronized as follows:

- Drive all SAM's from one external oscillator.
- Stop external oscillator.
- Lower V_{CC} below 0.6 volts for at least 1.0 millisecond.
- Raise V_{CC} to 5.0 volts.
- Start external oscillator.
- Wait at least 500 nanoseconds.

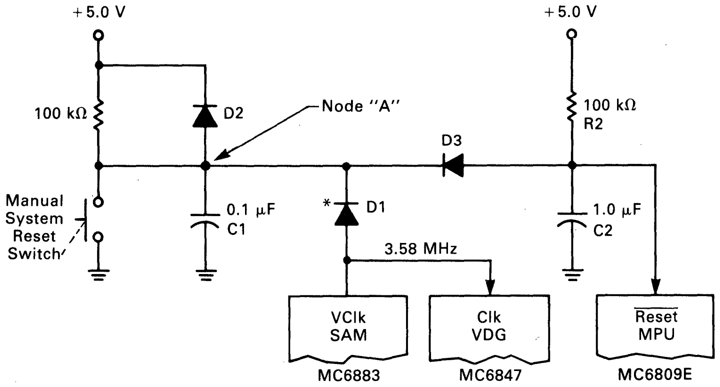
Now, the "E" clocks from all SAM's should be in-phase.

External Reset

When the VClk pin on SAM is forced below 0.8 volts for at least eight cycles of "oscillator-out", the SAM becomes **partially** reset. That is, all bits in the SAM control register are cleared. However, signals such as $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, E or Q are **not** stopped (as they are with an **internal** reset), since the SAM must maintain dynamic RAM refresh even during this external reset period.

Figure 7 shows how VClk can be pulled low through diode D1 when node "A" is low.* When node "A" is high, only the backbiased capacitance of diode D1 loads the 3.58 MHz on VClk. Diode D2 helps discharge C1 (Power-on-Reset capacitor) when power is turned off. Diode D3 allows the MPU reset time constant R2C2 to be greater than the SAM reset time constant. Thereby, ensuring **release** of the SAM reset **prior to** attempting to program the SAM control register.

FIGURE 7 — EXTERNAL RESET CIRCUITRY



VDG Synchronization

In order for the VDG and MPU to share the same dynamic RAM (see page 13,) the **VDG clock must be stopped** until the VDG data fetch and MPU data fetch are synchronized as shown in Figure 12. Once synchronized, the VDG clock resumes its 3.579545 MHz rate and is not stopped again unless an extreme temperature change (or SAM reset) occurs. When stopped, the VDG clock remains stopped for **no more than** 32 Osc$_{Out}$ cycles (approximately 2 microseconds.)

In the block diagram in Figure 4, DA0 enters a block labeled VDG Timing Error Detector. If DA0 rises **between** time reference points** τ_A and τ_C, then $\overline{\text{Error}}$ is high and VClk is the result of dividing BOSC (Buffered Osc$_{Out}$ ≈ 14 MHz) by four. However, if DA0 rises **outside** the time Window τ_A to τ_C, then $\overline{\text{Error}}$ goes LOW and the VDG stops. A START pulse at time reference point τ_B (center of Window) restarts the VDG . . . properly synchronized.

---

*Use a diode with sufficiently low forward voltage drop to meet V_{IL} requirement at VClk.

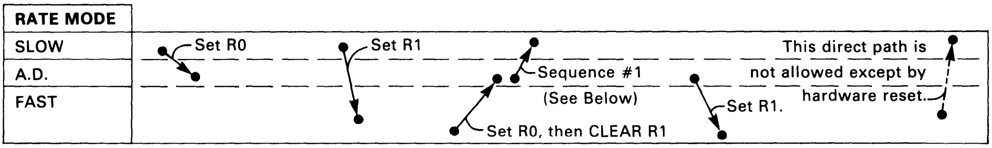
**See timing diagrams on page 5 and 6.

Changing the MPU Rate (by changing SAM control register bits R0, R1).

Two bits in the SAM control register determine the period of both "E" and "Q" MPU clocks. Three rate modes are implemented as follows:

RATE MODE	R1	R0	
SLOW	0	0	The frequency of "E" (and "Q") is f crystal ÷ 16. This rate mode is automatically selected when the SAM is reset. Note that system timing is least critical in this "SLOW" rate mode.
A.D. (Address Dependent)	0	1	The frequency of "E" (and "Q") is either f crystal ÷ 16 or f crystal ÷ 8, depending on the address the MPU is presenting.
FAST	1	X	The frequency of "E" (and "Q") is f crystal ÷ 8. This is accomplished by stealing the time that is normally used for VDG/REFRESH, and using this time for the MPU. Note: Neither VDG display nor dynamic RAM refresh are available in the "FAST" rate mode. (Both are available in SLOW and A.D. rate modes).

When changing between any two of the three rate modes, the following procedures must be followed to ensure that MPU timing specifications are met:



$$\underbrace{\text{May be ANY address from \$0000 to \$7FFF.}}$$

SEQUENCE #1:

```
7D 00 00 TST #$0000 . . . Synchronizes STA instruction to write during T2-TG (See Figure #8).*
21 00    BRN 00
B7 FF D6 STA #$FFD6 . . . Clears bit R0
```

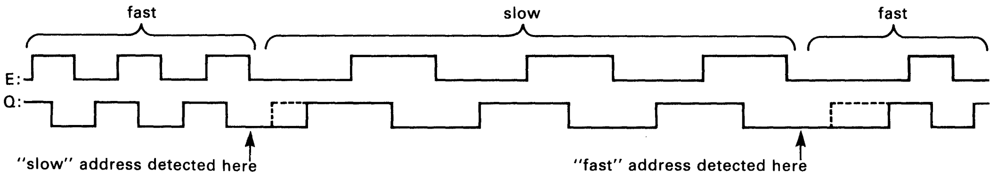
*Note: "TST" instruction affects MC6809E condition code register.

Changing the MPU Rate (In Address Dependent Mode)

When the SAM control register bits "R1", and "R0" are programmed to "0" and "1", respectively, the Address Dependent Rate Mode is selected. In this mode, the ÷ 16 MPU rate is automatically used when addressing within $0000 to $7FFF* or $FF00 to $FF1F ranges. Otherwise the ÷ 8 MPU rate is automatically used. (Refer to Figure 8 for sample "E" and "Q" waveforms yielding ÷ 8 to ÷ 16 and ÷ 16 to ÷ 8 rate changes). This mode often nearly doubles the MPU throughput while still providing transparent VDG and dynamic, RAM refresh functions. For example, since much of the MPU's time may be spent performing internal MPU functions (address = $FFFF)**, accessing ROM (address = $8000 to $FEFF) or accessing I/O (address = $FF20 — $FF5F), the faster f crystal ÷ 8 MPU rate may be used much of the time.

Note: The VDG operates normally when using the SLOW or A.D. rate modes. However, in the FAST rate mode, the VDG is not allowed access to the dynamic RAM.

FIGURE 8 — RATE CHANGE E AND Q WAVEFORMS

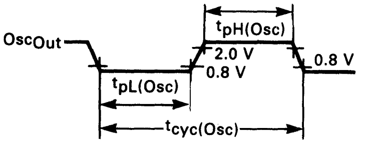


---

*When using Memory Map 0, addresses $0000 to $7FFF may access Dynamic RAM.
**The MC6809 outputs $FFFF on A0–A15 when no other valid addresses are being presented.

Oscillator

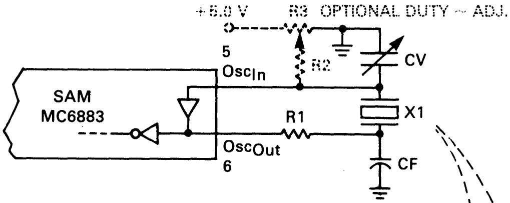
In Figure 4, an amplifier between Osc_{In} and Osc_{Out} provides the gain for oscillation (using a crystal as shown in Figure 9.) Alternately, Pin 5 (Osc_{In}) may be grounded while Pin 6 (Osc_{Out}) may be driven at low-power Schottky levels as shown in Figure 10. Also, see V_{IH}, V_{IL} on page 2.


OscOut
tpH(Osc)
2.0 V
0.8 V
0.8 V
tpL(Osc)
tcyc(Osc)

AC Specifications*

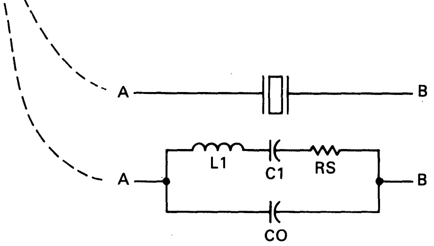
	Max	Typ	Min	Units
$t_{pH(Osc)}$	—	30	22	ns
$t_{pL(Osc)}$	—	30	22	ns
$t_{cyc(Osc)}$	—	70	62.4	.ns

FIGURE 9 — CRYSTAL OSCILLATOR


+5.0 V
R3 OPTIONAL DUTY ~ ADJ.
5
OscIn
R2
CV
SAM
MC6883
R1
X1
OscOut
6
CF

Suggested Component Values

Freq. MHz	CV*	CF*	R1*	R2*	R3*	X1
14.31818	2.5–30 pF	33 pF	1.5 kΩ	~ 100K	10K	*
16.0000	2.5–30 pF	33 pF	1.5 kΩ	~ 100K	10K	*

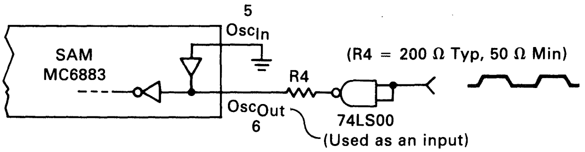

A
B
A
L1
C1
RS
B
CO

Recommended Crystal Parameters

	14.31818 MHz**	16.0000 MHz**
R_S	10 Ω ± 2.0 Ω	10 Ω ± 2.0 Ω
CO	5.0 pF ± 1.5 pF	6.0 pF ± 1.0 pF
C1	0.0245 pF ± 15%	0.0319 pF ± 15%
L1	5.05 mH	3.1 mH
Q	50K ± 10K	40K ± 10K

Calibration Tolerance: 0.002% at 26°C
Temperature Tolerance: 0.001% 0°C to 70°C

FIGURE 10 — TTL CLOCK INPUT


5
OscIn
SAM
MC6883
(R4 = 200 Ω Typ, 50 Ω Min)
R4
OscOut
6
74LS00
(Used as an input)

Typical input capacitances are 3.0 pF for Pin 5 and 5.5 pF for Pin 6.

*Optimum values depend on characteristics of the crystal (X1). For many applications, VClk must be 3.579545 MHz ± 50 Hz! Hence, Osc_{Out} must be made similarly "drift resistant" (by balancing temperature coefficients of X1, CV, CF, R1, R2 and R3).

**Specifically cut for the SAM are International Crystal Manufacturing, Inc. Crystals (#167568 for 14.31818 MHz or #167569 for 16.0 MHz). However, other crystals may be used.

THEORY OF OPERATION

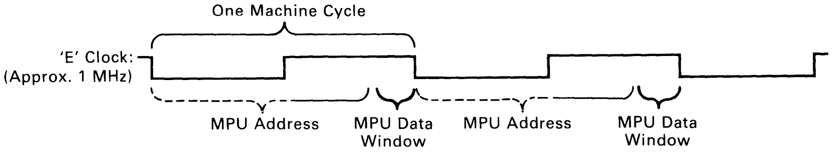
Video or No Video

Although the SAM may be used as a dynamic RAM controller **without** a video display*, most applications are likely to include a MC6847 video display generator (VDG). Therefore, this document emphasizes use of the SAM with MC6847 systems.

Shared RAM (with interleaved DMA)

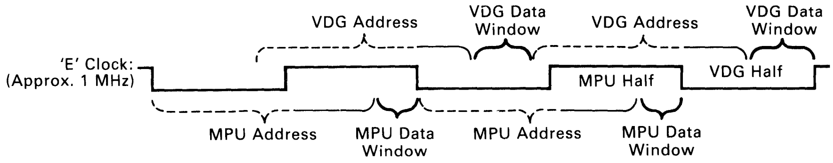
To minimize the number of RAM and interface chips, both the MPU and VDG share common dynamic RAM. Yet, the use of common RAM creates an apparent difficulty. That is, the MPU and VDG must both access the RAM without contention. This difficulty is overcome by taking advantage of the timing and architecture of Motorola MPU's (MC6800, MC6801E, MC6809E, MC68000). Specifically, **all** MPU accesses of external memory **always** occur in the **latter half** of the machine cycle, as shown below:

FIGURE 11 — MOTOROLA MPU TIMING



Similarly, the MC6847 (non-interlaced) VDG transfers a data byte in a half machine cycle (E or Φ2). Thus, when properly positioned, VDG and MPU RAM accesses interleave without contention as shown below:

FIGURE 12 — MOTOROLA MPU WITH VDG TIMING



This Interleaved Direct Memory Access (IDMA) is synchronized via the MC6883 by centering the VDG data window half-way between MPU data windows.**

The result is a shared RAM system without MPU/VDG RAM access contention, with both MPU and VDG running uninterrupted at normal operating speed, each transparent to the other.

RAM Refresh

Dynamic RAM refresh is accomplished by accessing eight*** sequential row addresses every 64*** microseconds until all addresses have been accessed. To avoid RAM access contention between REFRESH and MPU, each of the refresh accesses occupies the "VDG half" of the interleaved DMA (IDMA). Furthermore, refresh accesses occur only during the television retrace period (at which time the VDG doesn't need to access RAM).

In summary, the VDG, MPU and SAM's Refresh Counter all transparently access the common dynamic RAM without contention or interruption.

Why IDMA?

Use of the interleaved direct memory access results in fast modification to variable portions of display RAM, by the MPU, without any distracting flashes on the screen (due to RAM access contention). In addition, the MPU is not slowed down nor stopped by the SAM; thereby, assuring accurate software timing loops without costly additional hardware timers. Furthermore, additional hardware and software to give "access permission" to the MPU is eliminated since the MPU may access RAM at **any** time.

---

*Only 1 pin, (DA0) out of 40 pins is dedicated to the video display.

**See VDG synchronization (page 10) for more detail.

***When not using a MC6847, $\overline{HS}$ may be wired low for continuous transparent refresh.

"Systems On Silicon" Concept

Total Timing

For most applications, the SAM can supply complete system timing from its on-chip precision 14.31818 MHz oscillator. This includes buffered MPU clocks (E and Q), VDG clock, color subcarrier (3.58 MHz), row address select ($\overline{\text{RAS}}$), column address select ($\overline{\text{CAS}}$) and write enable ($\overline{\text{WE}}$).

Total Address Decode

For most applications, the SAM plus a "1 of 8 decoder" chip completely decodes I/O, ROM and RAM chip selects without wasting memory address space and without needlessly chopping-up contiguous address space. Chip selects are positioned in address space to allow three types of memory (RAM, local ROM and cartridge ROM) independent room for growth. For example, RAM may grow from address $0000-up, cartridge ROM may grow from address $FEFF-down and local ROM may grow from $BFFF-down. Alternately, if the application requires minimum ROM and maximum contiguous RAM, a second choice of two memory maps places RAM from $0000 to $FEFF. (See Figures 14–16.)

In both memory maps all I/O, MPU vectors, SAM control registers, and some reserved address spaces are efficiently contained between addresses $FF00 and $FFFF.

How Much RAM?

Using nine SAM pins (Z0–Z7 and $\overline{\text{RAS0}}$) the following combinations require no additional address logic.

FIGURE 13 — RAM CONFIGURATIONS

Address: MSB LSB	Chip Select:	
Z5Z4Z3Z2Z1Z0	$\overline{\text{RAS0}}$	One or two banks of 4K x 8 (like MCM4027's)
Z5Z4Z3Z2Z1Z0	$\overline{\text{RAS1}}$ (=Z7)	
Z6Z5Z4Z3Z2Z1Z0	$\overline{\text{RAS0}}$	One or two banks of 16K x 8 (like MCM4116's)
Z6Z5Z4Z3Z2Z1Z0	$\overline{\text{RAS1}}$ (=Z7)	
Z7Z6Z5Z4Z3Z2Z1Z0	$\overline{\text{RAS0}}$	One bank of 64K x 8 (like MCM6665's) or one bank of 16K x 4 (like TMS4416's)

PROGRAMMING GUIDE

SAM — Programmability

The SAM contains a 16-bit control register which allows the MC6809E to program the SAM for the following options:

VDG Addressing Mode	3-bits
VDG Address Offset	7-bits
32K Page Switch	1-bit
MPU Rate	2-bits
Memory Size	2-bits
Map Type	1-bit

Note that when the SAM is **reset** by first applying power or by manual hardware reset,† all control register bits are **cleared** (to a logic "0").

VDG Addressing Mode

Three bits (V2, V1, V0) control the sequence of DISPLAY ADDRESSES generated by the SAM (which are used to scan dynamic RAM for video information). For example, if you wish to display Dynamic RAM data as INTERNAL ALPHANUMERICS VIDEO, you should program‡ the MC6847 for the INTERNAL ALPHANUMERICS MODE **and** CLEAR BITS V2, V1 and V0 in the SAM. The table on the following page summarizes the available modes:

† See Figure 7 for manual reset circuit.

‡ Typically, part of a PIA (MC6821) at location $FF22 is used to control MC6847 modes. (See MC6847 Data Sheet.)

Mode Type	MC6847 Mode					SAM Mode		
	G/$\overline{A}$	GM2‡	GM1‡	GM0‡ EXT/$\overline{I}$	CSS	V2	V1	V0
Internal Alphanumerics	0	X	X	0	X	0	0	0
External Alphanumerics	0	X	X	1	X	0	0	0
OSemigraphics — 4	0	X	X	0	X	0	0	0
Semigraphics — 6	0	X	X	1	X	0	0	0
Semigraphics — 8*	0	X	X	0	X	0	1	0
Semigraphics — 12*	0	X	X	0	X	1	0	0
Semigraphics — 24*	0	X	X	0	X	1	1	0
Full Graphics — 1C	1	0	0	0	X	0	0	1
Full Graphics — 1R	1	0	0	1	X	0	0	1
Full Graphics — 2C	1	0	1	0	X	0	1	0
Full Graphics — 2R	1	0	1	1	X	0	1	1
Full Graphics — 3C	1	1	0	0	X	1	0	0
Full Graphics — 3R	1	1	0	1	X	1	0	1
Full Graphics — 6C	1	1	1	0	X	1	1	0
Full Graphics — 6R	1	1	1	1	X	1	1	0
Direct Memory Access†	X	X	X	X	X	1	1	1

* S8, S12, & S24 modes are **not** described in the MC6847 Data Sheet. See appendix "A".
† DMA is identical to 6R except as shown in Figure 5 on page 9.
‡ The function of these control bits differs on the T1 version of the 6847. See the MC6847T1 data sheet for details.

VDG Address Offset

Seven bits (F6, F5, F4, F3, F2, F1 and F0) determine the **Starting Address** for the video display. The "Starting Address" is defined as "the address corresponding to data displayed in the **Upper Left** corner of the TV screen." The "Starting Address" is shown below in binary:

F6	F5	F4	F3	F2	F1	F0	0	0	0	0	0	0	0	0	0

Most Significant Bit

Least Significant Bit

Note that the "Starting Address" may be placed anywhere within the 64K address space with a resolution of 1/2K (the size of one alphanumeric page).

Page Switch

One bit (P1) is used "in place of" A15 from the MC6809E in order to refer access within $0000-$7FFF to one of two 32K byte **pages** of RAM. For systems using the LS783 and 32K bytes of RAM or less, the Page bit serves no useful function and is a "don't care." The LS785 uses the Page bit in conjunction with the memory size bits to determine whether 16K x 1 or 16K x 4 DRAM is being accessed. P1 is set for 16K x 4 and cleared for 16K x 1. The Page bit must also be cleared for the LS785 to function with 4K x 1 DRAMs.

MPU Rate

Two bits (R1, R0) control the clock rate to the MC6809E MPU. The options are:

RATE (FREQUENCY OF "E" CLOCK)	R1	R0
0.9 MHz (Crystal Frequency ÷ 16) Slow	0	0
0.9/1.8 MHz (Address Dependent Rate)	0	1
1.8 MHz (Crystal Frequency ÷ 8) Fast	1	X
(Typical Crystal Frequency = 14.31818 MHz)		

In the "address dependent rate" mode, accesses to \$0000-\$7FFF and \$FF00-\$FF1F are slowed to 0.9 MHz (crystal frequency ÷ 16) and all other addresses are accessed at 1.8 MHz (crystal frequency ÷ 8).

Note: "Slow" (0.9 MHz) operation can be accomplished using 1.0 MHz MC6809E and MC6821 devices. For "Fast" (1.8 MHz) operation, 2.0 MHz MC68B09E and MC68B21 devices must be used.

Memory Size

Two bits (M1 and M0) determine RAM memory size. the options are:

SIZE	M1	M0
One or two banks of 4K x 1 dynamic RAMs	0	0
One or two banks of 16K x 1 dynamic RAMs	0	1
One bank of 16K x 4 dynamic RAMs①	0	1
One bank of 64K x 1 dynamic RAMs	1	0
Up to 64K static RAM*	1	1

① This option is only available when using the LS785.
* Requires a latch for demultiplexing the RAM address.

IMPORTANT!

Note: Be sure to program the SAM for the correct memory size **before** using RAM (i.e., for a subroutine stack).

Map Type

One bit (TY) is used to select between two memory map configurations.

Refer to Figures 14–16 for details. Early versions of the LS783 did not allow the "Fast" MPU rate to be used in conjunction with Map Type "TY = 1." Devices manufactured after January 1, 1983 allow both "Fast" and "Slow" MPU rates to be used with Map Type "TY = 1." (Date of manufacture is marked on devices as YYWW where YY is the year and WW is the week of manufacture).

Writing To The SAM Control Register

Any bit in the control register (CR) may be set by writing to a specific unique address. Each bit has two unique addresses . . . writing to the **even** # address **clears** the bit and writing to the **odd** # address **sets** the bit. (Data on the data bus is irrelevant in this procedure.) The specific addresses are tabulated in Figures 14–16.

If desired, a short routine may be written to program the SAM CR "a word at a time." For example, the following routine copies "B" bits from "A" register to SAM CR addresses beginning with address "X."

```
SAM1     46         ROR   A
         24   06    BCC   SAM2
         30   01    INX   (LEAX1,X)
         A7   80    STA   0,X+
         20   02    BRA   SAM3
SAM2     A7   81    STA   0,X++
SAM3     5A         DEC   B
         26   F2    BNE   SAM1
         39         RTS
```

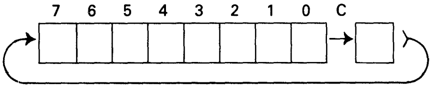
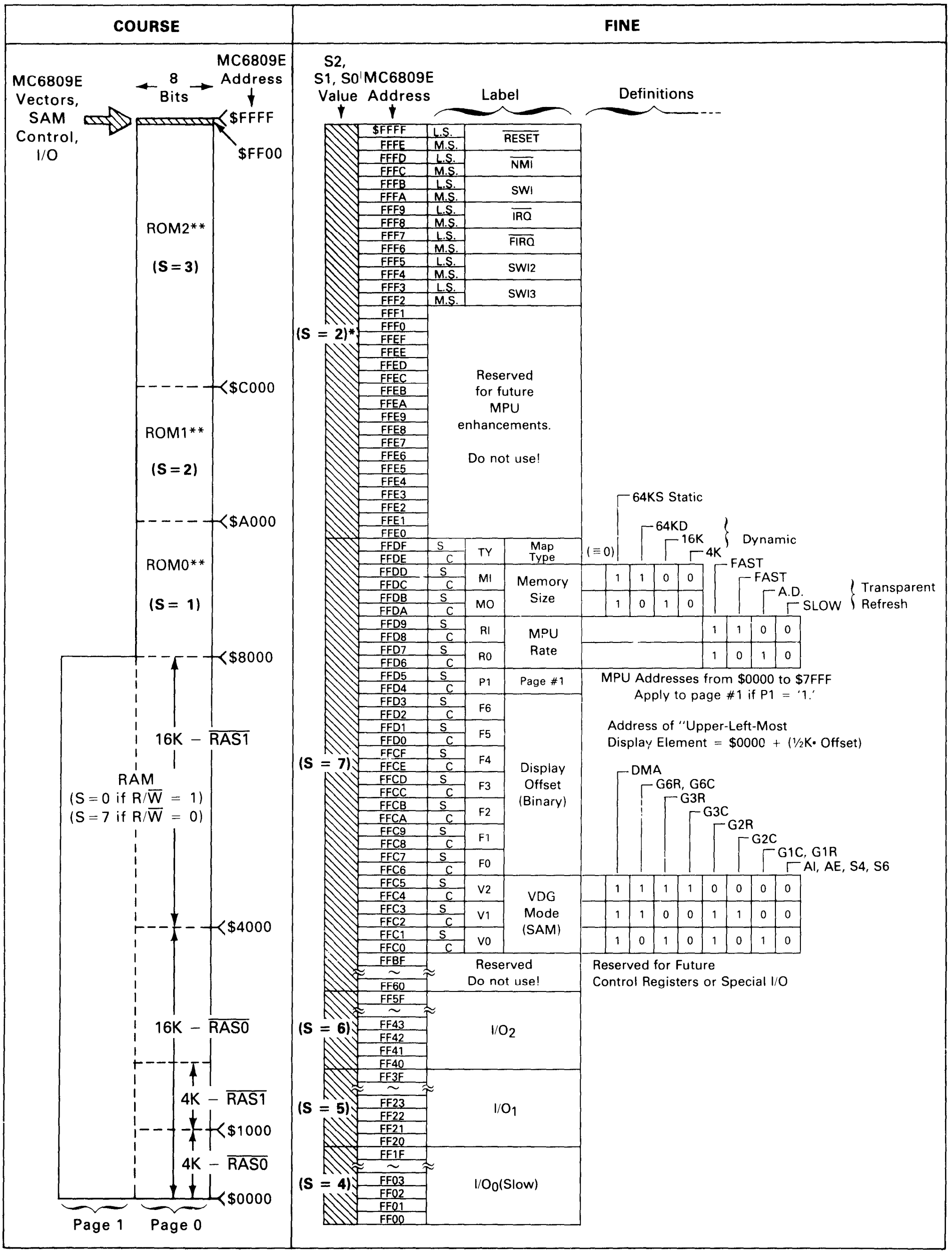


FIGURE 14 — MEMORY MAP (TYPE #0)


COURSE
FINE
MC6809E Vectors, SAM Control, I/O
8 Bits
MC6809E Address
$FFFF
$FF00
ROM2**
(S=3)
$C000
ROM1**
(S=2)
$A000
ROM0**
(S= 1)
$8000
16K − RAS1
RAM
(S=0 if R/W = 1)
(S=7 if R/W = 0)
$4000
16K − RAS0
4K − RAS1
$1000
4K − RAS0
$0000
Page 1
Page 0
S2, S1, S0 Value
MC6809E Address
Label
Definitions
$FFFF L.S. FFFE M.S. RESET
FFFD L.S. FFFC M.S. NMI
FFFB L.S. FFFA M.S. SWI
FFF9 L.S. FFF8 M.S. IRQ
FFF7 L.S. FFF6 M.S. FIRQ
FFF5 L.S. FFF4 M.S. SWI2
FFF3 L.S. FFF2 M.S. SWI3
(S = 2)*
FFF1 FFF0 FFEF FFEE FFED FFEC FFEB FFEA FFE9 FFE8 FFE7 FFE6 FFE5 FFE4 FFE3 FFE2 FFE1 FFE0
Reserved for future MPU enhancements.
Do not use!
FFDF S FFDE C TY Map Type (≡0)
64KS Static
64KD
16K
4K
Dynamic
FFDD S FFDC C M1
FFDB S FFDA C M0
Memory Size
1 1 0 0
1 0 1 0
FAST
FAST
A.D.
SLOW
Transparent Refresh
FFD9 S FFD8 C R1
FFD7 S FFD6 C R0
MPU Rate
1 1 0 0
1 0 1 0
FFD5 S FFD4 C P1 Page #1
MPU Addresses from $0000 to $7FFF Apply to page #1 if P1 = '1.'
(S = 7)
FFD3 S FFD2 C F6
FFD1 S FFD0 C F5
FFCF S FFCE C F4
FFCD S FFCC C F3
FFCB S FFCA C F2
FFC9 S FFC8 C F1
FFC7 S FFC6 C F0
Display Offset (Binary)
Address of "Upper-Left-Most Display Element = $0000 + (½K• Offset)
DMA
G6R, G6C
G3R
G3C
G2R
G2C
G1C, G1R
AI, AE, S4, S6
FFC5 S FFC4 C V2
FFC3 S FFC2 C V1
FFC1 S FFC0 C V0
VDG Mode (SAM)
1 1 1 1 0 0 0 0
1 1 0 0 1 1 0 0
1 0 1 0 1 0 1 0
FFBF ~ FF60
Reserved Do not use!
Reserved for Future Control Registers or Special I/O
(S = 6)
FF5F ~ FF43 FF42 FF41 FF40
I/O2
(S = 5)
FF3F ~ FF23 FF22 FF21 FF20
I/O1
(S = 4)
FF1F ~ FF03 FF02 FF01 FF00
I/O0(Slow)

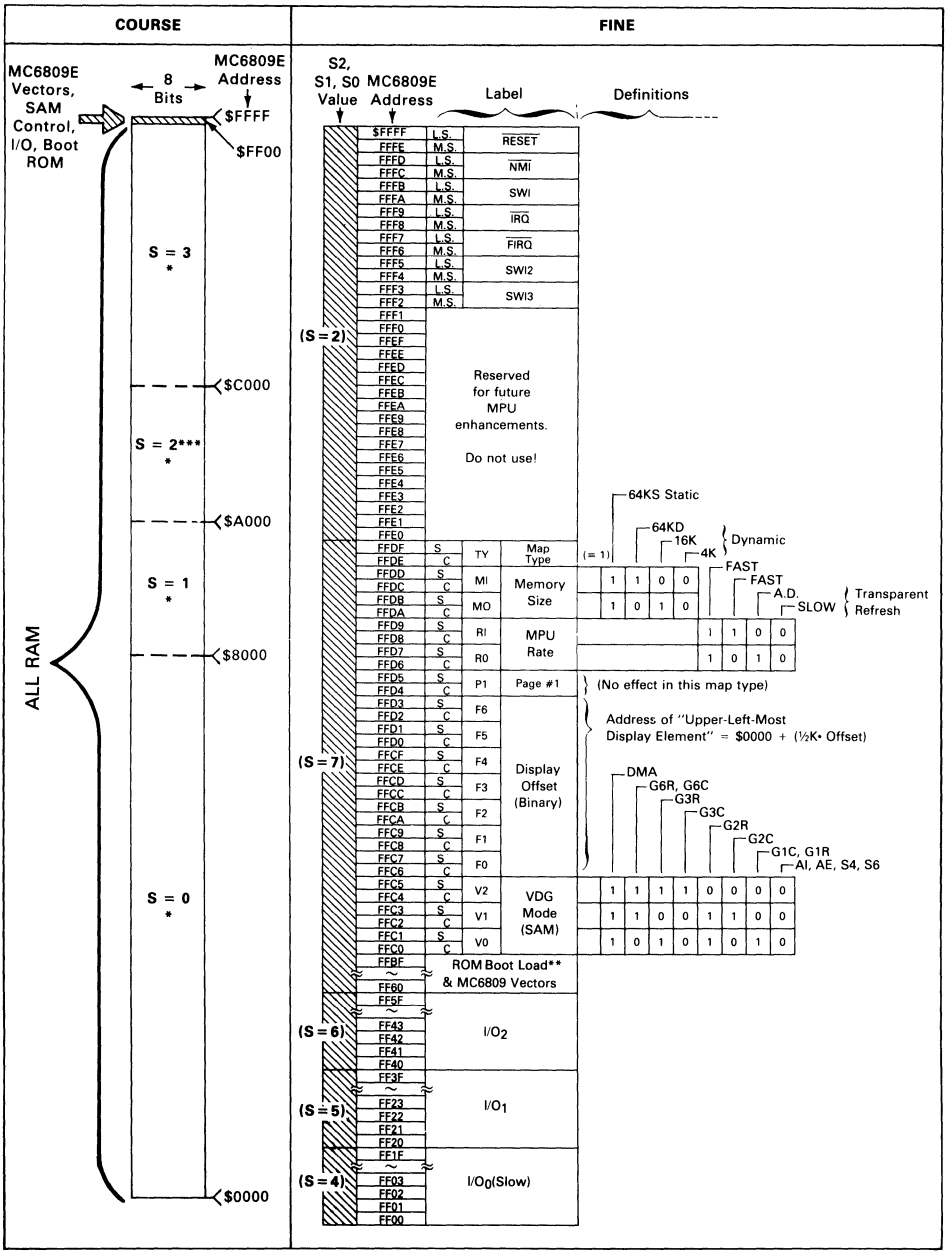
Abbreviations:
- M.S. ≡ Most Significant
- L.S. ≡ Least Significant
- S ≡ Set Bit
- C ≡ Clear Bit (All bits are cleared when SAM is reset.)
- **S** ≡ Device Select value = 4 x S2 + 2 x S1 + 1 x S0

NOTES:

*On LS785, S = 7 if R/W = 0

**This memory area may also be RAM. However, locations $FFE0-$FFFF must be ROM when using LS785.

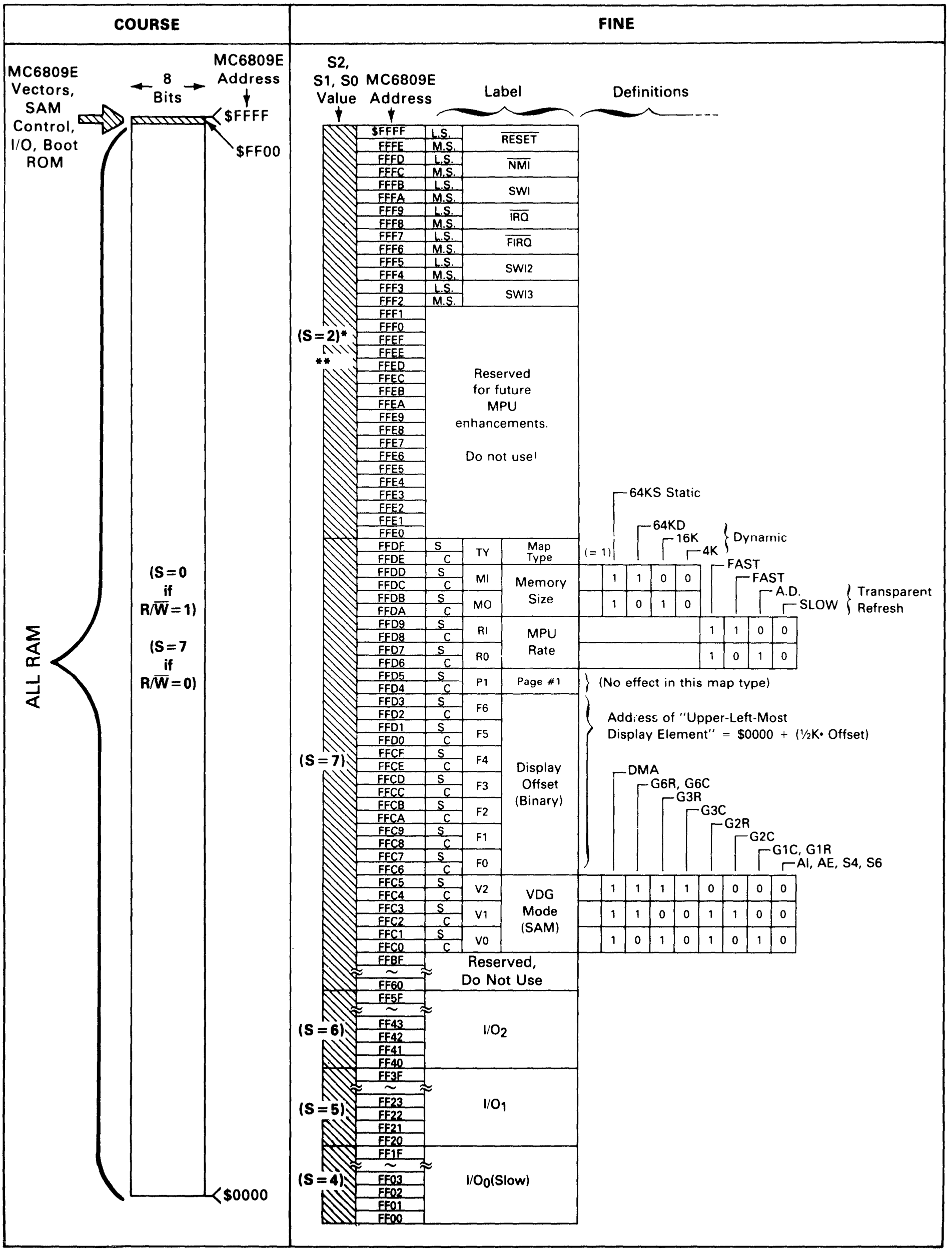
FIGURE 15 — LS783 MEMORY MAP (TYPE #1 64K RAM)


COURSE
FINE
MC6809E Vectors, SAM Control, I/O, Boot ROM
8 Bits
MC6809E Address
$FFFF
$FF00
S = 3 *
$C000
S = 2*** *
$A000
S = 1 *
$8000
S = 0 *
$0000
ALL RAM
S2, S1, S0 Value
MC6809E Address
Label
Definitions
$FFFF L.S. / FFFE M.S. — RESET
FFFD L.S. / FFFC M.S. — NMI
FFFB L.S. / FFFA M.S. — SWI
FFF9 L.S. / FFF8 M.S. — IRQ
FFF7 L.S. / FFF6 M.S. — FIRQ
FFF5 L.S. / FFF4 M.S. — SWI2
FFF3 L.S. / FFF2 M.S. — SWI3
FFF1–FFE0 — Reserved for future MPU enhancements. Do not use!
(S = 2)
FFDF S / FFDE C — TY — Map Type — (= 1)
64KS Static
64KD
16K
4K
Dynamic
FFDD S / FFDC C — MI — Memory Size — 1 1 0 0
FFDB S / FFDA C — MO — 1 0 1 0
FAST
FAST
A.D.
SLOW
Transparent Refresh
FFD9 S / FFD8 C — R1 — MPU Rate — 1 1 0 0
FFD7 S / FFD6 C — R0 — 1 0 1 0
FFD5 S / FFD4 C — P1 — Page #1 — (No effect in this map type)
FFD3 S / FFD2 C — F6
FFD1 S / FFD0 C — F5
FFCF S / FFCE C — F4
FFCD S / FFCC C — F3
FFCB S / FFCA C — F2
FFC9 S / FFC8 C — F1
FFC7 S / FFC6 C — F0
Display Offset (Binary)
Address of "Upper-Left-Most Display Element" = $0000 + (½K• Offset)
(S = 7)
DMA
G6R, G6C
G3R
G3C
G2R
G2C
G1C, G1R
AI, AE, S4, S6
FFC5 S / FFC4 C — V2 — VDG Mode (SAM) — 1 1 1 1 0 0 0 0
FFC3 S / FFC2 C — V1 — 1 1 0 0 1 1 0 0
FFC1 S / FFC0 C — V0 — 1 0 1 0 1 0 1 0
FFBF ~ FF60 — ROM Boot Load** & MC6809 Vectors
FF5F ~ FF43 FF42 FF41 FF40 — I/O2
(S = 6)
FF3F ~ FF23 FF22 FF21 FF20 — I/O1
(S = 5)
FF1F ~ FF03 FF02 FF01 FF00 — I/O0(Slow)
(S = 4)

Abbreviations:
M.S. ≡ Most Significant
L.S. ≡ Least Significant
S ≡ Set Bit
C ≡ Clear Bit
(All bits are cleared when SAM is reset.)
S ≡ Device Select value = 4 x S2 + 2 x S1 + 1 x S0

NOTES:
*S = 0 if R/$\overline{W}$ = 1
**Decode S2, S1, and S0 with an open collector SN74LS156 and 'wire-or' state 7 with state 2. (See Appendix B for suggested decode circuit.)
***To avoid ROM enable during R/$\overline{W}$ = LOW, the ROM at S = 2 must be gated with R/$\overline{W}$. (See Appendix B for suggested decode circuit.)

FIGURE 16 — LS785 MEMORY MAP (TYPE #1 64K RAM)


COURSE
FINE
MC6809E Vectors, SAM Control, I/O, Boot ROM
8 Bits
MC6809E Address
$FFFF
$FF00
(S=0 if R/W̄=1)
(S=7 if R/W̄=0)
ALL RAM
$0000
S2, S1, S0 Value
MC6809E Address
Label
Definitions
(S=2)*
**
(S=7)
(S=6)
(S=5)
(S=4)

MC6809E Address		Label
$FFFF	L.S.	$\overline{RESET}$
FFFE	M.S.	
FFFD	L.S.	$\overline{NMI}$
FFFC	M.S.	
FFFB	L.S.	SWI
FFFA	M.S.	
FFF9	L.S.	$\overline{IRQ}$
FFF8	M.S.	
FFF7	L.S.	$\overline{FIRQ}$
FFF6	M.S.	
FFF5	L.S.	SWI2
FFF4	M.S.	
FFF3	L.S.	SWI3
FFF2	M.S.	
FFF1–FFE0		Reserved for future MPU enhancements. Do not use!

MC6809E Address		Bit	Label	Definitions
FFDF	S	TY	Map Type	(≡ 1)
FFDE	C			
FFDD	S	M1	Memory Size	
FFDC	C			
FFDB	S	M0		
FFDA	C			
FFD9	S	R1	MPU Rate	
FFD8	C			
FFD7	S	R0		
FFD6	C			
FFD5	S	P1	Page #1	(No effect in this map type)
FFD4	C			
FFD3	S	F6	Display Offset (Binary)	Address of "Upper-Left-Most Display Element" = $0000 + (½K• Offset)
FFD2	C			
FFD1	S	F5		
FFD0	C			
FFCF	S	F4		
FFCE	C			
FFCD	S	F3		
FFCC	C			
FFCB	S	F2		
FFCA	C			
FFC9	S	F1		
FFC8	C			
FFC7	S	F0		
FFC6	C			
FFC5	S	V2	VDG Mode (SAM)	
FFC4	C			
FFC3	S	V1		
FFC2	C			
FFC1	S	V0		
FFC0	C			
FFBF ~ FF60			Reserved, Do Not Use	
FF5F ~ FF43, FF42, FF41, FF40			I/O2	
FF3F ~ FF23, FF22, FF21, FF20			I/O1	
FF1F ~ FF03, FF02, FF01, FF00			I/O0(Slow)	

Memory Size	64KS Static	64KD (Dynamic)	16K (Dynamic)	4K (Dynamic)
M1	1	1	0	0
M0	1	0	1	0

MPU Rate	FAST	FAST (Transparent Refresh)	A.D. (Transparent Refresh)	SLOW (Transparent Refresh)
R1	1	1	0	0
R0	1	0	1	0

VDG Mode	DMA	G6R, G6C	G3R	G3C	G2R	G2C	G1C, G1R	AI, AE, S4, S6
V2	1	1	1	1	0	0	0	0
V1	1	1	0	0	1	1	0	0
V0	1	0	1	0	1	0	1	0

Abbreviations:
M.S. ≡ Most Significant
L.S. ≡ Least Significant
S ≡ Set Bit
C ≡ Clear Bit
(All bits are cleared when SAM is reset.)
S ≡ Device Select value = 4 x S2 + 2 x S1 + 1 x S0

NOTES:
*S = 7 if R/W̄ = 0
**Memory locations $FFE0-$FFFF cannot be written to (i.e. write protected).

FIGURE 17 — MEMORY ALLOCATION TABLE
(Also, see the memory MAPs on pages 17 and 18.)

Type # 0: (Primarily for ROM based systems)

Address Range	Intended Use
$FFF2 to FFFF	MC6809E Vectors: $\overline{\text{Reset}}$, $\overline{\text{NMI}}$, SWI, $\overline{\text{IRQ}}$, $\overline{\text{FIRQ}}$, SWI2, SWI3.
FFE0 to FFF1	Reserved for future MPU enhancements.
FFC0 to FFDF	SAM Control Register: V0, – V2, F0 – F6, P, R0, R1, M0, M1, TY.
FF60 to FFBF	Reserved for future control register enhancements.
FF40 to FF5F	I/O_2: Input/Output (PIAs, ACIAs, etc.) To subdivide, use A0–A4.
FF20 to FF3F	I/O_1: Input/Output (PIAs, ACIAs, etc.) To subdivide, use A0–A4.
FF00 to FF1F	I/O_0: Input/Output (PIAs, ACIAs, etc.) To subdivide, use A0–A4.
C000 to FEFF	ROM2: 16K addresses. External cartridge ROM*.
A000 to BFFF	ROM1: 8K addresses. Internal ROM*. Note that MC6809E vector addresses select this ROM*.
8000 to 9FFF	ROM0: 8K addresses. Internal ROM*.
0000 to 7FFF	RAM: 32K addresses. RAM shared by MPU and VDG.

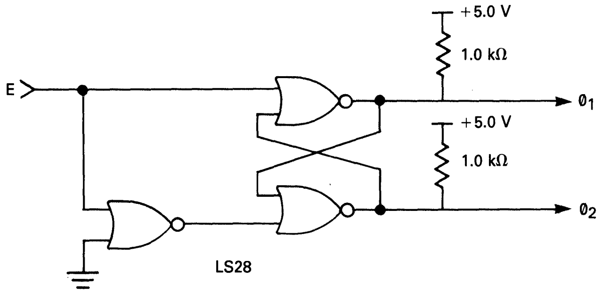
*Not restricted to ROM. For example, RAM or I/O may be used here.

Type # 1: (Primarily for RAM based systems)

Address Range	Intended Use
$FFF2 to FFFF	MC6809E Vectors: $\overline{\text{Reset}}$, $\overline{\text{NMI}}$, SWI, $\overline{\text{IRQ}}$, $\overline{\text{FIRQ}}$, SWI2, SWI3.
FFE0 to FFF1	Reserved for future MPU enhancements.
FFC0 to FFDF	SAM Control Register: V0 – V2, F0 – F6, P, R0, R1, M0, M1, TY.
FF60 to FFBF	Small ROM: Boot load program and initial MC6809 vectors.
FF40 to FF5F	I/O_2: Input/Output (PIAs, ACIAs, etc.) To subdivide, use A0–A4.
FF20 to FF3F	I/O_1: Input/Output (PIAs, ACIAs, etc.) To subdivide, use A0–A4.
FF00 to FF1F	I/O_1: Input/Output (PIAs, ACIAs, etc.) To subdivide, use A0–A4.
0000 to FEFF	RAM: 64K(–256) addresses, shared by MPU and VDG. (If $R/\overline{W}$ = 0 then S = 3 for $C000-$FEFF; S = 2 for $A000-$BFFF; S = 1 for $8000-$9FFF and S = 7 for $0000-$7FFF.)

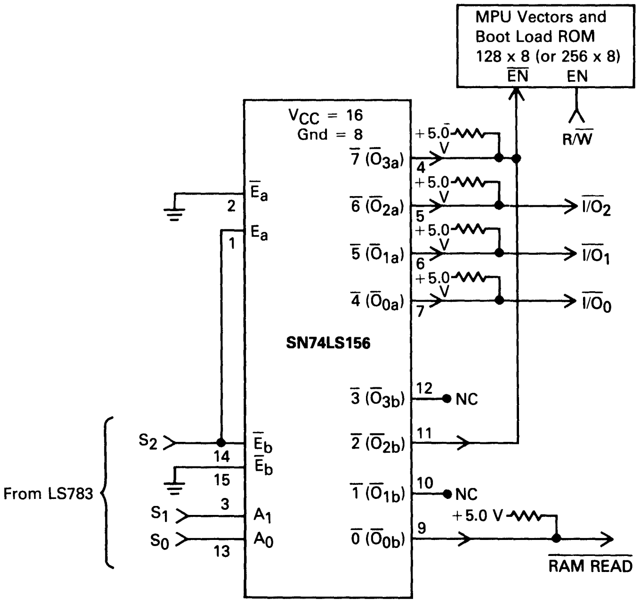
APPENDIX A

Providing a Clock for MC6800 Microprocessors



APPENDIX B

Memory Decode for LS783 "MAP TYPE = 1"


MPU Vectors and
Boot Load ROM
128 x 8 (or 256 x 8)
$\overline{EN}$ EN
R/$\overline{W}$
V_{CC} = 16
Gnd = 8
7 ($\overline{O}_{3a}$)
6 ($\overline{O}_{2a}$)
5 ($\overline{O}_{1a}$)
4 ($\overline{O}_{0a}$)
SN74LS156
3 ($\overline{O}_{3b}$)
2 ($\overline{O}_{2b}$)
1 ($\overline{O}_{1b}$)
0 ($\overline{O}_{0b}$)
$\overline{E}_a$
E_a
$\overline{E}_b$
$\overline{E}_b$
A_1
A_0
+5.0 V
$\overline{I/O}_2$
$\overline{I/O}_1$
$\overline{I/O}_0$
NC
NC
$\overline{\text{RAM READ}}$
From LS783
S_2
S_1
S_0
1
2
3
4
5
6
7
9
10
11
12
13
14
15

APPENDIX C

VDG/SAM Video Display System Offers 3 New Modes

by

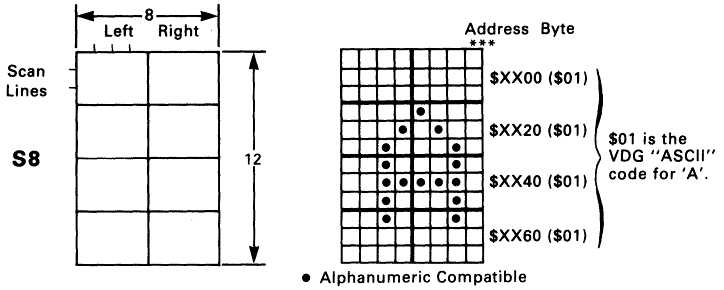
Paul Fletcher

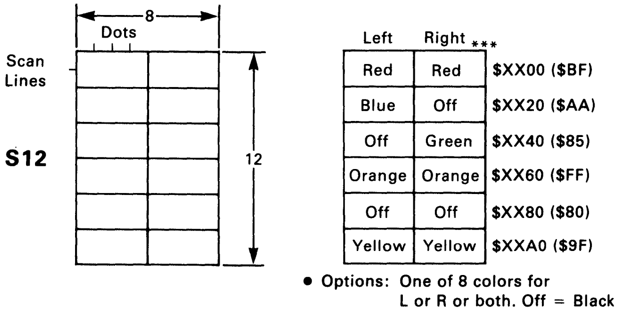
There are three new modes created when the VDG and SAM are used together in a video display system. These modes offer alphanumeric compatibility with 8 color low-to-high resolution graphics, 64H x 64 V, 64H x 96 V, 64H x 192 V. The new modes S8, S12, and S24 are created by placing the VDG in the Alpha Internal mode and having the SAM in a 2K, 3K or 6K full color graphics mode. In all modes the VDG's S/$\overline{A}$ and Inv. pins are connected to data bits DD7 and DD6 to allow switching on the fly between Alpha and Semigraphics and between inverted and non-inverted alpha. This method is used in most VDG systems to obtain maximum flexibility.

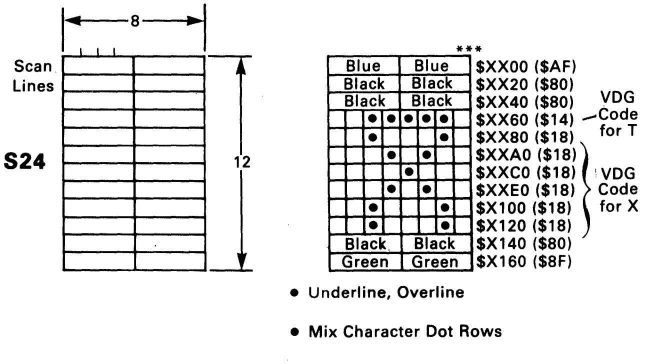
The three modes divide the standard 8*12 dot box used by the VDG for the standard alpha and semigraphics modes into eight 4*3 dot boxes for the S8 mode, twelve 4*2 dot boxes for the S12 mode, and twenty-four 4*1 dot boxes for the S24 mode. Figure 17 shows the arrangement of these boxes. One byte is needed to control two horizontally consecutive boxes. It therefore takes four bytes for the S8, six bytes for the S12, and 12 bytes for the S24 mode to control the entire 8*12 dot box. These two horizontally consecutive boxes have four combinations of luminance controlled by bits B0–B3. For convenience B2 should be made equal to B0 and B3 should be made equal to B1. This eliminates a screen placement problem which would cause other codes to change patterns when moved vertically on the screen. The illuminated boxes can be one of eight colors which are controlled by B4–B6 (see Figure 18). The bytes needed to control all the boxes in the 8*12 dot box must be spaced 32 address spaces apart in the display RAM because of the addressing scheme originally used in the VDG and duplicated by the SAM. This means to place an alphanumeric character on the TV screen it requires 4, 6, or 12 bytes depending on the mode used. These bytes are placed 32 memory locations apart in the display RAM (see Figure 18). This multiple byte format allows the mixing of character rows of different characters in the same 8*12 dot box creating new characters and symbols. It also allows overlining and underlining in eight colors by switching to semigraphics at the correct time.

These new modes optimize the memory versus screen density tradeoffs for RF performance on color TVs. This could make them the most versatile of all the modes depending on the users creativity and the software sophistication.

FIGURE C1 — DISLAY MODES S8, S12, S24
Bit/Visible Dot Correlation

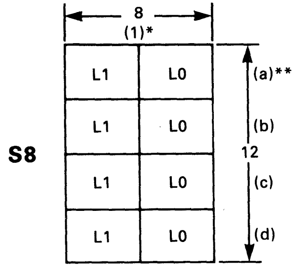

8
Left
Right
Scan Lines
S8
12
Address Byte
***
$XX00 ($01)
$XX20 ($01)
$XX40 ($01)
$XX60 ($01)
$01 is the VDG "ASCII" code for 'A'.
• Alphanumeric Compatible


8
Dots
Scan Lines
S12
12
Left
Right
***
Red
Red
$XX00 ($BF)
Blue
Off
$XX20 ($AA)
Off
Green
$XX40 ($85)
Orange
Orange
$XX60 ($FF)
Off
Off
$XX80 ($80)
Yellow
Yellow
$XXA0 ($9F)
• Options: One of 8 colors for L or R or both. Off = Black


8
Scan Lines
S24
12
***
Blue
Blue
$XX00 ($AF)
Black
Black
$XX20 ($80)
Black
Black
$XX40 ($80)
$XX60 ($14)
$XX80 ($18)
VDG Code for T
$XXA0 ($18)
$XXC0 ($18)
$XXE0 ($18)
$X100 ($18)
$X120 ($18)
VDG Code for X
Black
Black
$X140 ($80)
Green
Green
$X160 ($8F)
• Underline, Overline
• Mix Character Dot Rows

*** Characters will always remain in standard VDG positions.

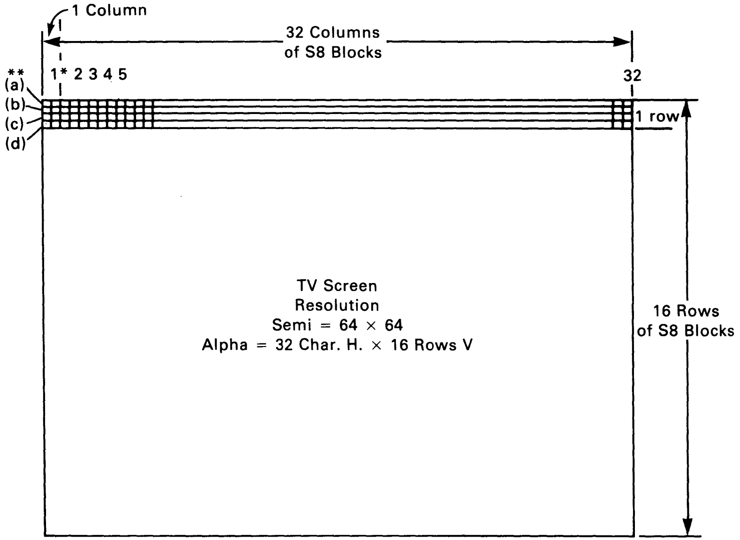
FIGURE C2 — S8 DISPLAY FORMAT EXAMPLES


8
(1)*
S8
L1
L0
L1
L0
L1
L0
L1
L0
(a)**
(b)
12
(c)
(d)

B7							B0	
X	C2	C1	C0	L3	L2	L1	L0	Semi
S/$\overline{A}$	Inv	X	X	X	X	X	X	Alpha
Extra		ASCII Code						

LX	C2	C1	C0	Color
0	X	X	X	Black
1	0	0	0	Green
1	0	0	1	Yellow
1	0	1	0	Blue
1	0	1	1	Red
1	1	0	0	Buff
1	1	0	1	Cyan
1	1	1	0	Magenta
1	1	1	1	

B3,B1	B2,B0		4	
0	0	=	Off	Off
0	1	=	Off	Color
1	0	=	Color	Off
1	1	=	Color	


1 Column
32 Columns of S8 Blocks
**
(a)
(b)
(c)
(d)
1* 2 3 4 5
32
1 row
TV Screen Resolution
Semi = 64 × 64
Alpha = 32 Char. H. × 16 Rows V
16 Rows of S8 Blocks

S8 Screen Memory Map

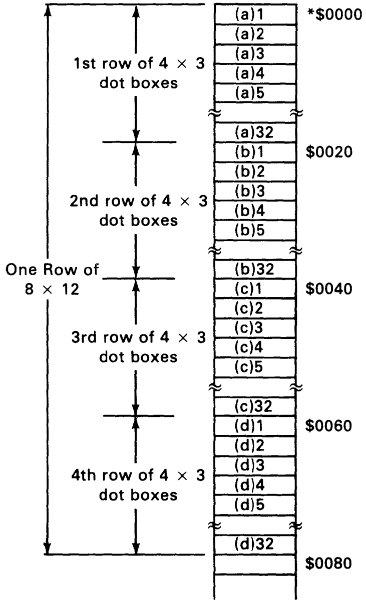

1st row of 4 × 3 dot boxes
2nd row of 4 × 3 dot boxes
One Row of 8 × 12
3rd row of 4 × 3 dot boxes
4th row of 4 × 3 dot boxes
(a)1
(a)2
(a)3
(a)4
(a)5
(a)32
(b)1
(b)2
(b)3
(b)4
(b)5
(b)32
(c)1
(c)2
(c)3
(c)4
(c)5
(c)32
(d)1
(d)2
(d)3
(d)4
(d)5
(d)32
*$0000
$0020
$0040
$0060
$0080

FIGURE 18 — EQUIVALENT OF OSCILLATOR INPUT AND OUTPUT

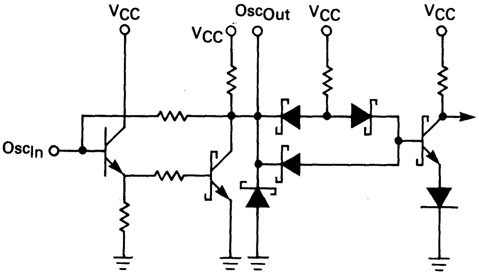

VCC
OscOut
VCC
VCC
VCC
OscIn

FIGURE 21 — E AND Q OUTPUTS

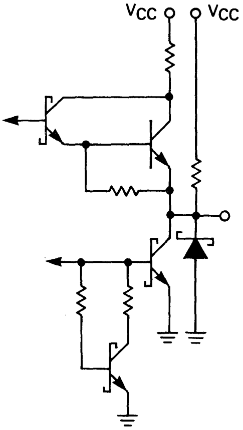


FIGURE 19 — DA0 INPUT

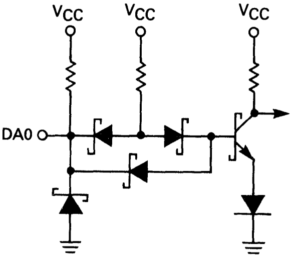

VCC
VCC
VCC
DA0

FIGURE 22 — TYPICAL INPUT

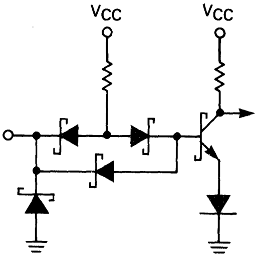


FIGURE 20 — VClk INPUT/OUTPUT

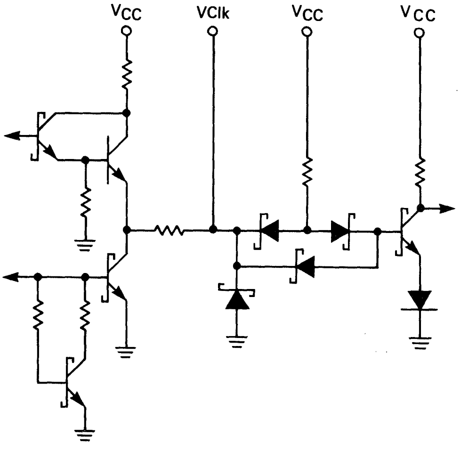

VCC
VClk
VCC
VCC

FIGURE 23 — TYPICAL OUTPUT

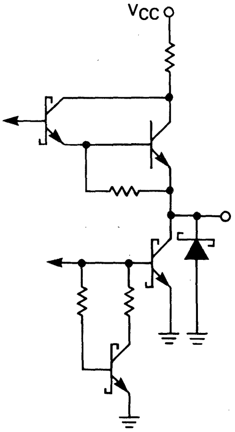
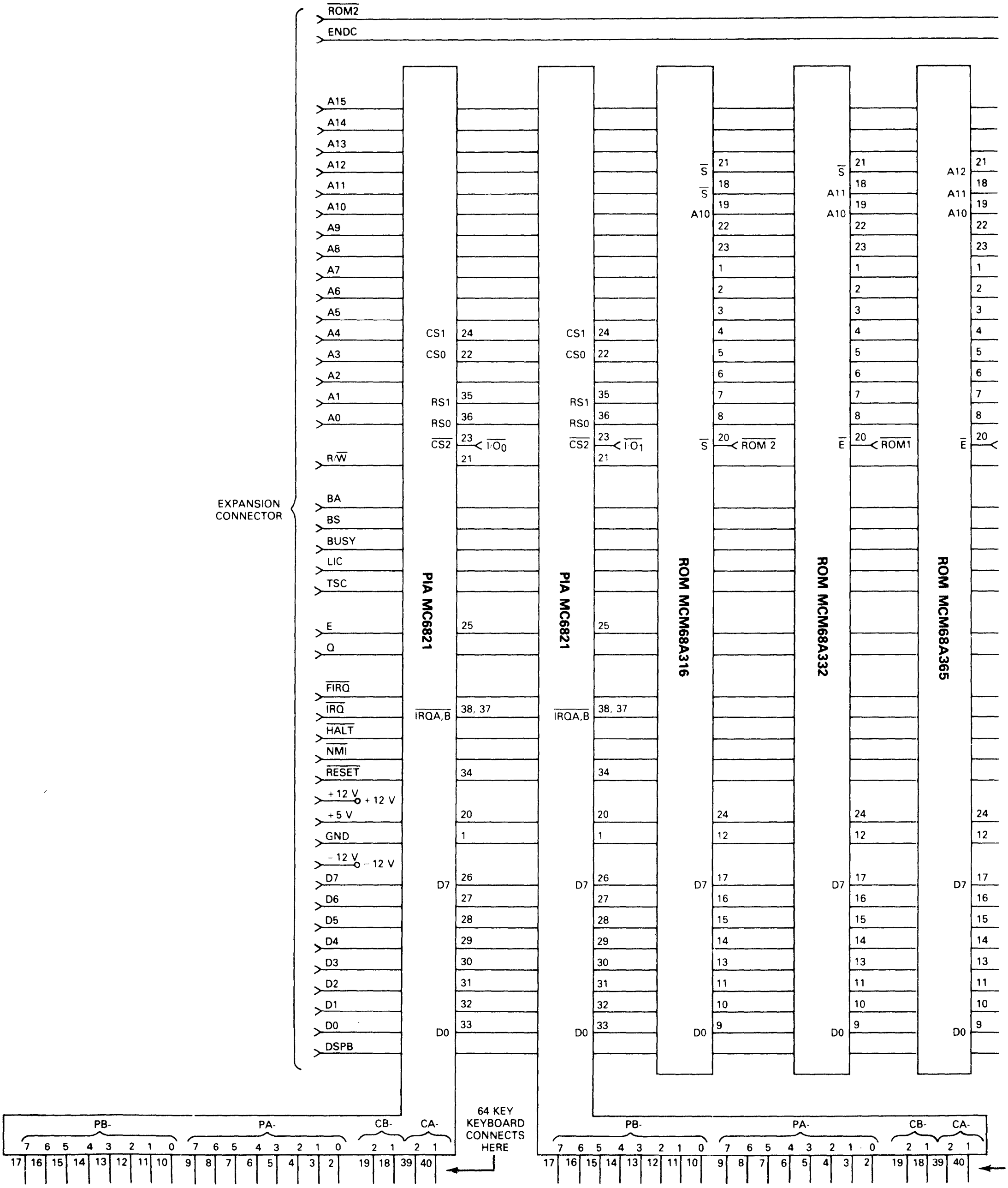
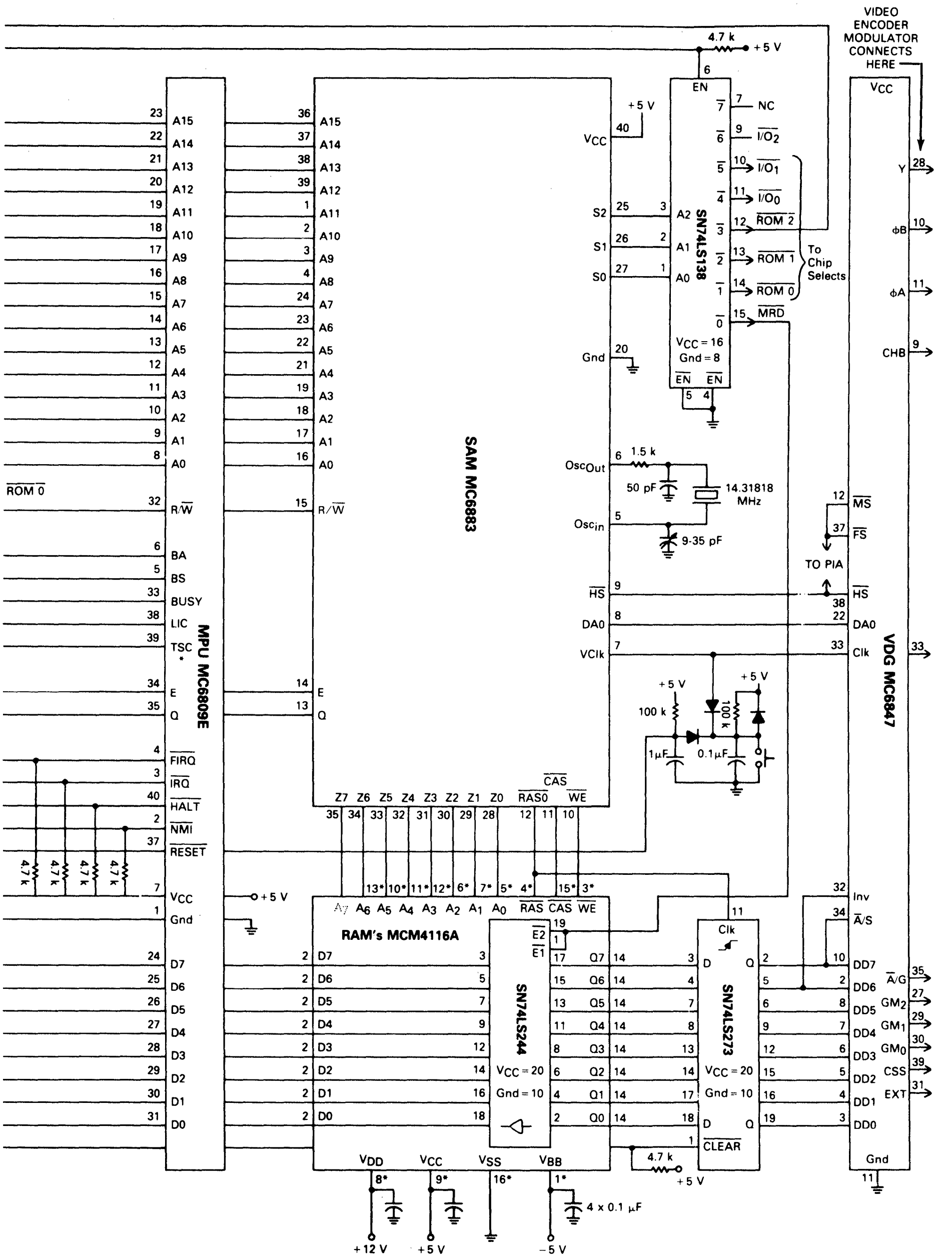


FIGURE 24— EXAMPLE of MC6809E, MC6883 and MC6847 COMPUTER


ROM2
ENDC
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
R/W
EXPANSION CONNECTOR
BA
BS
BUSY
LIC
TSC
E
Q
FIRQ
IRQ
HALT
NMI
RESET
+12 V
+12 V
+5 V
GND
−12 V
−12 V
D7
D6
D5
D4
D3
D2
D1
D0
DSPB
PIA MC6821
CS1 24
CS0 22
RS1 35
RS0 36
CS2 23 IO0
21
25
IRQA,B 38, 37
34
20
1
D7 26
27
28
29
30
31
32
D0 33
PIA MC6821
CS1 24
CS0 22
RS1 35
RS0 36
CS2 23 IO1
21
25
IRQA,B 38, 37
34
20
1
D7 26
27
28
29
30
31
32
D0 33
ROM MCM68A316
S 21
S 18
A10 19
22
23
1
2
3
4
5
6
7
8
S 20 ROM 2
24
12
D7 17
16
15
14
13
11
10
D0 9
ROM MCM68A332
S 21
A11 18
A10 19
22
23
1
2
3
4
5
6
7
8
E 20 ROM1
24
12
D7 17
16
15
14
13
11
10
D0 9
ROM MCM68A365
A12 21
A11 18
A10 19
22
23
1
2
3
4
5
6
7
8
E 20
24
12
D7 17
16
15
14
13
11
10
D0 9
PB-
7 6 5 4 3 2 1 0
17 16 15 14 13 12 11 10
PA-
7 6 5 4 3 2 1 0
9 8 7 6 5 4 3 2
CB- CA-
2 1 2 1
19 18 39 40
64 KEY KEYBOARD CONNECTS HERE
PB-
7 6 5 4 3 2 1 0
17 16 15 14 13 12 11 10
PA-
7 6 5 4 3 2 1 0
9 8 7 6 5 4 3 2
CB- CA-
2 1 2 1
19 18 39 40


VIDEO ENCODER MODULATOR CONNECTS HERE
MPU MC6809E
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
ROM 0
R/W
BA
BS
BUSY
LIC
TSC
E
Q
FIRQ
IRQ
HALT
NMI
RESET
VCC
Gnd
D7 D6 D5 D4 D3 D2 D1 D0
4.7 k
+5 V
SAM MC6883
VCC
S2
S1
S0
Gnd
OscOut
OscIn
1.5 k
50 pF
14.31818 MHz
9-35 pF
HS
DA0
VClk
100 k
1 μF
0.1 μF
Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0 RAS0 CAS WE
SN74LS138
EN
A2 A1 A0
VCC = 16
Gnd = 8
NC
I/O2
I/O1
I/O0
ROM 2
ROM 1
ROM 0
MRD
To Chip Selects
RAM's MCM4116A
A7 A6 A5 A4 A3 A2 A1 A0 RAS CAS WE
VDD VCC VSS VBB
+12 V
+5 V
-5 V
4 x 0.1 μF
SN74LS244
E2
E1
VCC = 20
Gnd = 10
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
SN74LS273
Clk
D
Q
CLEAR
VDG MC6847
VCC
Y
ϕB
ϕA
CHB
MS
FS
TO PIA
HS
DA0
Clk
Inv
A/S
DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0
A/G
GM2
GM1
GM0
CSS
EXT
Gnd

MC6847 Mode Control & Misc I/O connects here.

*This pin number on 8 different RAM chips is connected to this point.

MOTOROLA

SN54/74LS795
SN54/74LS796
SN54/74LS797
SN54/74LS798

TRI-STATE OCTAL BUFFERS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS795 thru SN54LS/74LS798 device types provide a second source for the 71/81LS95 thru 71/81LS98 series. These devices are octal low power Schottky versions of the 70/8095 thru 70/8098 3-STATE Hex Buffers. The LS795 and LS797 are noninverting and the LS796 and LS798 are inverting functions. On each buffer, one of the two inputs is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer. On the LS795 and LS796 access is through a 2-input NOR gate, with all eight 3-STATE enable lines common. On the LS797 and LS798, four buffers are enabled from one common line and the other four buffers from another common line. On all device types the 3-STATE condition is achieved by applying a high logic level to the enable pins.

TRUTH TABLES

LS795

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

LS796

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

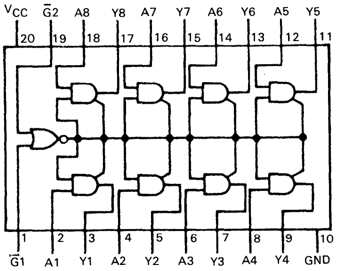
LS797

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

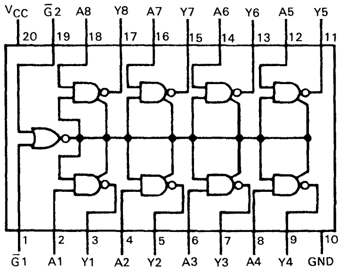
LS798

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

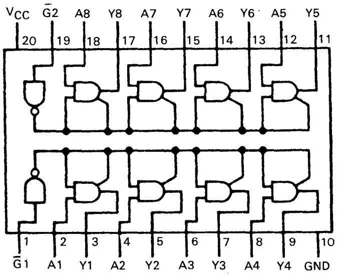
LOGIC DIAGRAMS


VCC
Ḡ2
A8
Y8
A7
Y7
A6
Y6
A5
Y5
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
Ḡ1
A1
Y1
A2
Y2
A3
Y3
A4
Y4
GND

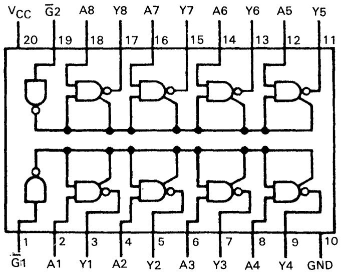
SN54LS/74LS795


VCC
Ḡ2
A8
Y8
A7
Y7
A6
Y6
A5
Y5
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
Ḡ1
A1
Y1
A2
Y2
A3
Y3
A4
Y4
GND

SN54LS/74LS796


VCC
Ḡ2
A8
Y8
A7
Y7
A6
Y6
A5
Y5
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
Ḡ1
A1
Y1
A2
Y2
A3
Y3
A4
Y4
GND

SN54LS/74LS797


VCC
Ḡ2
A8
Y8
A7
Y7
A6
Y6
A5
Y5
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
Ḡ1
A1
Y1
A2
Y2
A3
Y3
A4
Y4
GND

SN54LS/74LS798

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

GUARANTEED OPERATING RANGES

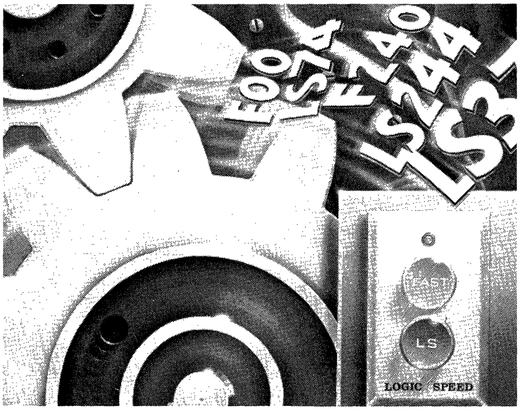
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−2.6 −5.0	mA
I_{OL}	Output Current — Low	54 74			8.0 16	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 8.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 16 mA	
I_{OZH}	Output Off Current—High				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current—Low				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					−0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current A Input, Both $\overline{G}$ at 0.4 V $\overline{G}$ Input				-0.400 -0.400	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	A Input, Both $\overline{G}$ at 2.0 V				−20	μA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current	LS795/LS797			26	mA	V_{CC} = MAX	
		LS796/LS798			21	mA		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS795/LS797			LS796/LS798				
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay		11 15	16 22		6.0 13	10 17	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PZH} t_{PZL}	Output Enable Time		16 13	25 20		17 16	27 25	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		13 19	20 27		13 18	20 27	ns	C_L = 5.0 pF


E00
LS
F
LS244
LS3
F240
FAST
LS
LOGIC SPEED

Reliability Data

THE "BETTER" PROGRAM

The "BETTER" program is offered on logic only, in dual-in-line ceramic and plastic packages.

Better Processing — Standard Product Plus:

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions — 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- 100% post burn-in functional and dc parametric tests at 25°C (or max rated T_A at Motorola's option). Maximum PDA of 2% (functional) and 5% (DC and functional).

HOW TO ORDER

MC10101	P	D
Part Identification	Standard Package Suffix	BETTER PROCESSING LEVEL II = SUFFIX D

Part Marking

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

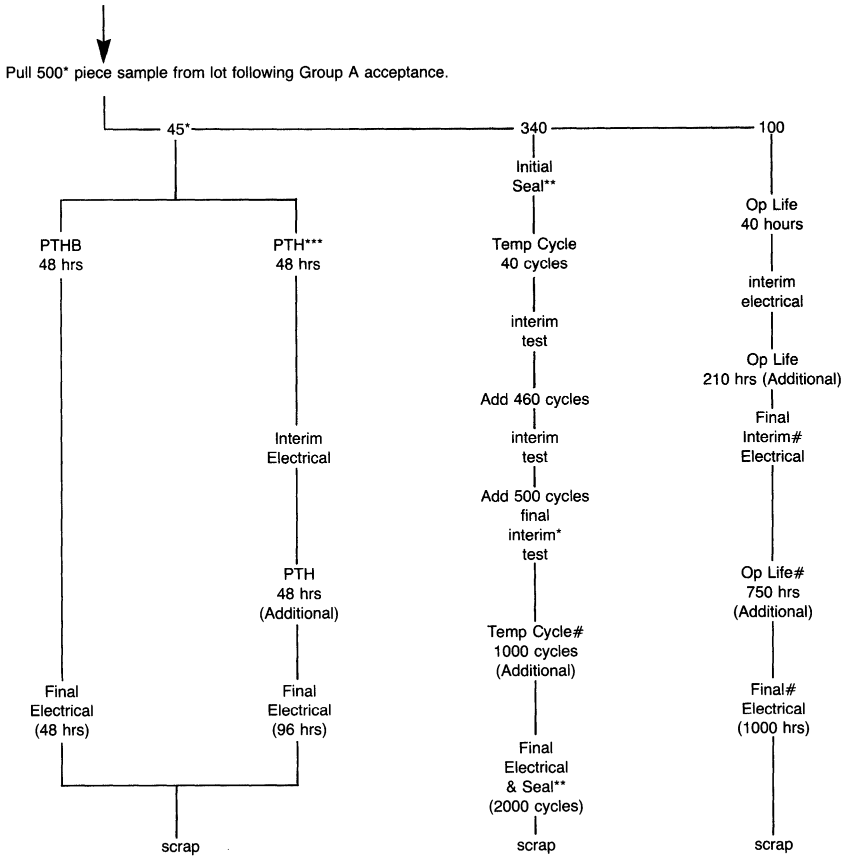
"RAP"
Reliability Audit Program for Logic Integrated Circuits

1.0 INTRODUCTION

The Reliability Audit Program developed in March 1977 is the Motorola internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations, and monthly reporting of results. These reports are available at all sales offices. Also available is the "Reliability and Quality Handbook" which contains data for all Motorola Semiconductors (#BR518S).

RAP is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in section 2.0. Frequency of testing is specified per internal document 12MRM15301A.

2.0 RAP TEST FLOW


Pull 500* piece sample from lot following Group A acceptance.
45*
340
100
PTHB
48 hrs
PTH***
48 hrs
Interim
Electrical
PTH
48 hrs
(Additional)
Final
Electrical
(48 hrs)
Final
Electrical
(96 hrs)
scrap
Initial
Seal**
Temp Cycle
40 cycles
interim
test
Add 460 cycles
interim
test
Add 500 cycles
final
interim*
test
Temp Cycle#
1000 cycles
(Additional)
Final
Electrical
& Seal**
(2000 cycles)
scrap
Op Life
40 hours
interim
electrical
Op Life
210 hrs (Additional)
Final
Interim#
Electrical
Op Life#
750 hrs
(Additional)
Final#
Electrical
(1000 hrs)
scrap

#One sample per month for FAST, LS, 10H, 10K, MG CMOS, and HSL CMOS.
*PTHB or PTH not required for hermetic products: reduce total sample size to 450 pcs.
Additional sample reductions for high pin-count devices per TABLE II notes.
**Seal (Fine & Gross Leak) required only for hermetic products.
***PTH to be used when sockets for PTHB are not available.

3.0 TEST CONDITIONS AND COMMENTS

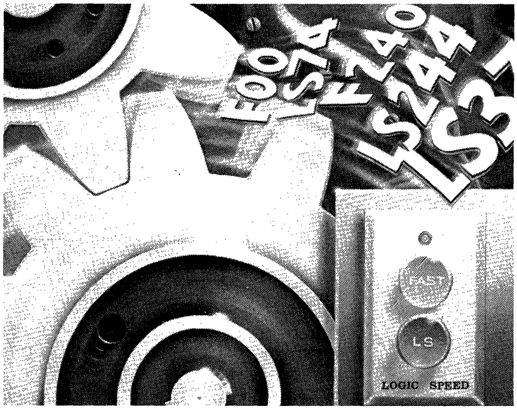
PTHB — 15 psig/121°C/100% RH at rated V_{CC} or V_{EE} — to be performed on plastic encapsulated devices only.

TEMP CYCLING — MIL-STD-883, Method 1010, Condition C, $-65°C/+150°C$.

OP LIFE — MIL-STD-883, Method 1005, Condition C (Power plus Reverse Bias), $T_A = 145°C$.

NOTES:

1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. Sampling to include all package types routinely.
4. Device types sampled will be by generic type within each logic I/C product family (MECL, TTL, etc.) and will include all assembly locations (Korea, Philippines, Malaysia, etc.)
5. 16 hrs. PTHB is equivalent to approximatley 800 hours of 85°C/85% RH THB for $V_{CC} \leq 15$ V.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. Special device specifications (48A's) for logic products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.


F00
LS74
F240
LS244
LS3
FAST
LS
LOGIC SPEED

Package Information Including Surface Mount

BIPOLAR LOGIC SURFACE MOUNT

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and/ or offer increased functions with the same size product.

SURFACE MOUNT AVAILABILITY

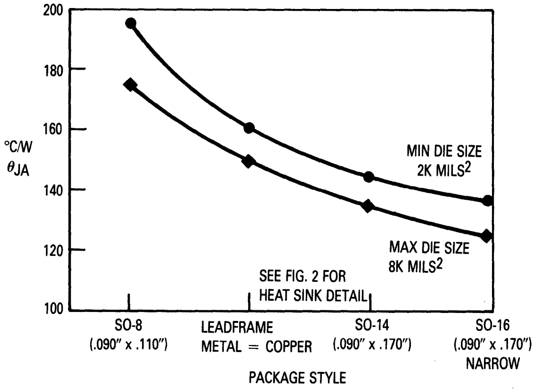
Bipolar Logic is currently offering LS-TTL and FAST-TTL in production quantities in SOIC packages.

Refer to the following Selector Guides (SG-60, SG-113, BR127) which indicate availability and package type for these families.

These families may be ordered in rails or on Tape and Reel. Refer to Tape and Reel information for ordering details.

THERMAL DATA

The power dissipation of surface mount packages is dependent on many factors that must be taken into consideration in the initial board design. The board material, the board surface metal thickness, pad area and the proximity to other heat generating components all have a bearing on the device dissipation capability.



DATA TAKEN USING PHILIPS SO TEST BOARD #7322-078, 80873

Figure 2-1. Thermal Resistance, Junction-To-Ambient (°C/W)

Measurement specimens are solder mounted on printed circuit card 19 mm x 28 mm x 1.5 mm in still air. No auxiliary thermal condition aids are used.

This data was collected using thermal test die in 20-pin PLCC packages on PLCC test boards (2.24" x 2.24" x .062" glass epoxy, type FR-4, with solder coated 1 oz./sq. ft. copper).

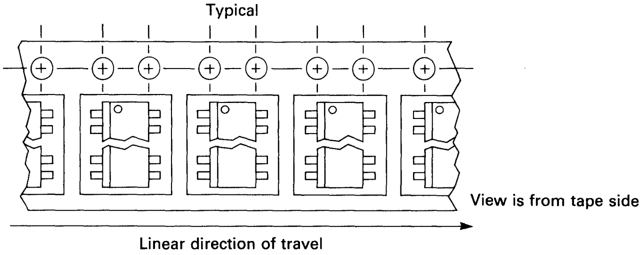
TAPE AND REEL

STANDARD BIPOLAR LOGIC INTEGRATED CIRCUITS

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

MECHANICAL POLARIZATION

SOIC DEVICES



GENERAL INFORMATION

— Reel Size 13 inch (330 mm) Suffix R2
— Tape Width 12 mm to 24 mm (see table)
— Units/Reel (see table)
— No Partial Reel Counts Available and Minimum Lot Size is Per Table

ORDERING INFORMATION

To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

EXAMPLE:

Tape and Reel Suffix

	Magazines (Rails)‡	13 Inch Tape and Reel
	*	
SN74LSXXD	NR	R2
SN74LSXXDW	NR	R2
MC74FXXD	NR	R2
MC74FXXDW	NR	R2

* NR = No Suffix Required

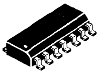
‡ All rail orders are packaged in UNIT/PAK. For full details, order BR378/D.

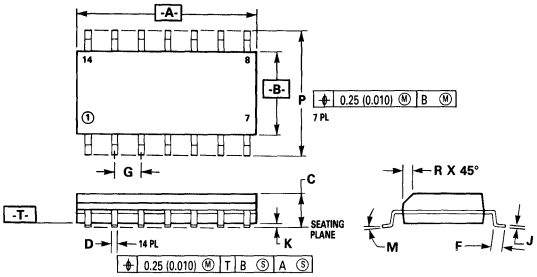
TABLE 2.1 Tape and Reel Data

Device Type	Tape Width (mm)	Device/Reel	Reel Size (inch)	Min Lot Size Per Part No. Tape and Reel
SO-8	12	2,500	13	5,000
SO-14	16	2,500	13	5,000
SO-16	16	2,500	13	5,000
SO-16 Wide	16	1,000	13	5,000
SO-20 Wide	24	1,000	13	5,000

PACKAGE OUTLINES

Case 751A D Suffix
14-Pin Plastic
SO-14



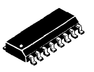

-A-
14
8
1
7
-B-
P
0.25 (0.010) Ⓜ B Ⓜ
7 PL
G
C
R X 45°
-T-
SEATING PLANE
D
14 PL
K
M
F
J
0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

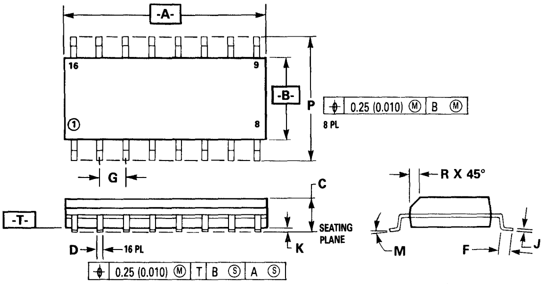
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

Case 751B D Suffix
16-Pin Plastic
SO-16



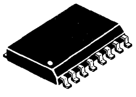

-A-
16
9
1
8
-B-
P
0.25 (0.010) Ⓜ B Ⓜ
8 PL
G
C
R X 45°
-T-
SEATING PLANE
D
16 PL
K
M
F
J
0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

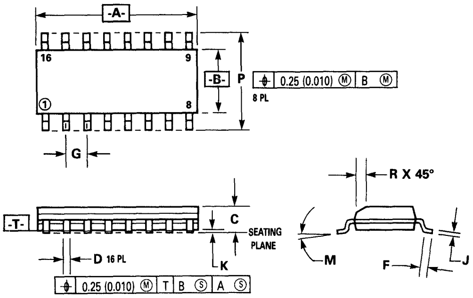
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

Case 751G DW Suffix
16-Pin Plastic
SO-16 (WIDE)




-A-
16
9
1
8
-B-
P
0.25 (0.010) Ⓜ B Ⓜ
8 PL
G
R X 45°
-T-
C
SEATING PLANE
D 16 PL
K
M
F
J
0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

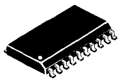
NOTES:

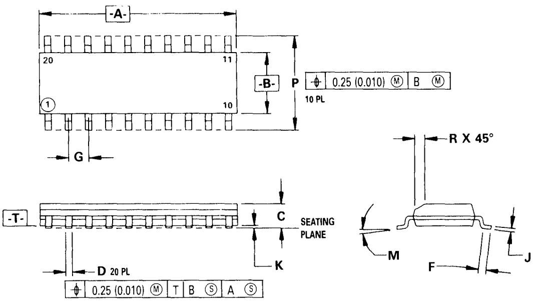
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

PACKAGE OUTLINES

SOIC (continued)

Case 751D DW Suffix
20-Pin Plastic
SO-20 (WIDE)




-A-
20
11
1
10
-B-
P
0.25 (0.010) Ⓜ B Ⓜ
10 PL
G
R X 45°
-T-
C
SEATING PLANE
K
D 20 PL
0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ
M
F
J

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

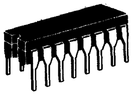
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

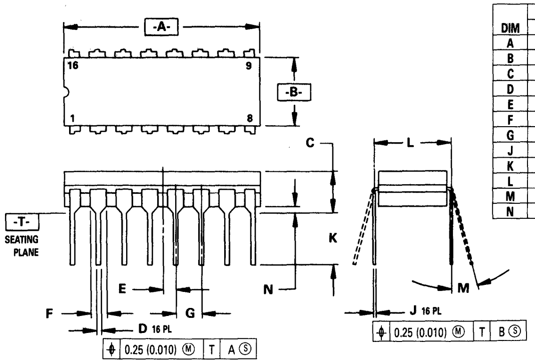
7

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE

Case 620-09
16-Pin Ceramic Dual In-Line

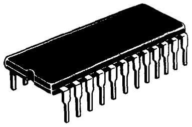


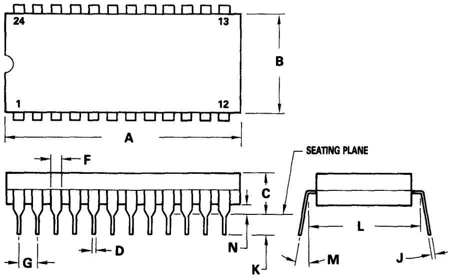

-A-
16
9
1
8
-B-
C
L
-T-
SEATING PLANE
K
E
N
M
F
G
D 16 PL
J 16 PL
0.25 (0.010) Ⓜ T AⓈ
0.25 (0.010) Ⓜ T BⓈ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

Case 623-05
24-Pin Ceramic Dual In-Line

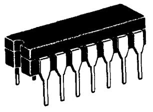


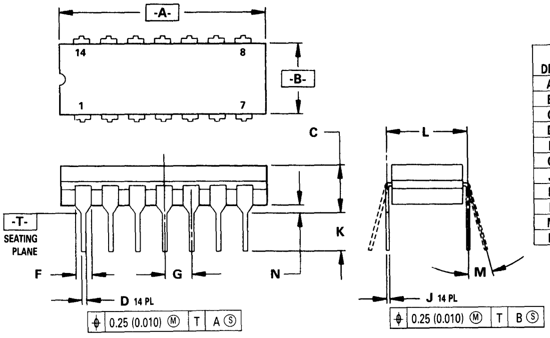

24
13
1
12
B
A
F
SEATING PLANE
C
L
N
K
G
D
M
J

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

Case 632-08
14-Pin Ceramic Dual In-Line




-A-
14
8
1
7
-B-
C
L
-T-
SEATING PLANE
K
N
M
F
G
D 14 PL
J 14 PL
0.25 (0.010) Ⓜ T AⓈ
0.25 (0.010) Ⓜ T BⓈ

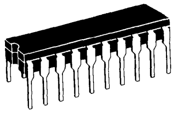
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

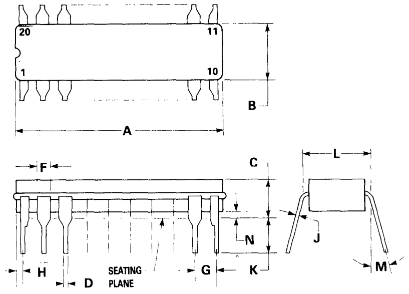
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE (continued)

Case 732-03
20-Pin Ceramic Dual In-Line

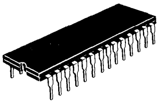


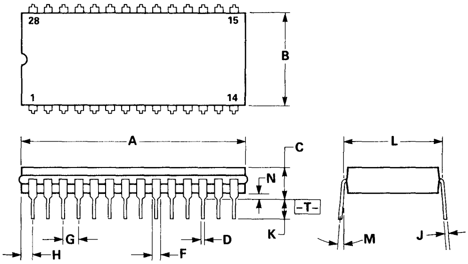


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.04C

Case 733-04
28-Pin Ceramic Dual In-Line

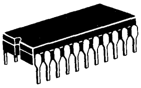


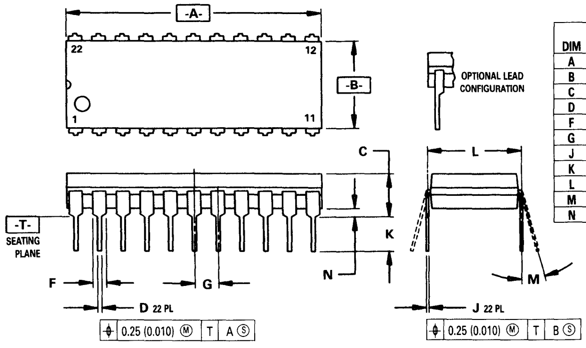


NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   -⌖- ϕ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING & TOLERANCING PER Y14.5, 1982.
7. CONTROLLING DIM: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

Case 736-05
22-Pin Ceramic Dual In-Line





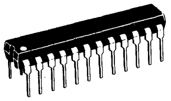
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

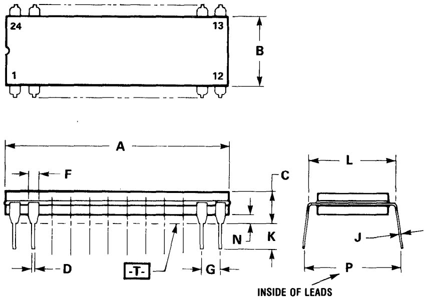
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.93	27.81	1.060	1.095
B	9.15	9.90	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.39	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.39	0.008	0.015
K	3.18	4.31	0.125	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE (continued)

Case 758-01
24-Pin Ceramic Dual In-Line

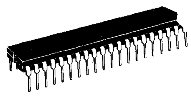


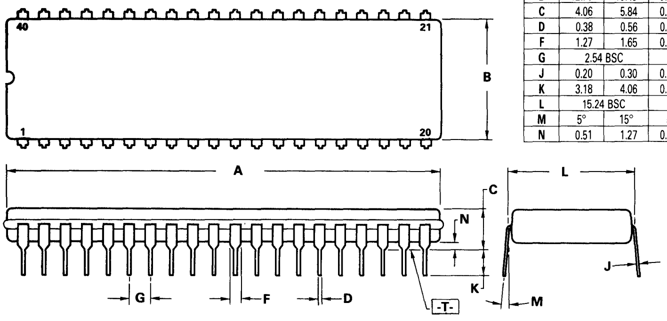


NOTES:
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
   ⌖ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

Case 734-04
J Suffix
Ceramic Package



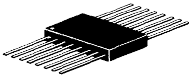


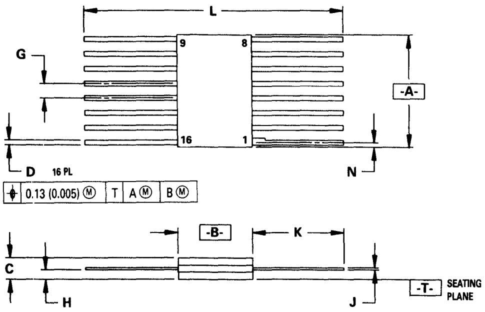
NOTES:
1. DIM -A- IS A DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

CERAMIC FLATPAK

Case 650-05
16-Pin Ceramic Flatpak





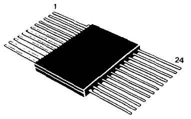
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

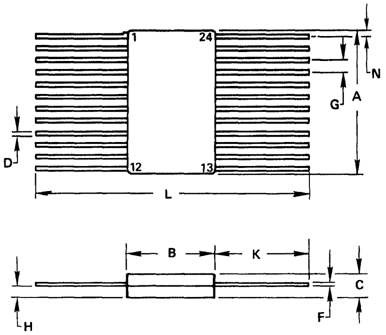
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	1.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

PACKAGE OUTLINES

CERAMIC FLATPAK (continued)

Case 652-02
24-Pin Ceramic Flatpak



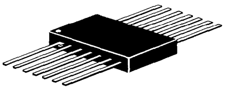


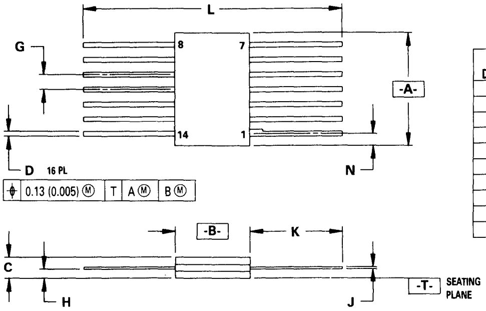
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

CASE 652-02

Case 717-04
14-Pin Ceramic Flatpak

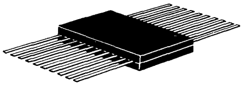


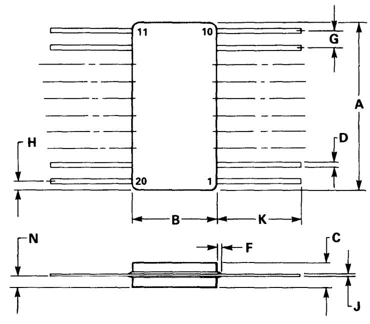


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	1.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	1.14	—	0.045

Case 737-02
20-Pin Ceramic Flatpak





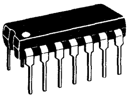
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

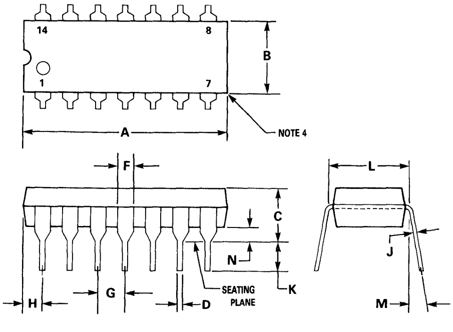
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	13.08	—	0.515
B	5.84	7.11	0.230	0.280
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	—	0.25	—	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	—	9.14	—	0.360
N	—	1.02	—	0.040

PACKAGE OUTLINES

PLASTIC

Case 646-06
14-Pin Plastic

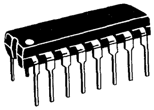


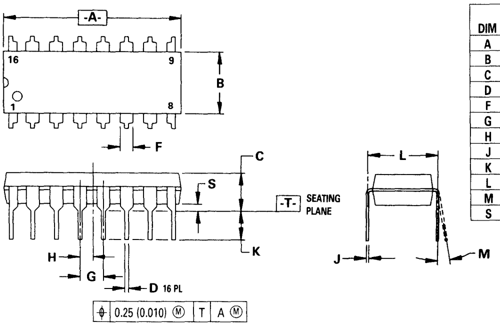


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

Case 648-08
16-Pin Plastic

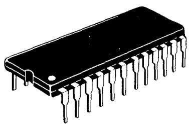


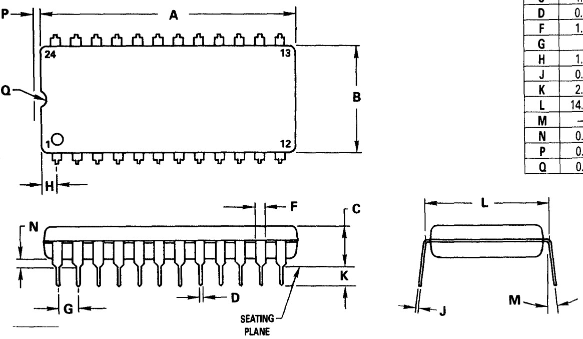


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 649-03
24-Pin Plastic





NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

1 Selection Information FAST/LS

2 Circuit Characteristics

3 Design Considerations and Testing

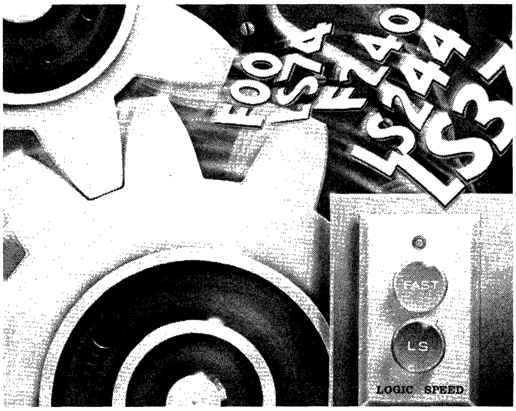
4 FAST Data Sheets

5 LS Data Sheets

6 Reliability Data

7 Package Information Including Surface Mount

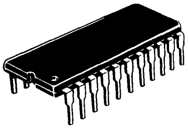
FAST AND LS


LS244
FAST
LS
LOGIC SPEED

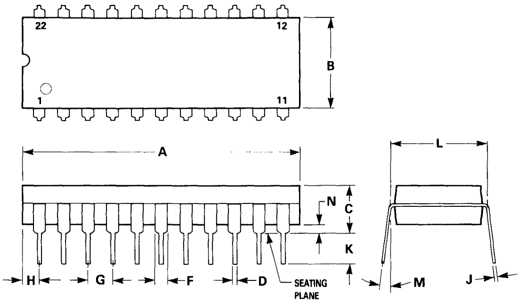
PACKAGE OUTLINES

PLASTIC (continued)

Case 708-04
22-Pin Plastic

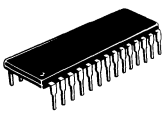


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

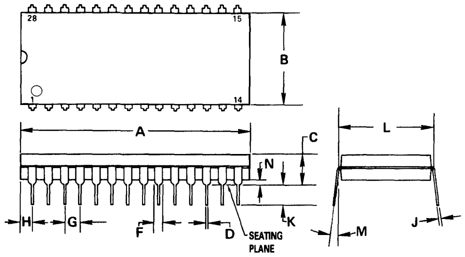


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Case 710-02
28-Pin Plastic

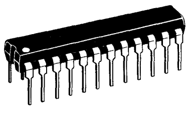


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

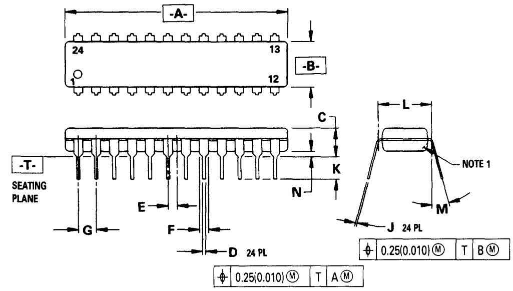


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Case 724-03
24-Pin Plastic



NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

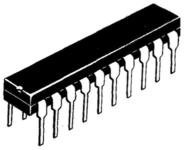


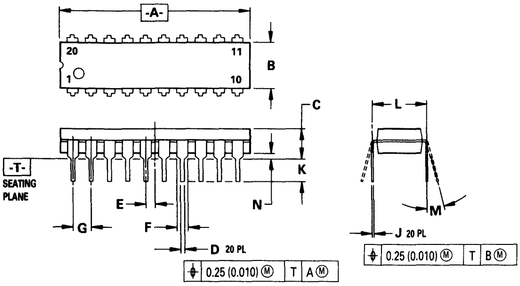
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

PACKAGE OUTLINES

PLASTIC (continued)

Case 738-03
20-Pin Plastic

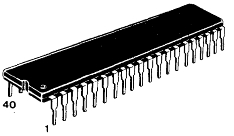




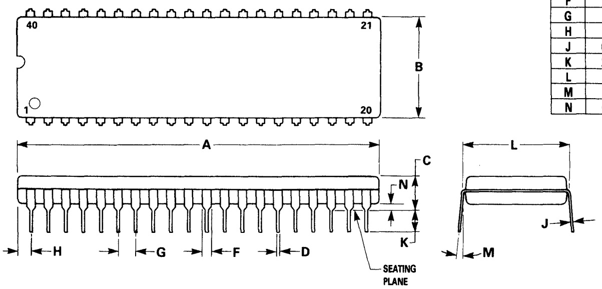
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

Case 711-03
40-Pin Plastic



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

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